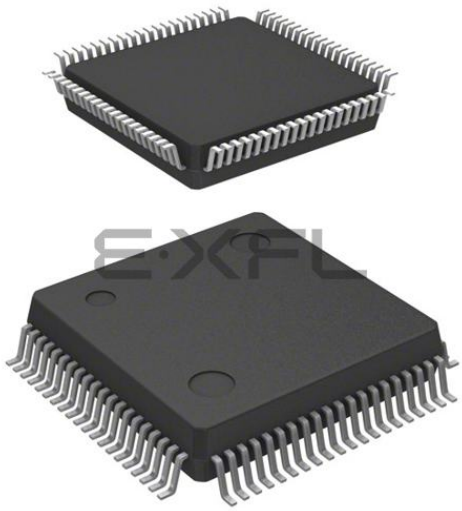

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Details	
Product Status	Active
Core Processor	H8/300H
Core Size	16-Bit
Speed	10MHz
Connectivity	I²C, IrDA, SCI
Peripherals	LCD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	52KB (52K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38076rh10v

User's Manual

16

The revision list can be viewed directly by clicking the title page.

The revision list summarizes the locations of revisions and additions. Details should always be checked by referring to the relevant text.

H8/38076R Group

Hardware Manual

Renesas 16-Bit Single-Chip Microcomputer
H8 Family/H8/300H Super Low Power Series

H8/38076RF
H8/38076R
H8/38075R
H8/38074R
H8/38073R

Renesas Electronics
www.renesas.com

Rev.4.00 2006.08

Application notes:

Document Title	Document No.
F-ZTAT Microcomputer On-Board Programming	REJ05B0523

		Coordinate	
Pad No.	**Pad Name**	**X (µm)**	**Y (µm)**
61	P85/SEG30	2223	1987
62	P86/SEG31	1987	2223
63	P87/SEG32	1852	2223
64	PB7/AN7	1483	2223
65	PB6/AN6	1341	2223
66	PB5/AN5	1150	2223
67	PB4/AN4	941	2223
68	PB3/AN3	732	2223
69	PB2/AN2/$\overline{\text{IRQ3}}$	523	2223
70	PB1/AN1/$\overline{\text{IRQ1}}$	314	2223
71	PB0/AN0/$\overline{\text{IRQ0}}$	105	2223
72	AVcc	–105	2223
73	Vss/AVss	–314	2223
74	IRQAEC	–523	2223
75	P90/PWM1	–732	2223
76	P91/PWM2	–941	2223
77	P92/$\overline{\text{IRQ4}}$	–1150	2223
78	P93	–1360	2223
79	P10/AEVH	–1569	2223
80	P11/AEVL	–1778	2223
81	P12/TIOCA1/TCLKA	–1987	2223

Note: The power supply (Vss) pads in pad numbers 12 and 13 must not be open but connected.
When the TEST pad in pad number 16 is not used as the $\overline{\text{ADTRG}}$ pin, it must be connected to the Vss voltage level. If not, this LSI does not operate correctly.
When the TEST pad is used as the $\overline{\text{ADTRG}}$ pin, the function should be changed to the $\overline{\text{ADTRG}}$ pin at Vss voltage level during a reset in advance.

Table 2.7 Branch Instructions

Instruction	Size	Function
Bcc*	—	Branches to a specified address if a specified condition is true. The branching conditions are listed below.

Mnemonic	Description	Condition
BRA(BT)	Always (true)	Always
BRN(BF)	Never (false)	Never
BHI	High	C ∨ Z = 0
BLS	Low or same	C ∨ Z = 1
BCC(BHS)	Carry clear (high or same)	C = 0
BCS(BLO)	Carry set (low)	C = 1
BNE	Not equal	Z = 0
BEQ	Equal	Z = 1
BVC	Overflow clear	V = 0
BVS	Overflow set	V = 1
BPL	Plus	N = 0
BMI	Minus	N = 1
BGE	Greater or equal	N ⊕ V = 0
BLT	Less than	N ⊕ V = 1
BGT	Greater than	Z∨(N ⊕ V) = 0
BLE	Less or equal	Z∨(N ⊕ V) = 1

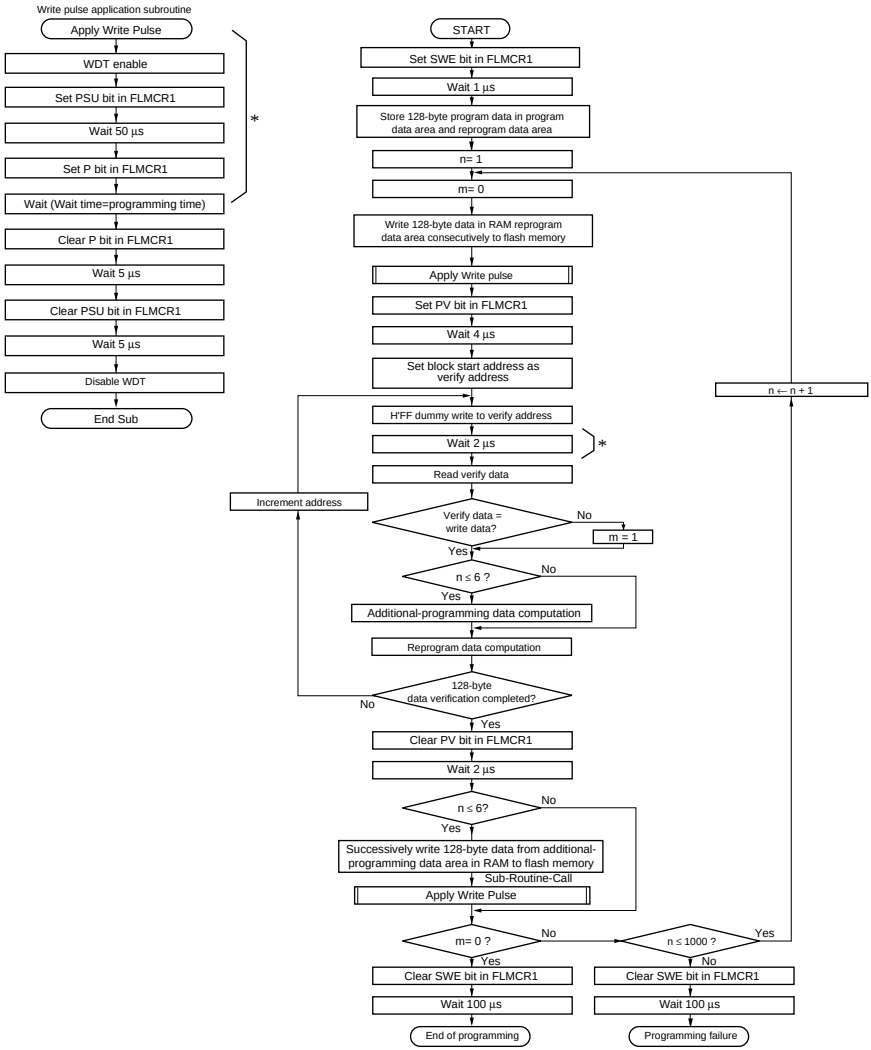
JMP	—	Branches unconditionally to a specified address.
BSR	—	Branches to a subroutine at a specified address.
JSR	—	Branches to a subroutine at a specified address.
RTS	—	Returns from a subroutine

Note: * Bcc is the general name for conditional branch instructions.

Table 4.2 Interrupt Sources, Vector Addresses, and Interrupt Priorities

Origin of Interrupt Source	Name	Vector Number	Vector Address	IPR	Priority
Reset	$\overline{\text{RES}}$, Watchdog Timer	0	H'0000	—	High
NMI	NMI	3	H'0006		
Address break	Break conditions satisfied	5	H'000A		
External pins	IRQ0	6	H'000C	IPRA7, IPRA6	
	IRQ1	7	H'000E	IPRA5, IPRA4	
	IRQAEC	8	H'0010	IPRA3, IPRA2	
	IRQ3	9	H'0012	IPRA1, IPRA0	
	IRQ4	10	H'0014		
	WKP0	11	H'0016	IPRB7, IPRB6	
	WKP1	12	H'0018		
	WKP2	13	H'001A		
	WKP3	14	H'001C		
	WKP4	15	H'001E		
	WKP5	16	H'0020		
	WKP6	17	H'0022		
	WKP7	18	H'0024		
RTC	0.25-second overflow	19	H'0026	IPRB5, IPRB4	
	0.5-second overflow	20	H'0028		
	Second periodic overflow	21	H'002A		
	Minute periodic overflow	22	H'002C		
	Hour periodic overflow	23	H'002E		
	Day-of-week periodic overflow	24	H'0030		
	Week periodic overflow	25	H'0032		
	Free-running overflow	26	H'0034		Low

8. The maximum number of repetitions of the program/program-verify sequence of the same bit is 1,000.



Note: *The RTS instruction must not be used during the following 1. and 2. periods.
1. A period between 128-byte data programming to flash memory and the P bit clearing
2. A period between dummy writing of H'FF to a verify address and verify data reading

Figure 7.3 Program/Program-Verify Flowchart

9.5.1 Port Data Register 6 (PDR6)

PDR6 is a register that stores data of port 6.

Bit	Bit Name	Initial Value	R/W	Description
7	P67	0	R/W	If port 6 is read while PCR6 bits are set to 1, the values stored in PDR6 are read, regardless of the actual pin states. If port 6 is read while PCR6 bits are cleared to 0, the pin states are read.
6	P66	0	R/W	
5	P65	0	R/W	
4	P64	0	R/W	
3	P63	0	R/W	
2	P62	0	R/W	
1	P61	0	R/W	
0	P60	0	R/W	

9.5.2 Port Control Register 6 (PCR6)

PCR6 selects inputs/outputs in bit units for pins to be used as general I/O ports of port 6.

Bit	Bit Name	Initial Value	R/W	Description
7	PCR67	0	W	Setting a PCR6 bit to 1 makes the corresponding pin an output pin, while clearing the bit to 0 makes the pin an input pin. The settings in PCR6 and in PDR6 are valid when the corresponding pin is designated as a general I/O pin.
6	PCR66	0	W	
5	PCR65	0	W	
4	PCR64	0	W	
3	PCR63	0	W	PCR6 is a write-only register. These bits are always read as 1.
2	PCR62	0	W	
1	PCR61	0	W	
0	PCR60	0	W	

9.7.1 Port Data Register 8 (PDR8)

PDR8 is a register that stores data of port 8.

Bit	Bit Name	Initial Value	R/W	Description
7	P87	0	R/W	If port 8 is read while PCR8 bits are set to 1, the values stored in PDR8 are read, regardless of the actual pin states. If port 8 is read while PCR8 bits are cleared to 0, the pin states are read.
6	P86	0	R/W	
5	P85	0	R/W	
4	P84	0	R/W	
3	P83	0	R/W	
2	P82	0	R/W	
1	P81	0	R/W	
0	P80	0	R/W	

9.7.2 Port Control Register 8 (PCR8)

PCR8 selects inputs/outputs in bit units for pins to be used as general I/O ports of port 8.

Bit	Bit Name	Initial Value	R/W	Description
7	PCR87	0	W	Setting a PCR8 bit to 1 makes the corresponding pin (P87 to P80) an output pin, while clearing the bit to 0 makes the pin an input pin. The settings in PCR8 and in PDR8 are valid when the corresponding pin is designated as a general I/O pin.
6	PCR86	0	W	
5	PCR85	0	W	
4	PCR84	0	W	
3	PCR83	0	W	PCR8 is a write-only register. These bits are always read as 1.
2	PCR82	0	W	
1	PCR81	0	W	
0	PCR80	0	W	

9.8.2 Port Control Register 9 (PCR9)

PCR9 selects inputs/outputs in bit units for pins to be used as general I/O ports of port 9.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 1	—	Reserved These bits are always read as 1 and cannot be modified.
3	PCR93	0	W	Setting a PCR9 bit to 1 makes the corresponding pin an output pin, while clearing the bit to 0 makes the pin an input pin. The settings in PCR9 and in PDR9 are valid when the corresponding pin is designated as a general I/O pin. PCR9 is a write-only register. These bits are always read as 1.
2	PCR92	0	W	
1	PCR91	0	W	
0	PCR90	0	W	

9.8.3 Port Mode Register 9 (PMR9)

PMR9 controls the selection of functions for port 9 pins.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 1	—	Reserved These bits are always read as 1 and cannot be modified.
3	—	0	R/W	Reserved Although this bit is readable/writable, 1 should not be written to this bit.
2	IRQ4	0	R/W	P92/$\overline{\text{IRQ4}}$ Pin Function Switch Selects whether pin P92/$\overline{\text{IRQ4}}$ is used as P92 or as $\overline{\text{IRQ4}}$. 0: P92 I/O pin 1: $\overline{\text{IRQ4}}$ input pin

- PB2/AN2/$\overline{\text{IRQ3}}$ pin

  The pin function is switched as shown below according to the combination of the CH3 to CH0 bits in AMR and IRQ3 bit in PMRB.

IRQ3	0		1
CH3 to CH0	Other than B'0110	B'0110	x
Pin Function	PB2 input pin	AN2 input pin	$\overline{\text{IRQ3}}$ input pin

[Legend] x: Don't care.

- PB1/AN1/$\overline{\text{IRQ1}}$ pin

  The pin function is switched as shown below according to the combination of the CH3 to CH0 bits in AMR and IRQ1 bit in PMRB.

IRQ1	0		1
CH3 to CH0	Other than B'0101	B'0101	x
Pin Function	PB1 input pin	AN1 input pin	$\overline{\text{IRQ1}}$ input pin

[Legend] x: Don't care.

- PB0/AN0/$\overline{\text{IRQ0}}$ pin

  The pin function is switched as shown below according to the combination of the CH3 to CH0 bits in AMR and IRQ0 bit in PMRB.

IRQ0	0		1
CH3 to CH0	Other than B'0100	B'0100	x
Pin Function	PB0 input pin	AN0 input pin	$\overline{\text{IRQ0}}$ input pin

[Legend] x: Don't care.

11.3 Register Descriptions

The timer F has the following registers.

- Timer counters FH and FL (TCFH, TCFL)
- Output compare registers FH and FL (OCRFH, OCRFL)
- Timer control register F (TCRF)
- Timer control/status register F (TCSRF)

11.3.1 Timer Counters FH and FL (TCFH, TCFL)

TCF is a 16-bit read/write up-counter configured by cascaded connection of 8-bit timer counters TCFH and TCFL. In addition to the use of TCF as a 16-bit counter with TCFH as the upper 8 bits and TCFL as the lower 8 bits, TCFH and TCFL can also be used as independent 8-bit counters.

TCFH and TCFL are initialized to H'00 upon a reset.

(1) 16-Bit Mode (TCF)

When CKSH2 is cleared to 0 in TCRF, TCF operates as a 16-bit counter. The TCF input clock is selected by bits CKSL2 to CKSL0 in TCRF.

TCF can be cleared in the event of a compare match by means of CCLRH in TCSRF.

When TCF overflows from H'FFFF to H'0000, OVFH is set to 1 in TCSRF. If OVIEH in TCSRF is 1 at this time, IRRTFH is set to 1 in IRR2, and if IENTFH in IENR2 is 1, an interrupt request is sent to the CPU.

(2) 8-Bit Mode (TCFH/TCFL)

When CKSH2 is set to 1 in TCRF, TCFH and TCFL operate as two independent 8-bit counters. The TCFH (TCFL) input clock is selected by bits CKSH2 to CKSH0 (CKSL2 to CKSL0) in TCRF.

TCFH (TCFL) can be cleared in the event of a compare match by means of CCLRH (CCLRL) in TCSRF.

When TCFH (TCFL) overflows from H'FF to H'00, OVFH (OVFL) is set to 1 in TCSRF. If OVIEH (OVIEL) in TCSRF is 1 at this time, IRRTFH (IRRTFL) is set to 1 in IRR2, and if IENTFH (IENTFL) in IENR2 is 1, an interrupt request is sent to the CPU.

Bit	Bit Name	Initial Value	R/W	Description
5	OVIEH	0	R/W	Timer Overflow Interrupt Enable H Selects enabling or disabling of interrupt generation when TCFH overflows. 0: TCFH overflow interrupt request is disabled 1: TCFH overflow interrupt request is enabled
4	CCLRH	0	R/W	Counter Clear H In 16-bit mode, this bit selects whether TCF is cleared when TCF and OCRF match. In 8-bit mode, this bit selects whether TCFH is cleared when TCFH and OCRFH match. In 16-bit mode: 0: TCF clearing by compare match is disabled 1: TCF clearing by compare match is enabled In 8-bit mode: 0: TCFH clearing by compare match is disabled 1: TCFH clearing by compare match is enabled
3	OVFL	0	R/W*	Timer Overflow Flag L This is a status flag indicating that TCFL has overflowed. [Setting condition] When TCFL overflows from H'FF to H'00 [Clearing condition] When this bit is written to 0 after reading OVFL = 1
2	CMFL	0	R/W*	Compare Match Flag L This is a status flag indicating that TCFL has matched OCRFL. [Setting condition] When the TCFL value matches the OCRFL value [Clearing condition] When this bit is written to 0 after reading CMFL = 1

12.8.3 Caution on Period Setting

When counter clearing on compare match is set, TCNT is cleared in the last state in which it matches the TGR value (the point at which the count value matched by TCNT is updated). Consequently, the actual counter frequency is given by the following formula:

$$f = \frac{\phi}{(N + 1)}$$

Where f: Counter frequency
ϕ: Operating frequency
N: TGR set value

12.8.4 Contention between TCNT Write and Clear Operation

If the counter clear signal is generated in the T2 state of a TCNT write cycle, TCNT clearing takes priority and the TCNT write is not performed.

Figure 12.31 shows the timing in this case.

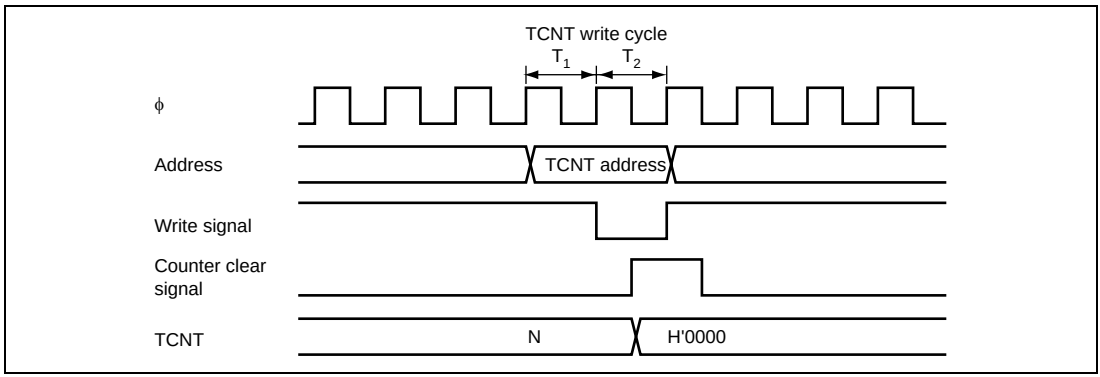
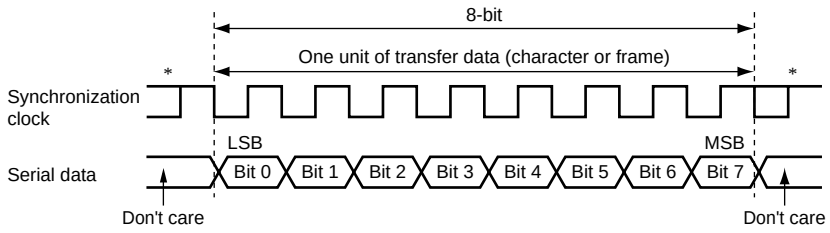


Figure 12.31 Contention between TCNT Write and Clear Operation

15.5 Operation in Clocked Synchronous Mode

Figure 15.9 shows the general format for clocked synchronous communication. In clocked synchronous mode, data is transmitted or received synchronous with clock pulses. A single character in the transmit data consists of the 8-bit data starting from the LSB. In clocked synchronous serial communication, data on the transmission line is output from one falling edge of the serial clock to the next. In clocked synchronous mode, the SCI3 receives data in synchronous with the rising edge of the serial clock. After 8-bit data is output, the transmission line holds the MSB state. In clocked synchronous mode, no parity or multiprocessor bit is added. Inside the SCI3, the transmitter and receiver are independent units, enabling full-duplex communication through the use of a common clock. Both the transmitter and the receiver also have a double-buffered structure, so data can be read or written during transmission or reception, enabling continuous data transfer.



Note: * High except in continuous transfer

Figure 15.9 Data Format in Clocked Synchronous Communication

15.5.1 Clock

Either an internal clock generated by the on-chip baud rate generator or an external synchronization clock input at the SCK31 (SCK32) pin can be selected, according to the setting of the COM bit in SMR and CKE0 and CKE1 bits in SCR. When the SCI3 is operated on an internal clock, the serial clock is output from the SCK31 (SCK32) pin. Eight serial clock pulses are output in the transfer of one character, and when no transfer is performed the clock is fixed high.

15.5.2 SCI3 Initialization

Before transmitting and receiving data, the SCI3 should be initialized as described in a sample flowchart in figure 15.4.

16.3.3 Transmit Data Register 4 (TDR4)

TDR4 is an 8-bit register that stores data for serial transmission. When the SCI4 detects that SR4 is empty, it transfers the transmit data written in TDR4 to SR4 and starts serial transmission. If the next transmit data is written to TDR4 while serial data in SR4 is being transmitted, continuous serial transmission is possible. TDR4 can be read from or written to by the CPU at any time. TDR4 is initialized to H'FF.

16.3.4 Receive Data Register 4 (RDR4)

RDR4 is an 8-bit register that stores receive data. When the SCI4 has received one byte of serial data, it transfers the received serial data from SR4 to RDR4, where it is stored. Then receive operation is completed. After this, SR4 is receive-enabled. RDR4 cannot be written to by the CPU. RDR4 is initialized to H'00.

16.3.5 Shift Register 4 (SR4)

SR4 is a register that receives or transmits serial data. SR4 cannot be directly read from or written to by the CPU.

Bit	Bit Name	Initial Value	R/W	Description
2	CTRM2	0	R/W	Variable Voltage Adjustment of 3-V Constant-Voltage Power Supply*
1	CTRM1	0	R/W	
0	CTRM0	0	R/W	The LCD drive power supply adjusted by the TRM bits can further be adjusted. If an LCD panel does not function normally due to a temperature in which LCD is used, set these bits to adjust it. 000: ±0 V 001: 0.09 V 010: 0.18 V 011: 0.27 V 100: -0.36 V 101: -0.27 V 110: -0.18 V 111: -0.09 V

Notes: Setting Method for LCD Trimming Register (LTRMR)
Assuming the following definitions,

V1 initial state voltage: A

LTRMR register TRM3 to TRM0: B

CTRM2 to CTRM0: C

rough guidelines for the voltages after trimming are as follows:

V1 voltage = A + B + C

V2 voltage = (A + B + C) × 2/3

V3 voltage = (A + B + C) / 3

After monitoring voltage A, set B and C so the V1 voltage is 3 V.

* These are approximate values and are not guaranteed. Therefore these values should be used as reference values.

Table 19.5 shows a output levels.

Table 19.5 Output Levels

	Data	0	0	1	1
	M	**0**	**1**	**0**	**1**
Static	Common output	V1	VSS	V1	VSS
	Segment output	V1	VSS	VSS	V1
1/2 duty	Common output	V2, V3	V2, V3	V1	VSS
	Segment output	V1	VSS	VSS	V1
1/3 duty	Common output	V3	V2	V1	VSS
	Segment output	V2	V3	VSS	V1
1/4 duty	Common output	V3	V2	V1	VSS
	Segment output	V2	V3	VSS	V1

M: LCD alternation signal

19.4.3 3-V Constant-Voltage Power Supply Circuit

This LSI incorporates a 3-V constant-voltage power supply circuit consisting of a band gap reference circuit (BGR), a triple step-up circuit, etc. This allows the 3 V constant voltage to drive LCD driver independently of Vcc.

Before activating a step-up circuit, LCD controller/driver operates and set the duty cycle, pin function of the LCD driver or I/O, display data, frame frequencies, etc. Insert a capacitance of 0.1 μF between the C1 pin and C2 pin, and connect a capacitance of 0.1 μF to each of V1, V2, and V3 pins. (See figure 19.9.)

After this setting, setting the BGRSTPN bit in the BGR control register (BGRMR) to 1 activates the band gap reference circuit, generating 1 V constant voltage (V_{LCD3}) at the V3 pin. Furthermore, selecting the step-up circuit clock of the LCD control register 2 (LCR2) and setting the SUPS bit to 1 activates the triple step-up circuit, generating 2 V constant voltage, twice V_{LCD3}, at the V2 pin, and generating 3 V constant voltage, triple V_{LCD3}, at the V1 pin.

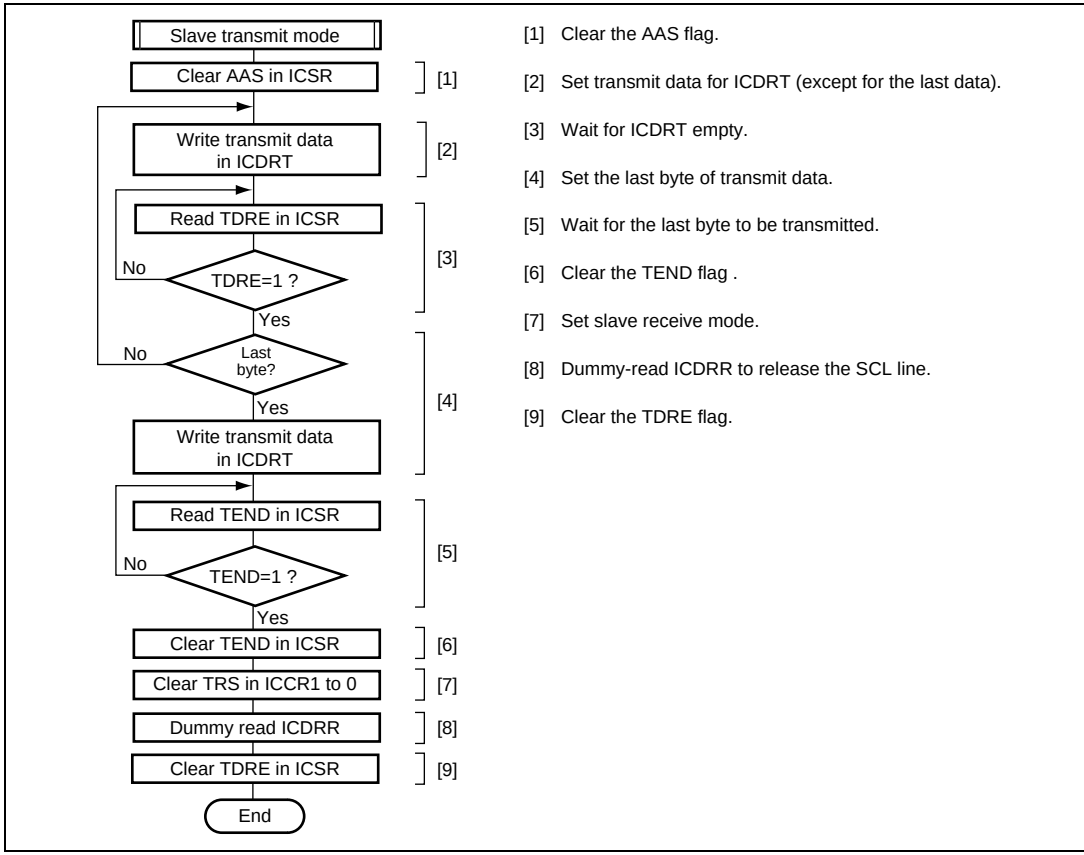


Figure 20.19 Sample Flowchart for Slave Transmit Mode

Instruction	Mnemonic	Instruction Fetch I	Branch Addr. Read J	Stack Operation K	Byte Data Access L	Word Data Access M	Internal Operation N
MULXS	MULXS.B Rs, Rd	2					12
	MULXS.W Rs, ERd	2					20
MULXU	MULXU.B Rs, Rd	1					12
	MULXU.W Rs, ERd	1					20
NEG	NEG.B Rd	1					
	NEG.W Rd	1					
	NEG.L ERd	1					
NOP	NOP	1					
NOT	NOT.B Rd	1					
	NOT.W Rd	1					
	NOT.L ERd	1					
OR	OR.B #xx:8, Rd	1					
	OR.B Rs, Rd	1					
	OR.W #xx:16, Rd	2					
	OR.W Rs, Rd	1					
	OR.L #xx:32, ERd	3					
	OR.L ERs, ERd	2					
ORC	ORC #xx:8, CCR	1					
POP	POP.W Rn	1				1	2
	POP.L ERn	2				2	2
PUSH	PUSH.W Rn	1				1	2
	PUSH.L ERn	2				2	2
ROTL	ROTL.B Rd	1					
	ROTL.W Rd	1					
	ROTL.L ERd	1					
ROTR	ROTR.B Rd	1					
	ROTR.W Rd	1					
	ROTR.L ERd	1					
ROTXL	ROTXL.B Rd	1					
	ROTXL.W Rd	1					
	ROTXL.L ERd	1					

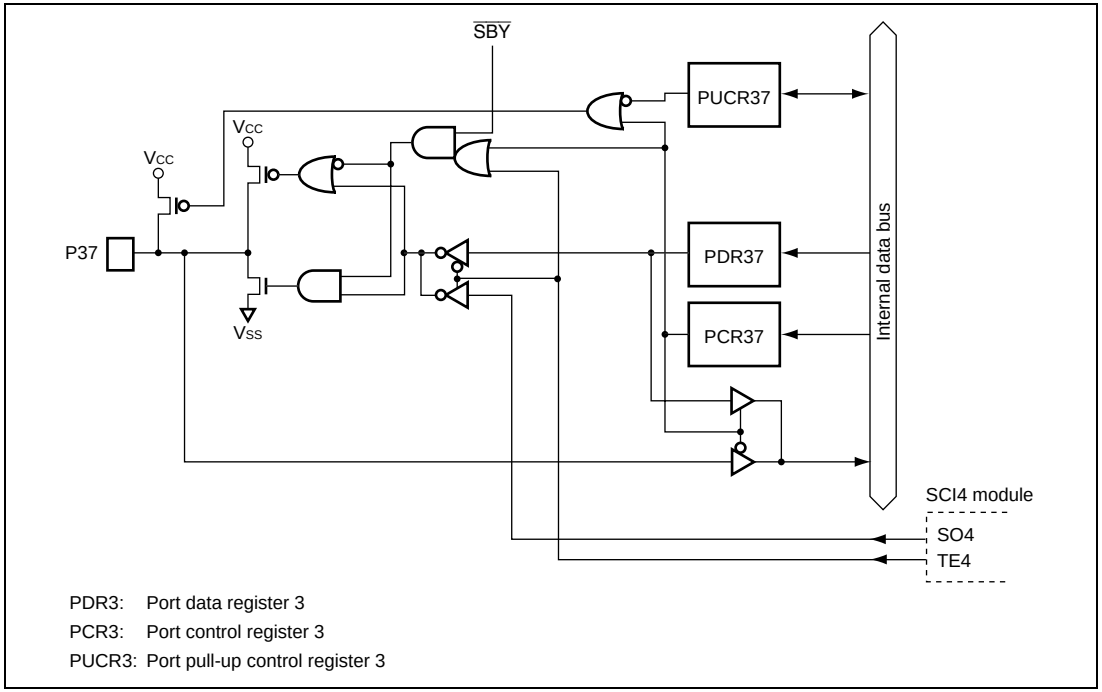


Figure B.2 (a) Port 3 Block Diagram (P37) (F-ZTAT Version)

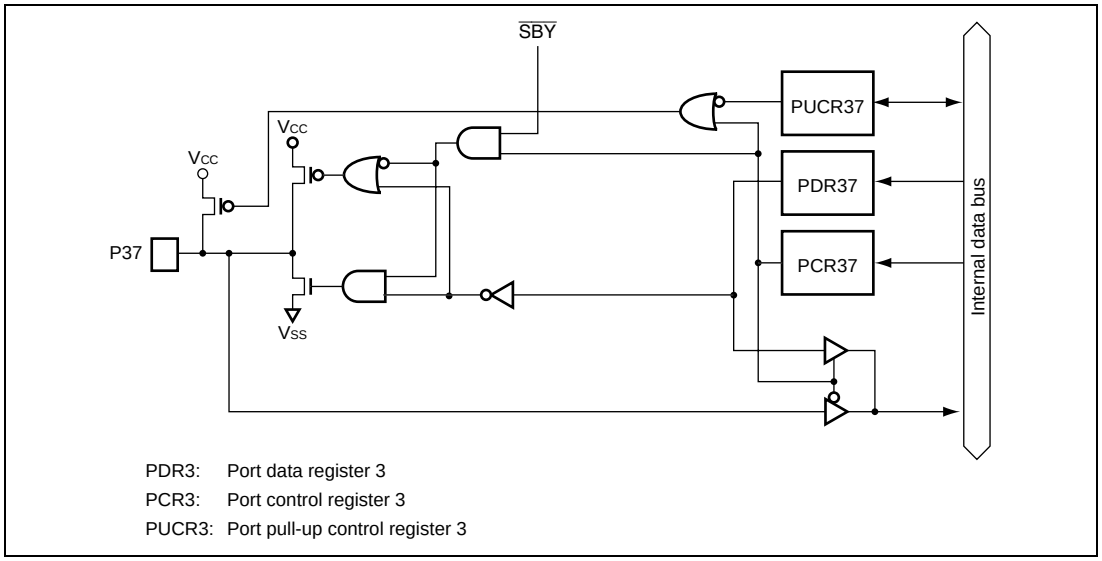


Figure B.2 (b) Port 3 Block Diagram (P37) (Masked ROM Version)