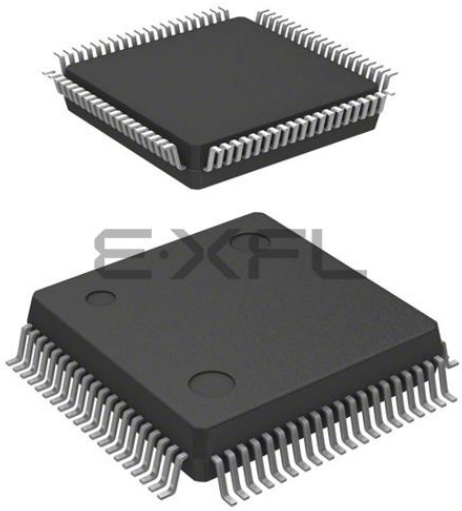

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Details	
Product Status	Active
Core Processor	H8/300H
Core Size	16-Bit
Speed	4MHz
Connectivity	I²C, IrDA, SCI
Peripherals	LCD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	52KB (52K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38076rh4v

Item	Page	Revision (See Manual for Details)
9.1.5 Pin Functions	162	Description amended

• P14/TIOCA2/TCLKC pin

Notes: 1. When the MD1 and MD0 bits are set to B'00 and the IOA3 bit to 1, the pin function becomes the TIOCA2 input pin.
Clear PCR14 to 0 when using TIOCA2 as an input pin.
2. When the TPSC2 to TPSC0 bits in TCR_2 are set to B'110, the pin function becomes the TCLKC input pin.
Clear PCR14 to 0 when using TCLKC as an input pin.

TPU Channel 2 Setting	(2)	(1)	(2)	(1)	(1)	(2)
MD1, MD0	B'00		B'1x	B'10	B'11	
IOA3 to IOA0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00	Other than B'xx00	
CCLR1, CCLR0	—	—	—	—	Other than B'01	B'01
Output Function	—	Output compare output	—	PWM mode 1* output	PWM mode 2 output	—

[Legend] x: Don't care.
Note: * The output of the TIOCB2 pin is disabled.

	163	• P13/TIOCB1/TCLKB pin

TPU Channel 1 Setting	Next table (1)	Next table (2)		Next table (3)	
PCR13	—	0	1	0	1
Pin Function	—	P13 input pin	P13 output pin	P13 input pin	P13 output pin
				TIOCB1 input pin	
		TCLKB input pin*			

Note: * When the TPSC2 to TPSC0 bits in TCR_1 or TCR_2 are set to B'101, the pin function becomes the TCLKB input pin.
Clear PCR13 to 0 when using TCLKB as an input pin.

TPU Channel 1 Setting	(2)	(3)	(1)	
MD1, MD0	B'00			B'10, B'01, B'11
IOB3 to IOB0	B'0000	B'1xxx	B'0001 to B'0111	B'xxxx
CCLR1, CCLR0	B'xx			
Output Function	—	Setting prohibited		

[Legend] x: Don't care.

	164	• P12/TIOCA1/TCLKA pin

Notes: 1. When the MD1 and MD0 bits are set to B'00 and the IOA3 bit to 1, the pin function becomes the TIOCA1 input pin.
Clear PCR12 to 0 when using TIOCA1 as an input pin.
2. When the TPSC2 to TPSC0 bits in TCR_1 or TCR_2 are set to B'100, the pin function becomes the TCLKA input pin.
Clear PCR12 to 0 when using TCLKA as an input pin.

Tables

13.3 Register Descriptions

The asynchronous event counter has the following registers.

- Event counter PWM compare register (ECPWCR)
- Event counter PWM data register (ECPWDR)
- Input pin edge select register (AEGSR)
- Event counter control register (ECCR)
- Event counter control/status register (ECCSR)
- Event counter H (ECH)
- Event counter L (ECL)

13.3.1 Event Counter PWM Compare Register (ECPWCR)

ECPWCR sets the one conversion period of the event counter PWM waveform.

Always read or write to this register in word size.

Bit	Bit Name	Initial Value	R/W	Description
15	ECPWCR15	1	R/W	One Conversion Period of Event Counter PWM Waveform When the ECPWME bit in AEGSR is 1, the event counter PWM is operating and therefore ECPWCR should not be modified. When changing the conversion period, the event counter PWM must be halted by clearing the ECPWME bit in AEGSR to 0 before modifying ECPWCR.
14	ECPWCR14	1	R/W	
13	ECPWCR13	1	R/W	
12	ECPWCR12	1	R/W	
11	ECPWCR11	1	R/W	
10	ECPWCR10	1	R/W	
9	ECPWCR9	1	R/W	
8	ECPWCR8	1	R/W	
7	ECPWCR7	1	R/W	
6	ECPWCR6	1	R/W	
5	ECPWCR5	1	R/W	
4	ECPWCR4	1	R/W	
3	ECPWCR3	1	R/W	
2	ECPWCR2	1	R/W	
1	ECPWCR1	1	R/W	
0	ECPWCR0	1	R/W	

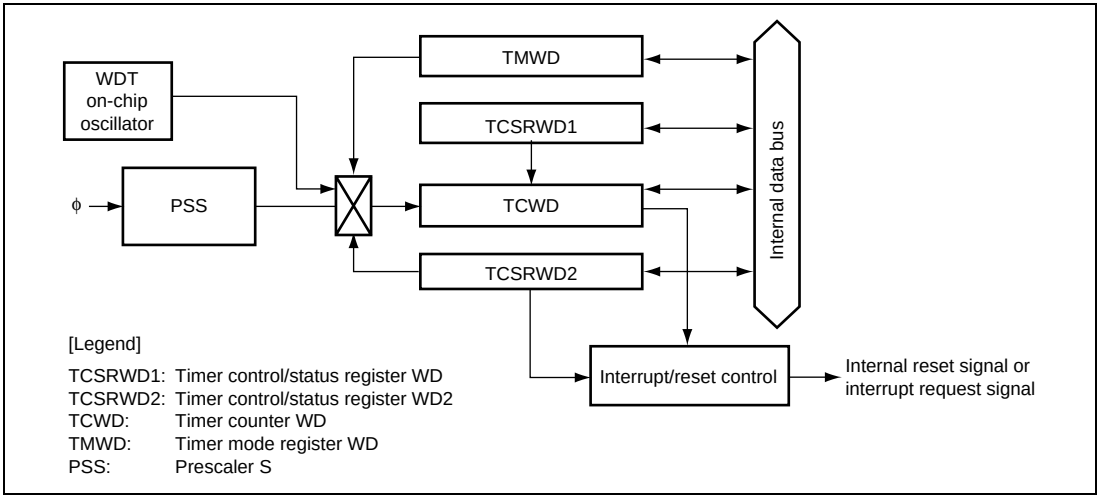

Figure 14.1 Block Diagram of Watchdog Timer

14.2 Register Descriptions

The watchdog timer has the following registers.

- Timer control/status register WD1 (TCSRWD1)
- Timer control/status register WD2 (TCSRWD2)
- Timer counter WD (TCWD)
- Timer mode register WD (TMWD)

14.2.2 Timer Control/Status Register WD2 (TCSRWD2)

TCSRWD2 performs the TCSRWD2 write control, mode switching, and interrupt control. TCSRWD2 must be rewritten by using the MOV instruction. The bit manipulation instruction cannot be used to change the setting value.

Bit	Bit Name	Initial Value	R/W	Description
7	OVF	0	R/(W)*[1]	Overflow Flag Indicates that TCWD has overflowed (changes from H'FF to H'00). [Setting condition] When TCWD overflows (changes from H'FF to H'00) When internal reset request generation is selected in watchdog timer mode, this bit is cleared automatically by the internal reset after it has been set. [Clearing condition] • When TCSRWD2 is read when OVF = 1, then 0 is written to OVF*[4]
6	B5WI	1	R/(W)*[2]	Bit 5 Write Inhibit The WT/IT bit can be written only when the write value of the B5WI bit is 0. This bit is always read as 1.
5	WT/IT	0	R/(W)*[3]	Timer Mode Select Selects whether the WDT is used as a watchdog timer or interval timer. 0: Watchdog timer mode 1: Interval timer mode
4	B3WI	1	R/(W)*[2]	Bit 3 Write Inhibit The IEOVF bit can be written only when the write value of the B3WI bit is 0. This bit is always read as 1.
3	IEOVF	0	R/(W)*[3]	Overflow Interrupt Enable Enables or disables an overflow interrupt request in interval timer mode. 0: Disables an overflow interrupt 1: Enables an overflow interrupt

9.7.3 Pin Functions

The relationship between the register settings and the port functions is shown below.

- P87/SEG32 to P84/SEG29 pins

  The pin function is switched as shown below according to the combination of the PCR8n bit in PCR8 and SGS3 to SGS0 bits in LPCR.

(n = 7 to 4)

SGS3 to SGS0	Other than B'1000, B'1001, B'1010, B'1011, B'1100, B'1101, B'1110, B'1111		B'1000, B'1001, B'1010, B'1011, B'1100, B'1101, B'1110, B'1111
PCR8n	0	1	x
Pin Function	P8n input pin	P8n output pin	SEGn+25 output pin

[Legend] x: Don't care.

- P83/SEG28 to P80/SEG25 pins

  The pin function is switched as shown below according to the combination of the PCR8m bit in PCR8 and SGS3 to SGS0 bits in LPCR.

(m = 3 to 0)

SGS3 to SGS0	Other than B'0111, B'1000, B'1001, B'1010, B'1011, B'1100, B'1101, B'1110		B'0111, B'1000, B'1001, B'1010, B'1011, B'1100, B'1101, B'1110
PCR8m	0	1	x
Pin Function	P8m input pin	P8m output pin	SEGm+25 output pin

[Legend] x: Don't care.

Table 12.6 MD3 to MD0

Bit 1 MD1	Bit 0 MD0	Description
0	0	Normal operation
	1	Reserved
1	0	PWM mode 1
	1	PWM mode 2

12.3.3 Timer I/O Control Register (TIOR)

TIOR controls TGR. The TPU has a total of two TIOR registers, one for each channel. Care is required as TIOR is affected by the TMDR setting.

The initial output specified by TIOR is valid when the counter is stopped (the CST bit in TSTR is cleared to 0). Note also that, in PWM mode 2, the output at the point at which the counter is cleared to 0 is specified.

- TIOR_1, TIOR_2

Bit	Bit Name	Initial Value	R/W	Description
7	IOB3	All 0	R/W	I/O Control B3 to B0
6	IOB2		R/W	Specify the function of TGRB.
5	IOB1		R/W	For details, refer to tables 12.7 and 12.8.
4	IOB0		R/W	
3	IOA3	All 0	R/W	I/O Control A3 to A0
2	IOA2		R/W	Specify the function of TGRA.
1	IOA1		R/W	For details, refer to tables 12.9 and 12.10.
0	IOA0		R/W	

Clocked synchronous mode

- Data length: 8 bits
- Receive error detection: Overrun errors detected

Table 15.1 SCI3 Channel Configuration

Channel	Abbreviation	Pin*[1]	Register*[2]	Register Address
Channel 1	SCI3_1	SCK31	SMR3_1	H'FF98
		RXD31	BRR3_1	H'FF99
		TXD31	SCR3_1	H'FF9A
			TDR3_1	H'FF9B
			SSR3_1	H'FF9C
			RDR3_1	H'FF9D
			RSR3_1	—
			TSR3_1	—
			IrCR	H'FFA7
Channel 2	SCI3_2	SCK32	SMR3_2	H'FFA8
		RXD32	BRR3_2	H'FFA9
		TXD32	SCR3_2	H'FFAA
			TDR3_2	H'FFAB
			SSR3_2	H'FFAC
			RDR3_2	H'FFAD
			RSR3_2	—
			TSR3_2	—

Notes: 1. Pin names SCK3, RXD3, and TXD3 are used in the text for all channels, omitting the channel designation.
2. In the text, channel description is omitted for registers and bits.