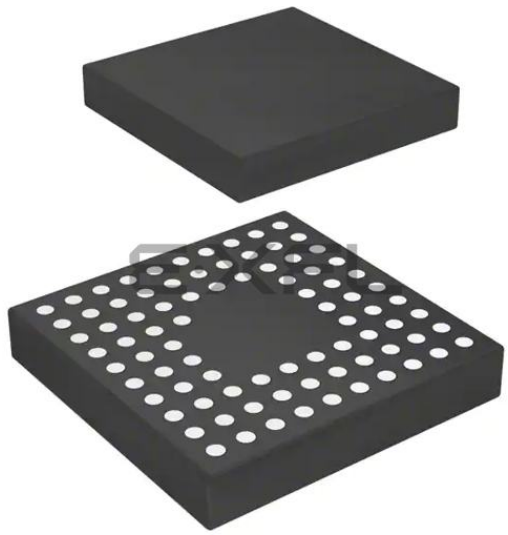

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8/300H
Core Size	16-Bit
Speed	10MHz
Connectivity	I²C, IrDA, SCI
Peripherals	LCD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	52KB (52K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	85-TFLGA
Supplier Device Package	85-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38076rlp10wv

User's Manual

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The revision list can be viewed directly by clicking the title page.

The revision list summarizes the locations of revisions and additions. Details should always be checked by referring to the relevant text.

H8/38076R Group

Hardware Manual

Renesas 16-Bit Single-Chip Microcomputer
H8 Family/H8/300H Super Low Power Series

H8/38076RF
H8/38076R
H8/38075R
H8/38074R
H8/38073R

Renesas Electronics
www.renesas.com

Rev.4.00 2006.08

Bit	Bit Name	Initial Value	R/W	Description
7	I	1	R/W	Interrupt Mask Bit Masks interrupts other than NMI when set to 1. NMI is accepted regardless of the I bit setting. The I bit is set to 1 at the start of an exception-handling sequence.
6	UI	Undefined	R/W	User Bit Can be written and read by software using the LDC, STC, ANDC, ORC, and XORC instructions.
5	H	Undefined	R/W	Half-Carry Flag When the ADD.B, ADDX.B, SUB.B, SUBX.B, CMP.B, or NEG.B instruction is executed, this flag is set to 1 if there is a carry or borrow at bit 3, and cleared to 0 otherwise. When the ADD.W, SUB.W, CMP.W, or NEG.W instruction is executed, the H flag is set to 1 if there is a carry or borrow at bit 11, and cleared to 0 otherwise. When the ADD.L, SUB.L, CMP.L, or NEG.L instruction is executed, the H flag is set to 1 if there is a carry or borrow at bit 27, and cleared to 0 otherwise.
4	U	Undefined	R/W	User Bit Can be written and read by software using the LDC, STC, ANDC, ORC, and XORC instructions.
3	N	Undefined	R/W	Negative Flag Stores the value of the most significant bit of data as a sign bit.
2	Z	Undefined	R/W	Zero Flag Set to 1 to indicate zero data, and cleared to 0 to indicate non-zero data.
1	V	Undefined	R/W	Overflow Flag Set to 1 when an arithmetic overflow occurs, and cleared to 0 at other times.
0	C	Undefined	R/W	Carry Flag Set to 1 when a carry occurs, and cleared to 0 otherwise. Used by: • Add instructions, to indicate a carry • Subtract instructions, to indicate a borrow • Shift and rotate instructions, to indicate a carry The carry flag is also used as a bit accumulator by bit manipulation instructions.

2.7 CPU States

There are four CPU states: the reset state, program execution state, program halt state, and exception-handling state. The program execution state includes active (high-speed or medium-speed) mode and subactive mode. For the program halt state, there are sleep (high-speed or medium-speed) mode, standby mode, watch mode, and subsleep mode. These states are shown in figure 2.11. Figure 2.12 shows the state transitions. For details on program execution state and program halt state, refer to section 6, Power-Down Modes. For details on exception handling, refer to section 3, Exception Handling.

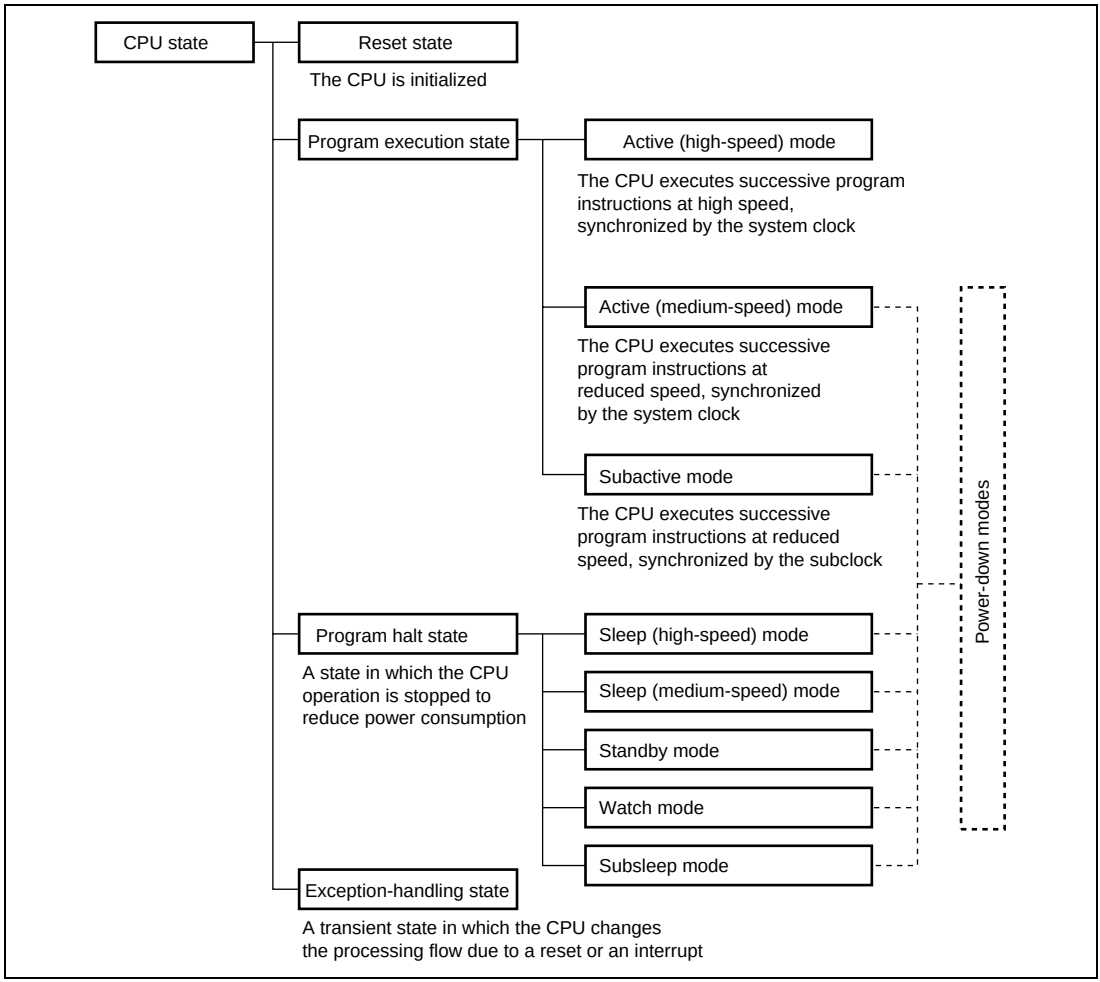

Figure 2.11 CPU Operating States

4.2 Input/Output Pins

Table 4.1 shows the pin configuration of the interrupt controller.

Table 4.1 Pin Configuration

Name	I/O	Function
$\overline{\text{NMI}}$	Input	Nonmaskable external interrupt pin Rising or falling edge can be selected
IRQAEC	Input	Maskable external interrupt pin Rising, falling, or both edges can be selected
$\overline{\text{IRQ4}}$	Input	Maskable external interrupt pins Rising or falling edge can be selected
$\overline{\text{IRQ3}}$	Input	
$\overline{\text{IRQ1}}$	Input	
$\overline{\text{IRQ0}}$	Input	
$\overline{\text{WKP7}}$ to $\overline{\text{WKP0}}$	Input	Maskable external interrupt pins Accepted at a rising or falling edge

4.3 Register Descriptions

The interrupt controller has the following registers.

- Interrupt edge select register (IEGR)
- Wakeup edge select register (WEGR)
- Interrupt enable register 1 (IENR1)
- Interrupt enable register 2 (IENR2)
- Interrupt request register 1 (IRR1)
- Interrupt request register 2 (IRR2)
- Wakeup interrupt request register (IWPR)
- Interrupt priority register A (IPRA)
- Interrupt priority register B (IPRB)
- Interrupt priority register C (IPRC)
- Interrupt priority register D (IPRD)
- Interrupt priority register E (IPRE)
- Interrupt mask register (INTM)

4.4.2 Internal Interrupts

Internal interrupts generated from the on-chip peripheral modules have the following features:

- For each on-chip peripheral module, there are flags that indicate the interrupt request status, and enable bits that select enabling or disabling of these interrupts. Internal interrupts can be controlled independently. If an enable bit is set to 1, an interrupt request is sent to the interrupt controller.
- The interrupt mask level can be set by IPR.

4.5 Interrupt Exception Handling Vector Table

Table 4.2 shows interrupt exception handling sources, vector addresses, and interrupt priorities. The lower the vector number, the higher the priority. The priority within a module is fixed. Mask levels for interrupts other than NMI and address break can be modified by IPR.

- PA2/COM3 pin

  The pin function depends on bit PCRA2 in PCRA and bits DTS1 and DTS0, bit CMX, and bits SGS3 to SGS0 in LPCR.

DTS1 to DTS0, CMX	x		Other than B'000, B'010	B'000, B'010	
SGS3 to SGS0	B'0000		Other than B'0000		
PCRA2	0	1	x	0	1
Pin Function	PA2 input pin*[1]	PA2 output pin*[1]	COM3 output pin	Leave open*[2]	Leave open*[2]

[Legend] x: Don't care.

Note: 1. The board power supply level is Vcc.
2. The board power supply level is the LCD drive power supply voltage level.

- PA1/COM2 pin

  The pin function depends on bit PCRA1 in PCRA and bits DTS1 and DTS0, bit CMX, and bits SGS3 to SGS0 in LPCR.

DTS1 to DTS0, CMX	x		Other than B'000	B'000	
SGS3 to SGS0	B'0000		Other than B'0000		
PCRA1	0	1	x	0	1
Pin Function	PA1 input pin*[1]	PA1 output pin*[1]	COM2 output pin	Leave open*[2]	Leave open*[2]

[Legend] x: Don't care.

Note: 1. The board power supply level is Vcc.
2. The board power supply level is the LCD drive power supply voltage level.

- PA0/COM1 pin

  The pin function depends on bit PCRA0 in PCRA and bits DTS1 and DTS0, bit CMX, and bits SGS3 to SGS0 in LPCR.

DTS1 to DTS0, CMX	x		
SGS3 to SGS0	B'0000		Other than B'0000
PCRA0	0	1	x
Pin Function	PA0 input pin	PA0 output pin	COM1 output pin

[Legend] x: Don't care.

9.10.3 Pin Functions

The relationship between the register settings and the port functions is shown below.

- PB7/AN7 pin

  The pin function is switched as shown below according to the CH3 to CH0 bits in AMR.

CH3 to CH0	Other than B'1011	B'1011
Pin Function	PB7 input pin	AN7 input pin

- PB6/AN6 pin

  The pin function is switched as shown below according to the CH3 to CH0 bits in AMR.

CH3 to CH0	Other than B'1010	B'1010
Pin Function	PB6 input pin	AN6 input pin

- PB5/AN5 pin

  The pin function is switched as shown below according to the CH3 to CH0 bits in AMR.

CH3 to CH0	Other than B'1001	B'1001
Pin Function	PB5 input pin	AN5 input pin

- PB4/AN4 pin

  The pin function is switched as shown below according to the CH3 to CH0 bits in AMR.

CH3 to CH0	Other than B'1000	B'1000
Pin Function	PB4 input pin	AN4 input pin

- PB3/AN3 pin

  The pin function is switched as shown below according to the CH3 to CH0 bits in AMR.

CH3 to CH0	Other than B'0111	B'0111
Pin Function	PB3 input pin	AN3 input pin

10.3.3 Hour Data Register (RHRDR)

RHRDR counts the BCD-coded hour value on the carry generated once per hour by RMINDR. The setting range is either decimal 00 to 11 or 00 to 23 by the selection of the 12/24 bit in RTCCR1.

Bit	Bit Name	Initial Value	R/W	Description
7	BSY	—	R	RTC Busy This bit is set to 1 when the RTC is updating (operating) the values of second, minute, hour, and day-of-week data registers. When this bit is 0, the values of second, minute, hour, and day-of-week data registers must be adopted.
6	—	0	—	Reserved This bit is always read as 0.
5	HR11	—	R/W	Counting Ten's Position of Hours
4	HR10	—	R/W	Counts on 0 to 2 for ten's position of hours.
3	HR03	—	R/W	Counting One's Position of Hours
2	HR02	—	R/W	Counts on 0 to 9 once per hour. When a carry is generated, 1 is added to the ten's position.
1	HR01	—	R/W	
0	HR00	—	R/W	

The term of validity of "Interrupt source generation signal"

= 1 cycle of ϕ_w + waiting time for completion of executing instruction
+ interrupt time synchronized with ϕ
= $1/\phi_w + ST \times (1/\phi) + (2/\phi)$ (second).....(1)

ST: Executing number of execution states

Method 1 is recommended to operate for time efficiency.

Method 1

1. Prohibit interrupt in interrupt handling routine (set IENFH, IENFL to 0).
2. After program process returned normal handling, clear interrupt request flags (IRRTFH, IRRTFL) after more than that calculated with (1) formula.
3. After reading the timer control status register F (TCSRF), clear the timer overflow flags (OVFH, OVFL) and compare match flags (CMFH, CMFL).
4. Enable interrupts (set IENFH, IENFL to 1).

Method 2

1. Set interrupt handling routine time to more than time that calculated with (1) formula.
2. Clear interrupt request flags (IRRTFH, IRRTFL) at the end of interrupt handling routine.
3. After read timer control status register F (TCSRF), clear timer overflow flags (OVFH, OVFL) and compare match flags (CMFH, CMFL).

All above attentions are also applied in 16-bit mode and 8-bit mode.

(3) Input Capture Signal Timing

Figure 12.24 shows input capture signal timing.

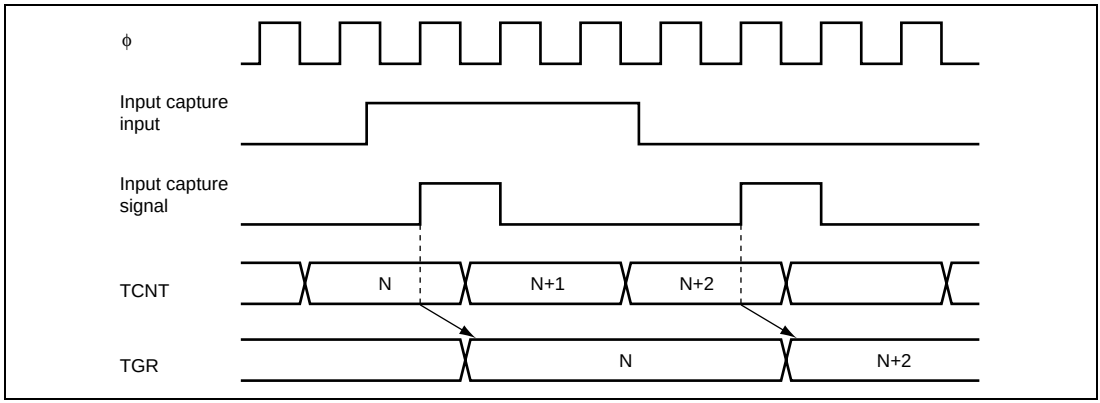

Figure 12.24 Input Capture Input Signal Timing

(4) Timing for Counter Clearing by Compare Match/Input Capture

Figure 12.25 shows the timing when counter clearing on compare match is specified, and figure 12.26 shows the timing when counter clearing on input capture is specified.

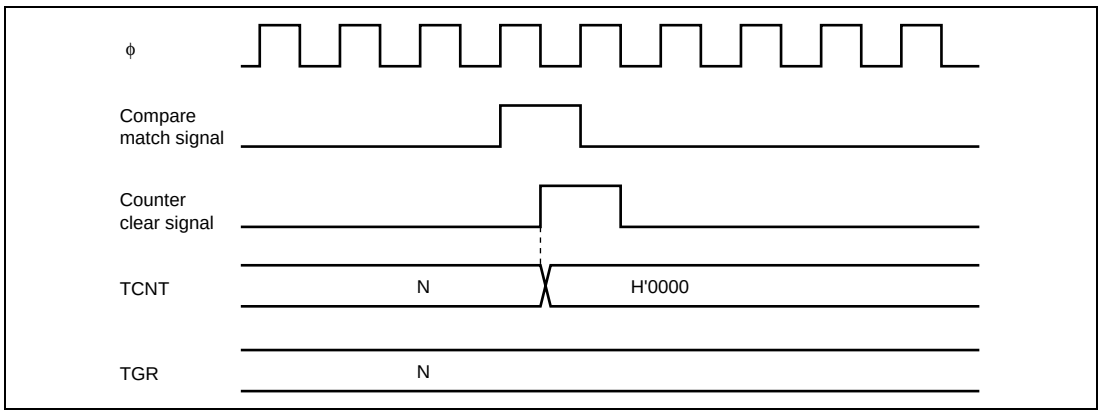

Figure 12.25 Counter Clear Timing (Compare Match)

12.8.6 Contention between TGR Write and Compare Match

If a compare match occurs in the T2 state of a TGR write cycle, the TGR write takes priority and the compare match signal is inhibited. A compare match does not occur even if the previous value is written.

Figure 12.33 shows the timing in this case.

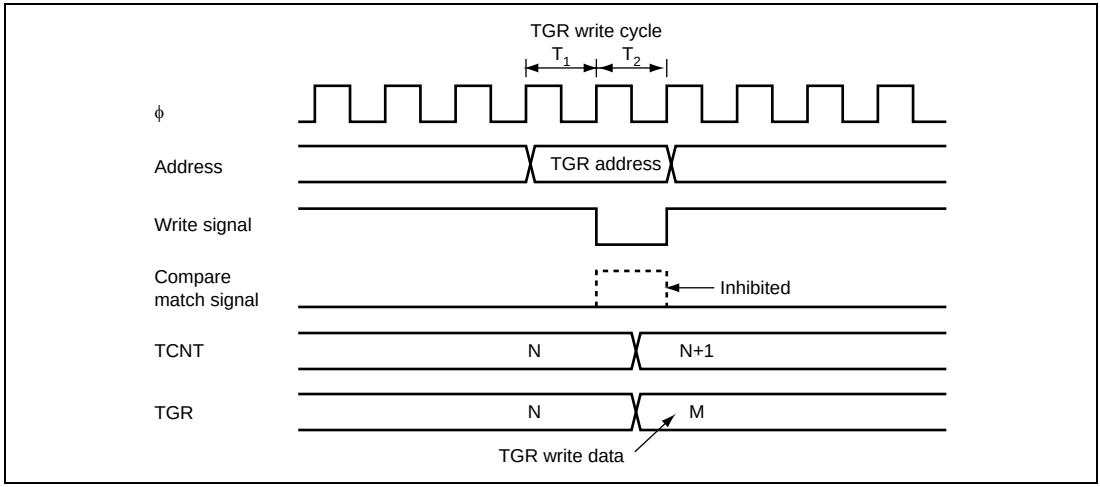

Figure 12.33 Contention between TGR Write and Compare Match

Table 15.3 Examples of BRR Settings for Various Bit Rates (Asynchronous Mode) (2)

	2.4576MHz			3MHz			3.6864MHz			4MHz		
Bit Rate (bit/s)	**n**	**N**	**Error (%)**	**n**	**N**	**Error (%)**	**n**	**N**	**Error (%)**	**n**	**N**	**Error (%)**
110	3	10	–0.83	2	52	0.50	2	64	0.70	2	70	0.03
150	3	7	0.00	2	38	0.16	3	11	0.00	2	51	0.16
200	3	5	0.00	2	28	1.02	3	8	0.00	2	38	0.16
250	2	18	1.05	2	22	1.90	2	28	–0.69	2	30	0.81
300	3	3	0.00	3	4	–2.34	3	5	0.00	2	25	0.16
600	3	1	0.00	0	155	0.16	3	2	0.00	0	207	0.16
1200	3	0	0.00	0	77	0.16	2	5	0.00	0	103	0.16
2400	2	1	0.00	0	38	0.16	2	2	0.00	0	51	0.16
4800	2	0	0.00	0	19	–2.34	0	23	0.00	0	25	0.16
9600	0	7	0.00	0	9	–2.34	0	11	0.00	0	12	0.16
19200	0	3	0.00	0	4	–2.34	0	5	0.00	—	—	—
31250	—	—	—	0	2	0.00	—	—	—	0	3	0.00
38400	0	1	0.00	—	—	—	0	2	0.00	—	—	—

15.5.5 Simultaneous Serial Data Transmission and Reception

Figure 15.14 shows a sample flowchart for simultaneous serial transmit and receive operations. The following procedure should be used for simultaneous serial data transmit and receive operations. To switch from transmit mode to simultaneous transmit and receive mode, after checking that the SCI3 has finished transmission and the TDRE and TEND flags are set to 1, clear TE to 0. Then simultaneously set TE and RE to 1 with a single instruction. To switch from receive mode to simultaneous transmit and receive mode, after checking that the SCI3 has finished reception, clear RE to 0. Then after checking that the RDRF and receive error flags (OER, FER, and PER) are cleared to 0, simultaneously set TE and RE to 1 with a single instruction.

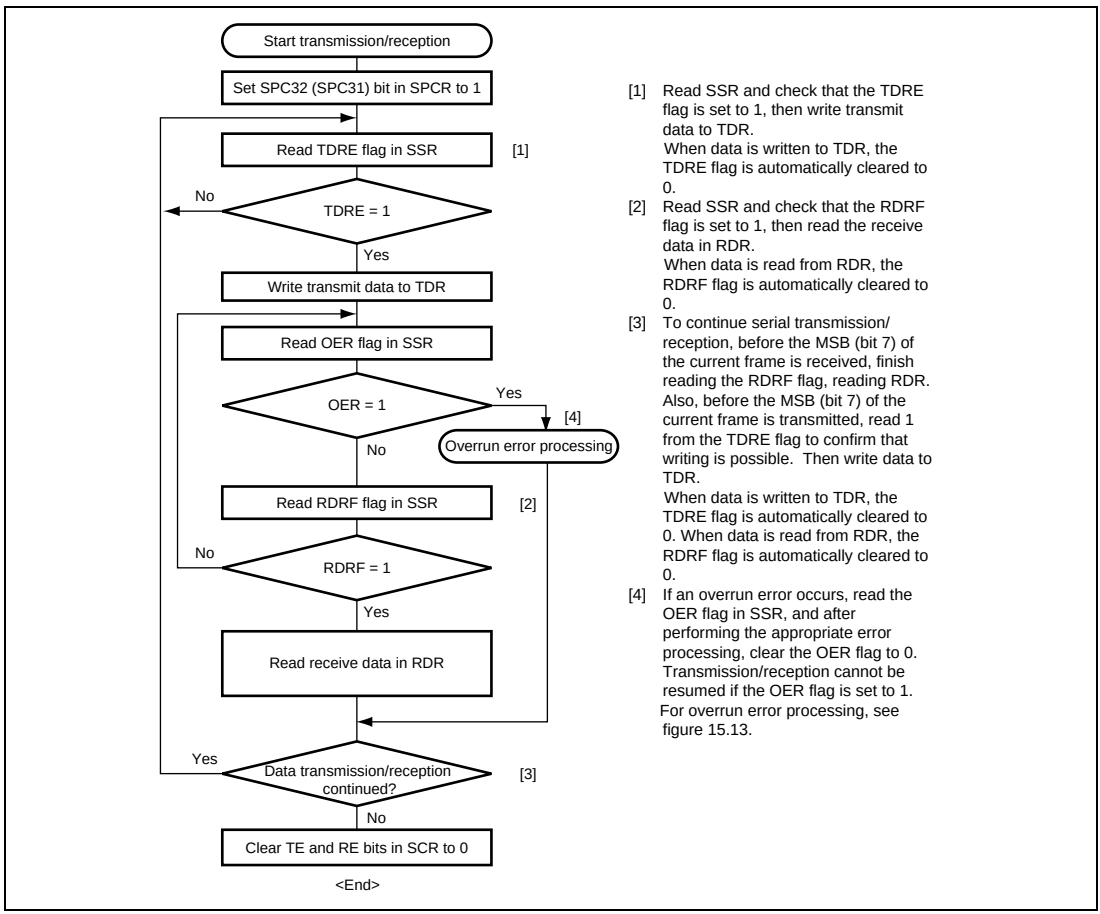

Figure 15.14 Sample Flowchart of Simultaneous Serial Transmit and Receive Operations (Clocked Synchronous Mode)

Section 16 Serial Communication Interface 4 (SCI4)

The serial communication interface 4 (SCI4) can handle clocked synchronous serial communication with the 8-bit buffer. The SCI4 is supported only by the F-ZTAT version. When the on-chip emulator debugger etc. is used, the SCK4, SI4, and SO4 pins in SCI4 are used by the system. Therefore the SCI4 is not available for the user.

16.1 Features

- Eight internal clocks (ϕ/1024, ϕ/256, ϕ/64, ϕ/32, ϕ/16, ϕ/8, ϕ/4, ϕ/2) or external clock can be selected as a clock source.
- Receive error detection: Overrun errors detected
- Four interrupt sources
  Transmit-end, transmit-data-empty, receive-data-full, and overrun error
- Full-duplex communication capability
  Buffering is used in both the transmitter and the receiver, enabling continuous transmission and continuous reception of serial data.
- When the on-chip emulator debugger etc. is not used, the SCI4 is available for the user.
- Use of module standby mode enables this module to be placed in standby mode independently when not used. (For details, refer to section 6.4, Module Standby Function.)

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name
TCNT_2	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	TPU_2
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
TGRA_2	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
TGRB_2	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
RTCFLG	FOIFG	WKIFG	DYIFG	HRIFG	MNIFG	SEIFG	05SEIFG	025SEIFG	RTC
RSECDR	BSY	SC12	SC11	SC10	SC03	SC02	SC01	SC00	
RMINDR	BSY	MN12	MN11	MN10	MN03	MN02	MN01	MN00	
RHRDR	BSY	—	HR11	HR10	HR03	HR02	HR01	HR00	
RWKDR	BSY	—	—	—	—	WK2	WK1	WK0	
RTCCR1	RUN	12/24	PM	RST	—	—	—	—	
RTCCR2	FOIE	WKIE	DYIE	HRIE	MNIE	1SEIE	05SEIE	025SEIE	
SUB32CR	32KSTOP	—	—	—	—	—	—	—	Clock pulse generator
RTCCSR	—	RCS6	RCS5	SUB32K	RCS3	RCS2	RCS1	RCS0	RTC
ICCR1	ICE	RCVD	MST	TRS	CKS3	CKS2	CKS1	CKS0	IIC2
ICCR2	BBSY	SCP	SDAO	SDAOP	SCLO	—	IICRST	—	
ICMR	MLS	WAIT	—	—	BCWP	BC2	BC1	BC0	
ICIER	TIE	TEIE	RIE	NAKIE	STIE	ACKE	ACKBR	ACKBT	
ICSR	TDRE	TEND	RDRF	NACKF	STOP	AL/OVE	AAS	ADZ	
SAR	SVA6	SVA5	SVA4	SVA3	SVA2	SVA1	SVA0	FS	
ICDRT	ICDRT7	ICDRT6	ICDRT5	ICDRT4	ICDRT3	ICDRT2	ICDRT1	ICDRT0	
ICDRR	ICDRR7	ICDRR6	ICDRR5	ICDRR4	ICDRR3	ICDRR2	ICDRR1	ICDRR0	
IPRA	IPRA7	IPRA6	IPRA5	IPRA4	IPRA3	IPRA2	IPRA1	IPRA0	Interrupts
IPRB	IPRB7	IPRB6	IPRB5	IPRB4	IPRB3	IPRB2	IPRB1	IPRB0	
IPRC	IPRC7	IPRC6	IPRC5	IPRC4	IPRC3	IPRC2	IPRC1	IPRC0	
IPRD	IPRD7	IPRD6	IPRD5	IPRD4	IPRD3	IPRD2	IPRD1	IPRD0	
IPRE	IPRE7	IPRE6	IPRE5	IPRE4	—	—	—	—	

24.2.8 Flash Memory Characteristics —Preliminary—

Table 24.10 lists the flash memory characteristics.

Table 24.10 Flash Memory Characteristics

Condition A:

AV_{CC} = 2.7 V to 3.6 V, DV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, V_{CC} = 2.7 V to 3.6 V (operating voltage range in reading), V_{CC} = 3.0 V to 3.6 V (operating voltage range in programming/erasing), Ta = –20 to +75°C (operating temperature range in programming/erasing: regular specifications, wide-range specifications, products shipped as chips)

Condition B:

AV_{CC} = 1.8 V to 3.6 V, DV_{CC} = 2.2 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, V_{CC} = 1.8 V to 3.6 V (operating voltage range in reading), V_{CC} = 3.0 V to 3.6 V (operating voltage range in programming/erasing), Ta = –20 to +50°C (operating temperature range in programming/erasing: regular specifications, wide-range specifications)

			Test	Values			
Item		**Symbol**	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Programming time (per 128 bytes)*1*2*4		t_P		—	7	200	ms
Erase time (per block)*1*3*6		t_E		—	100	1200	ms
Maximum number of reprogrammings		N_{WEC}		1000*8*11	10000*9	—	Times
				100*8*12	10000*9	—	
Data retention time		t_{DRP}		10*10	—	—	Years
Programming	Wait time after SWE bit setting*1	x		1	—	—	µs
	Wait time after PSU bit setting*1	y		50	—	—	µs
	Wait time after P bit setting*1*4	z1	1 ≤ n ≤ 6	28	30	32	µs
		z2	7 ≤ n ≤ 1000	198	200	202	µs
		z3	Additional-programming	8	10	12	µs
	Wait time after P bit clear*1	α		5	—	—	µs
	Wait time after PSU bit clear*1	β		5	—	—	µs
	Wait time after PV bit setting*1	γ		4	—	—	µs
	Wait time after dummy write*1	ε		2	—	—	µs
	Wait time after PV bit clear*1	η		2	—	—	µs
	Wait time after SWE bit clear*1	θ		100	—	—	µs
	Maximum programming count*1*4*5	N		—	—	1000	Times

Table A.3 Number of Cycles in Each Instruction

Execution Status (Instruction Cycle)		Access Location	
		On-Chip Memory	On-Chip Peripheral Module
Instruction fetch	S_I	2	—
Branch address read	S_J		
Stack operation	S_K		
Byte data access	S_L		2 or 3*
Word data access	S_M		—
Internal operation	S_N	1	

Note: * Depends on which on-chip peripheral module is accessed. See section 23.1, Register Addresses (Address Order).

Table A.4 Number of Cycles in Each Instruction

Instruction	Mnemonic	Instruction Fetch I	Branch Addr. Read J	Stack Operation K	Byte Data Access L	Word Data Access M	Internal Operation N
ADD	ADD.B #xx:8, Rd	1					
	ADD.B Rs, Rd	1					
	ADD.W #xx:16, Rd	2					
	ADD.W Rs, Rd	1					
	ADD.L #xx:32, ERd	3					
	ADD.L ERs, ERd	1					
ADDS	ADDS #1/2/4, ERd	1					
ADDX	ADDX #xx:8, Rd	1					
	ADDX Rs, Rd	1					
AND	AND.B #xx:8, Rd	1					
	AND.B Rs, Rd	1					
	AND.W #xx:16, Rd	2					
	AND.W Rs, Rd	1					
	AND.L #xx:32, ERd	3					
	AND.L ERs, ERd	2					
ANDC	ANDC #xx:8, CCR	1					
BAND	BAND #xx:3, Rd	1					
	BAND #xx:3, @ERd	2			1		
	BAND #xx:3, @aa:8	2			1		
Bcc	BRA d:8 (BT d:8)	2					
	BRN d:8 (BF d:8)	2					
	BHI d:8	2					
	BLS d:8	2					
	BCC d:8 (BHS d:8)	2					
	BCS d:8 (BLO d:8)	2					
	BNE d:8	2					
	BEQ d:8	2					
	BVC d:8	2					
	BVS d:8	2					
	BPL d:8	2					
	BMI d:8	2					
	BGE d:8	2					

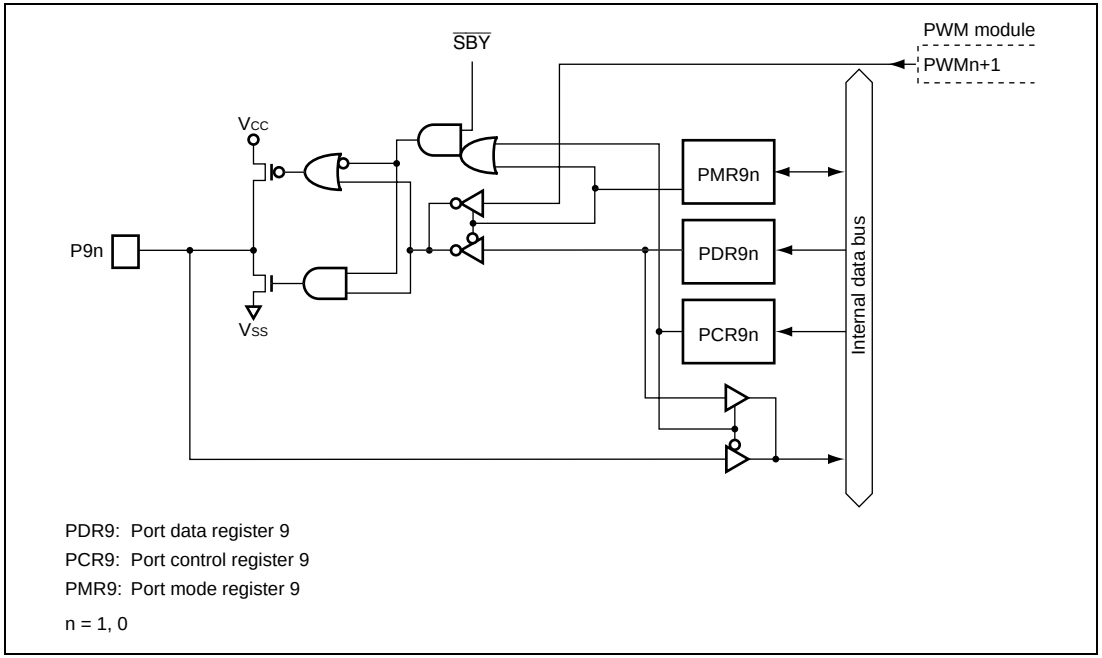

Figure B.8 (c) Port 9 Block Diagram (P91, P90)

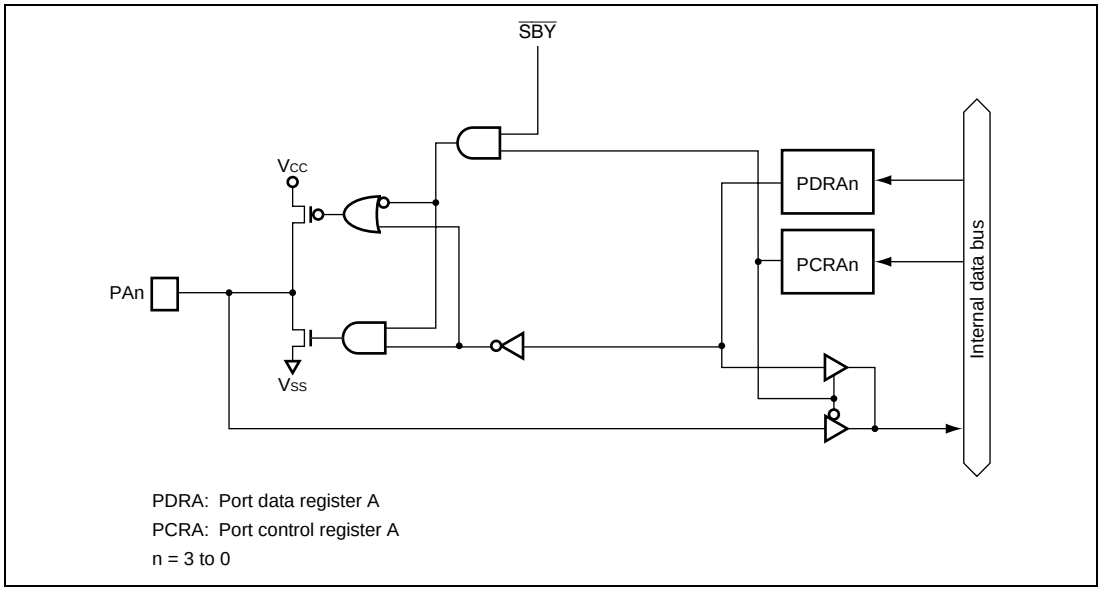

Figure B.9 Port A Block Diagram