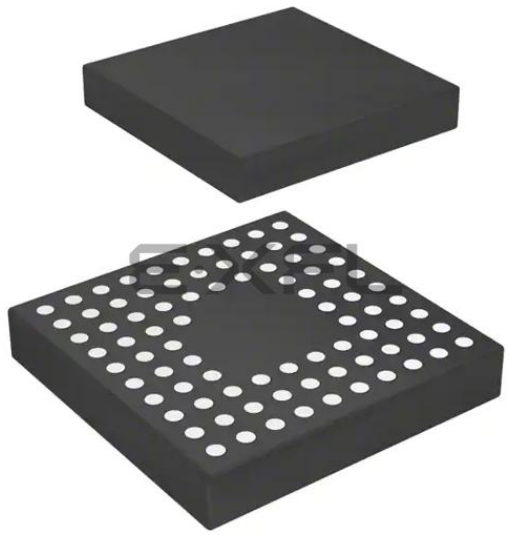

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Details	
Product Status	Active
Core Processor	H8/300H
Core Size	16-Bit
Speed	4MHz
Connectivity	I²C, IrDA, SCI
Peripherals	LCD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	52KB (52K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	85-TFLGA
Supplier Device Package	85-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38076rlp4v

Item	Page	Revision (See Manual for Details)
6.2 Mode Transitions and States of LSI Figure 6.1 Mode Transition Diagram	116	Note amended A transition between different modes cannot be made to occur simply because an interrupt request is generated. Make sure to enable interrupt requests.
Table 6.2 Transition Mode after SLEEP Instruction Execution and Interrupt Handling	118	Table amended

State Before Transition	LSON	MSON	SSBY	TMA3	DTON	Transition Mode after SLEEP Instruction Execution	Transition Mode due to Interrupt	Symbol in Figure 6.1
Active (medium-speed) mode	0	0	0	*	1	Active (high-speed) mode (direct transition)	—	f
	0	1	0	*	1	Active (medium-speed) mode (direct transition)	—	—

Table 6.3 Internal State in Each Operating Mode	120	Note amended

Function		Watch Mode	Subactive Mode	Subsleep Mode	Standby Mode
Peripheral modules	RTC	Functioning/ retained*9	Functioning/ retained*9	Functioning/ retained*9	Functioning/ retained*9
	Asynchronous event counter	Functioning*6	Functioning	Functioning	Functioning*6
	Timer F	Functioning/ retained*7	Functioning/retained*7	Functioning/ retained*7	Retained
	TPU	Retained	Retained	Retained	Retained
	WDT	Functioning*8/ retained	Functioning*8/ retained	Functioning*8/ retained	Functioning*8/ retained
	SCI3/IrDA	Reset	Functioning/ retained*2	Functioning/ retained*2	Reset

Notes:

6. Only incrementing of the external event timer by ECL/ECH and overflow interrupts operate.

7. Functioning if $\phi w/4$ is selected as an internal clock. Halted and retained otherwise.

8. Functioning if the on-chip oscillator is selected.

9. Functioning if the internal time keeping time-base function is selected and retained if the interval timer is selected.

Item	Page	Revision (See Manual for Details)
15.3.8 Bit Rate Register (BRR) Table 15.3 Examples of BRR Settings for Various Bit Rates (Asynchronous Mode) (3)	322	Table amended

	4.9152MHz			5MHz			6MHz			6.144MHz		
Bit Rate (bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	86	0.31	2	88	–0.25	2	106	–0.44	2	108	0.08
150	3	15	0.00	2	64	0.16	2	77	0.16	3	19	0.00
200	3	11	0.00	2	48	–0.35	2	58	–0.69	3	14	0.00
250	2	37	1.05	2	38	0.16	2	46	–0.27	3	11	0.00
300	3	7	0.00	2	32	–1.36	2	38	0.16	3	9	0.00
600	3	3	0.00	0	255	1.73	3	4	–2.34	3	4	0.00
1200	3	1	0.00	0	129	0.16	0	155	0.16	2	9	0.00

Table 15.5 Maximum Bit Rate for Each Frequency (Asynchronous Mode)	324	Table amended

		Setting	
OSC (MHz)	Maximum Bit Rate (bit/s)	n	N
0.0328	512.5	0	0
0.0384	600	0	0
2	62500	0	0

Table 15.6 BRR Settings for Various Bit Rates (Clocked Synchronous Mode) (1)	325	Table amended

ϕ	32.8 kHz			38.4 kHz			2 MHz		
Bit Rate (bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
200	0	20	–2.38	0	23	0.00	2	155	0.16
250	0	15	2.50	0	18	1.05	2	124	0.00
300	0	13	–2.38	0	15	0.00	2	103	0.16
500	0	7	2.50	—	—	—	2	62	–0.79
1k	0	3	2.50	—	—	—	2	30	0.81

Table 15.6 BRR Settings for Various Bit Rates (Clocked Synchronous Mode) (2)	326	Table and note amended

ϕ	4 MHz			8 MHz			10 MHz		
Bit Rate (bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
10k	0	99	0.00	0	199	0.00	2	15	–2.34

Note: * Continuous transmission/reception is not possible.

The value set in BRR is given by the following formula:

Active (medium-speed/high-speed) or sleep (medium-speed/high-speed)

$$N = \frac{OSC}{4 \times 2^{2n} \times B} - 1$$

Subactive or subsleep

$$N = \frac{OSC}{8 \times 2^{2n} \times B} - 1$$

B: Bit rate (bit/s)

N: BRR setting for baud rate generator ($0 \le N \le 255$)

OSC: ϕ_{osc} value (Hz)

n: Baud rate generator input clock number (n = 0, 2, or 3)
(The relation between n and the clock is shown in table 15.7.)

Table 2.4 Logic Operations Instructions

Instruction	Size*	Function
AND	B/W/L	Rd ∧ Rs → Rd, Rd ∧ #IMM → Rd Performs a logical AND operation on a general register and another general register or immediate data.
OR	B/W/L	Rd ∨ Rs → Rd, Rd ∨ #IMM → Rd Performs a logical OR operation on a general register and another general register or immediate data.
XOR	B/W/L	Rd ⊕ Rs → Rd, Rd ⊕ #IMM → Rd Performs a logical exclusive OR operation on a general register and another general register or immediate data.
NOT	B/W/L	¬ (Rd) → (Rd) Takes the one's complement (logical complement) of general register contents.

Note: * Refers to the operand size.
B: Byte
W: Word
L: Longword

Table 2.5 Shift Instructions

Instruction	Size*	Function
SHAL SHAR	B/W/L	Rd (shift) → Rd Performs an arithmetic shift on general register contents.
SHLL SHLR	B/W/L	Rd (shift) → Rd Performs a logical shift on general register contents.
ROTL ROTR	B/W/L	Rd (rotate) → Rd Rotates general register contents.
ROTXL ROTXR	B/W/L	Rd (rotate) → Rd Rotates general register contents through the carry flag.

Note: * Refers to the operand size.
B: Byte
W: Word
L: Longword

4.6.2 Interrupt Response Times

Table 4.4 shows interrupt response times – the interval between generation of an interrupt request and execution of the first instruction in the interrupt handling routine.

Table 4.4 Interrupt Response Times (States)

No.	Execution Status	Number of States
1	Interrupt mask level determination	1 or 2*[1]
2	Maximum number of wait states until executing instruction ends	1 to 23
3	PC, CCR stack	4
4	Vector fetch	4
5	Instruction fetch*[2]	4
6	Internal processing*[3]	4
	Total	19 to 41

Notes: 1. One state for internal interrupts and two states for external interrupts.
2. Prefetch after interrupt acceptance and interrupt handling routine prefetch.
3. Internal processing after interrupt acceptance and internal processing after vector fetch.

(2) TCFL, OCRFL

In toggle output, TMOFL pin output is toggled when a compare match occurs. If a TCRF write by a MOV instruction and generation of the compare match signal occur simultaneously, TOLL data is output to the TMOFL pin as a result of the TCRF write.

If an OCRFL write and compare match signal generation occur simultaneously, the compare match signal is invalid. However, a compare match signal may or may not be generated when the written data and the counter value match. As the compare match signal is output in synchronization with the TCFL clock, a compare match will not result in compare match signal generation if the clock is stopped.

If a TCFL write and overflow signal output occur simultaneously, the overflow signal is not output.

11.6.3 Flag Clearing

When $\phi_w/4$ is selected as the internal clock, "Interrupt source generation signal" will be operated with ϕ_w and the signal will be outputted with ϕ_w width. And, "Overflow signal" and "Compare match signal" are controlled with 2 cycles of ϕ_w signals. Those signals are output with 2-cycle width of ϕ_w (figure 11.3)

In active (high-speed, medium-speed) mode, even if you cleared interrupt request flag during the term of validity of "Interrupt source generation signal", same interrupt request flag is set. (1 in figure 11.3) And, the timer overflow flag and compare match flag cannot be cleared during the term of validity of "Overflow signal" and "Compare match signal".

For interrupt request flag is set right after interrupt request is cleared, interrupt process to one time timer FH, timer FL interrupt might be repeated. (2 in figure 11.3) Therefore, to definitely clear interrupt request flag in active (high-speed, medium-speed) mode, clear should be processed after the time that calculated with below (1) formula. And, to definitely clear timer overflow flag and compare match flag, clear should be processed after read timer control status register F (TCSRF) after the time that calculated with below (1) formula.

For ST of (1) formula, please substitute the longest number of execution states in used instruction.

In subactive mode, there are not limitation for interrupt request flag, timer overflow flag, and compare match flag clear.

12.3 Register Descriptions

The TPU has the following registers for each channel.

Channel 1:

- Timer control register_1 (TCR_1)
- Timer mode register_1 (TMDR_1)
- Timer I/O control register_1 (TIOR_1)
- Timer interrupt enable register_1 (TIER_1)
- Timer status register_1 (TSR_1)
- Timer counter_1 (TCNT_1)
- Timer general register A_1 (TGRA_1)
- Timer general register B_1 (TGRB_1)

Channel 2:

- Timer control register_2 (TCR_2)
- Timer mode register_2 (TMDR_2)
- Timer I/O control register_2 (TIOR_2)
- Timer interrupt enable register_2 (TIER_2)
- Timer status register_2 (TSR_2)
- Timer counter_2 (TCNT_2)
- Timer general register A_2 (TGRA_2)
- Timer general register B_2 (TGRB_2)

Common:

- Timer start register (TSTR)
- Timer synchro register (TSYR)

12.8.7 Contention between TGR Read and Input Capture

If an input capture signal is generated in the T1 state of a TGR read cycle, data that is read will be data after input capture transfer.

Figure 12.34 shows the timing in this case.

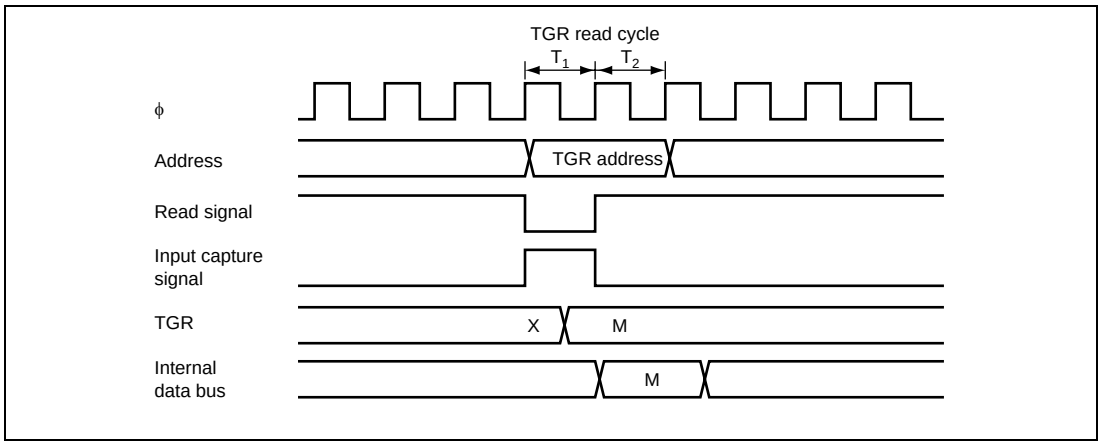


Figure 12.34 Contention between TGR Read and Input Capture

15.2 Input/Output Pins

Table 15.2 shows the SCI3 pin configuration.

Table 15.2 Pin Configuration

Pin Name	Abbreviation	I/O	Function
SCI3 clock	SCK31, SCK32	I/O	SCI3 clock input/output
SCI3 receive data input	RXD31, RXD32	Input	SCI3 receive data input
SCI3 transmit data output	TXD31, TXD32	Output	SCI3 transmit data output

15.3 Register Descriptions

The SCI3 has the following registers for each channel.

- Receive shift register 3 (RSR3)*
- Receive data register 3 (RDR3)*
- Transmit shift register 3 (TSR3)*
- Transmit data register 3 (TDR3)*
- Serial mode register 3 (SMR3)*
- Serial control register 3 (SCR3)*
- Serial status register 3 (SSR3)*
- Bit rate register 3 (BRR3)*
- Serial port control register (SPCR)
- IrDA control register (IrCR)

Note: * These register names are abbreviated to RSR, RDR, TSR, TDR, SMR, SCR, SSR, and BRR in the text.

15.3.6 Serial Control Register (SCR)

SCR enables or disables SCI3 transfer operations and interrupt requests, and selects the transfer clock source. For details on interrupt requests, refer to section 15.8, Interrupt Requests.

SCR is initialized to H'00 by a reset or in standby mode, watch mode, or module standby mode.

Bit	Bit Name	Initial Value	R/W	Description
7	TIE	0	R/W	Transmit Interrupt Enable When this bit is set to 1, the TXI (TXI32) interrupt request is enabled. TXI (TXI32) can be released by clearing the TDRE it or TI bit to 0.
6	RIE	0	R/W	Receive Interrupt Enable When this bit is set to 1, RXI and ERI interrupt requests are enabled. RXI (RXI32) and ERI (ERI32) can be released by clearing the RDRF bit or the FER, PER, or OER error flag to 0, or by clearing the RIE bit to 0.
5	TE	0	R/W	Transmit Enable When this bit is set to 1, transmission is enabled. When this bit is 0, the TDRE bit in SSR is fixed at 1. When transmit data is written to TDR while this bit is 1, Bit TDRE in SSR is cleared to 0 and serial data tansmission is started. Be sure to carry out SMR settings, and setting of bit SPC31 or SPC32 in SPCR, to decide the transmission format before setting bit TE to 1.
4	RE	0	R/W	Receive Enable When this bit is set to 1, reception is enabled. In this state, serial data reception is started when a start bit is detected in asynchronous mode or serial clock input is detected in clocked synchronous mode. Be sure to carry out the SMR settings to decide the reception format before setting bit RE to 1. Note that the RDRF, FER, PER, and OER flags in SSR are not affected when bit RE is cleared to 0, and retain their previous state

15.5.3 Serial Data Transmission

Figure 15.10 shows an example of SCI3 operation for transmission in clocked synchronous mode. In serial transmission, the SCI3 operates as described below.

1. The SCI3 monitors the TDRE flag in SSR, and if the flag is 0, the SCI recognizes that data has been written to TDR, and transfers the data from TDR to TSR.
2. The SCI3 sets the TDRE flag to 1 and starts transmission. If the TIE bit in SCR is set to 1 at this time, a TXI31 (TXI32) interrupt request is generated.
3. 8-bit data is sent from the TXD31 (TXD32) pin synchronized with the output clock when output clock mode has been specified, and synchronized with the input clock when use of an external clock has been specified. Serial data is transmitted sequentially from the LSB (bit 0), from the TXD31 (TXD32) pin.
4. The SCI checks the TDRE flag at the timing for sending the MSB (bit 7).
5. If the TDRE flag is cleared to 0, data is transferred from TDR to TSR, and serial transmission of the next frame is started.
6. If the TDRE flag is set to 1, the TEND flag in SSR is set to 1, and the TDRE flag maintains the output state of the last bit. If the TEIE bit in SCR is set to 1 at this time, a TEI31 (TEI32) is generated.
7. The SCK31 (SCK32) pin is fixed high.

Figure 15.11 shows a sample flowchart for serial data transmission. Even if the TDRE flag is cleared to 0, transmission will not start while a receive error flag (OER, FER, or PER) is set to 1. Make sure that the receive error flags are cleared to 0 before starting transmission.

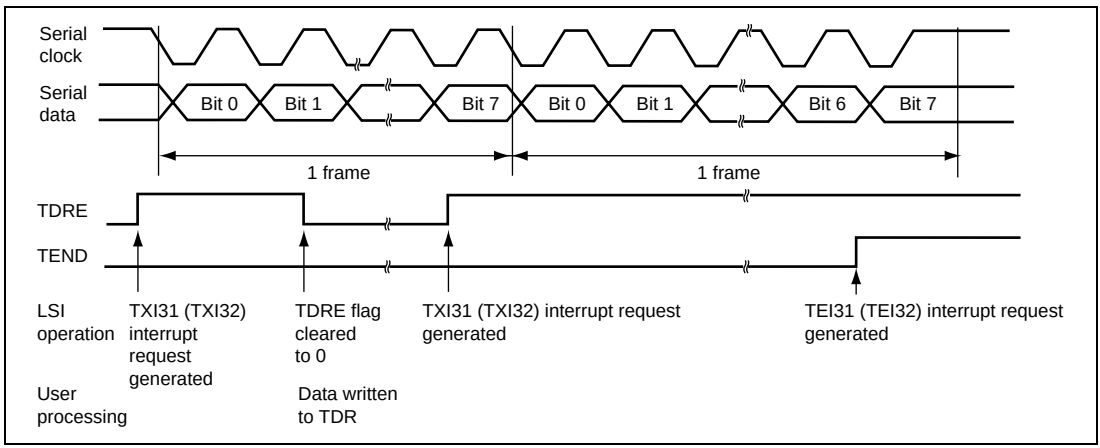
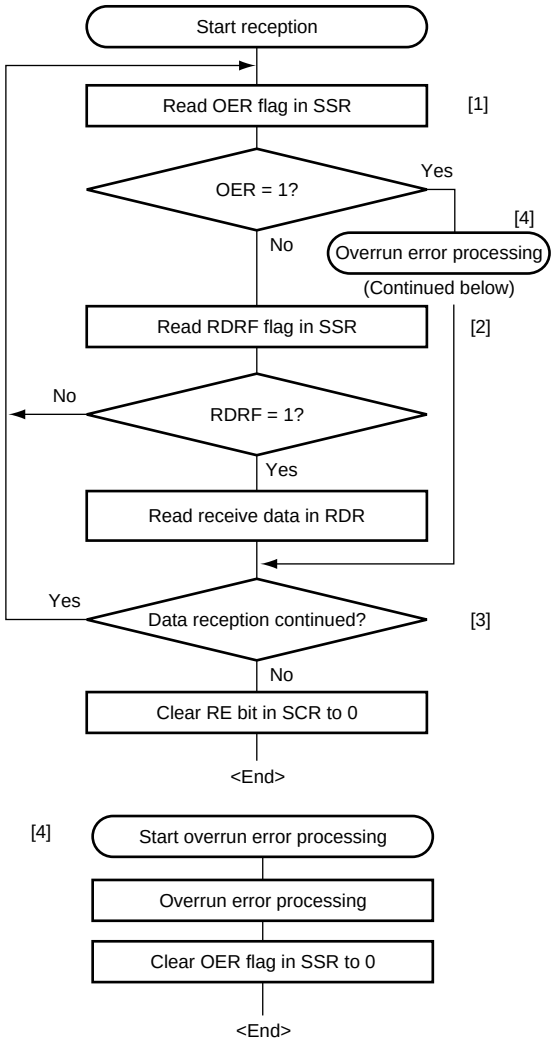


Figure 15.10 Example of SCI3 Operation in Transmission in Clocked Synchronous Mode

Reception cannot be resumed while a receive error flag is set to 1. Accordingly, clear the OER, FER, PER, and RDRF bits to 0 before resuming reception. Figure 15.13 shows a sample flowchart for serial data reception.



[1] Read the OER flag in SSR to determine if there is an error. If an overrun error has occurred, execute overrun error processing.

[2] Read SSR and check that the RDRF flag is set to 1, then read the receive data in RDR. When data is read from RDR, the RDRF flag is automatically cleared to 0.

[3] To continue serial reception, before the MSB (bit 7) of the current frame is received, reading the RDRF flag and reading RDR should be finished. When data is read from RDR, the RDRF flag is automatically cleared to 0.

[4] If an overrun error occurs, read the OER flag in SSR, and after performing the appropriate error processing, clear the OER flag to 0. Reception cannot be resumed if the OER flag is set to 1.

Figure 15.13 Sample Serial Reception Flowchart (Clocked Synchronous Mode)

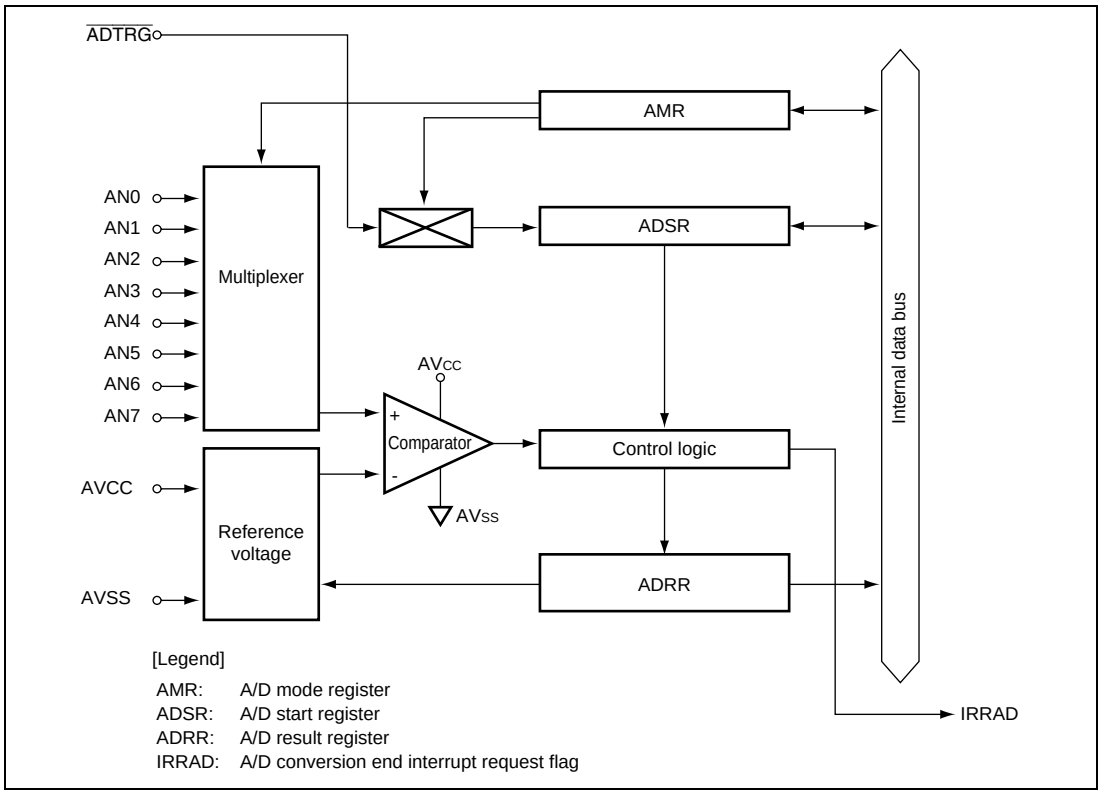


Figure 18.1 Block Diagram of A/D Converter

24.2.2 DC Characteristics

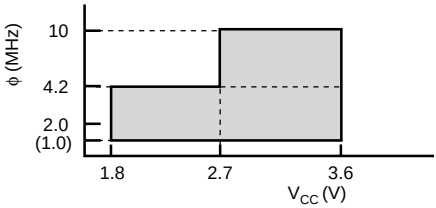
Table 24.2 lists the DC characteristics.

Table 24.2 DC Characteristics

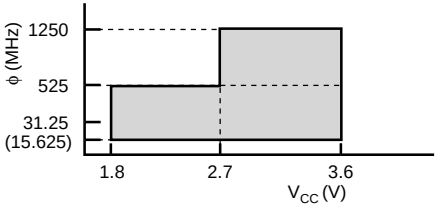
V_{CC} = 1.8 V to 3.6 V, AV_{CC} = 1.8 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, unless otherwise specified.

				Values				
Item	**Symbol**	**Applicable Pins**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**	**Notes**
Input high voltage	V_{IH}	$\overline{RES}$, $\overline{NMI}$*[3], $\overline{WKP0}$ to $\overline{WKP7}$, $\overline{IRQ4}$, AEVL, AEVH, TMIF, $\overline{ADTRG}$, SCK32, SCK31, SCK4		0.9V_{cc}	—	V_{cc} + 0.3	V	
		$\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{IRQ3}$		0.9V_{cc}	—	AV_{cc} + 0.3		
		RXD32, RXD31		0.8V_{cc}	—	V_{cc} + 0.3		
		OSC1		0.9V_{cc}	—	V_{cc} + 0.3		
		X1	V_{cc} = 2.7 to 3.6 V	0.9V_{cc}	—	V_{cc} + 0.3		
		P10 to P16, P30 to P32, P36, P37, P40 to P42, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P93, PA0 to PA3, TCLKA, TCLKB, TCLKC, TIOCA1, TIOCA2, TIOCB1, TIOCB2, SCL, SDA		0.8V_{cc}	—	V_{cc} + 0.3		
		PB0 to PB7		0.8V_{cc}	—	AV_{cc} + 0.3		
		IRQAEC		0.9V_{cc}	—	V_{cc} + 0.3		

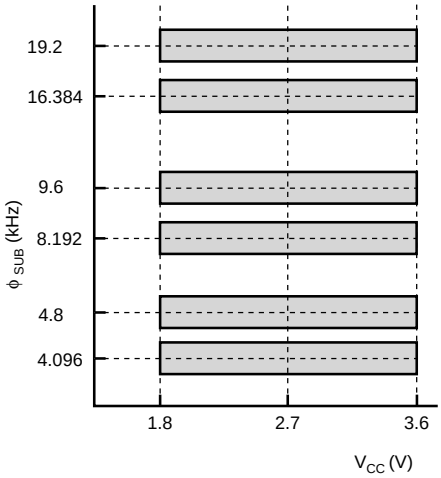
(2) Power Supply Voltage and Operating Frequency Range



- Active (high-speed) mode
- Sleep (high-speed) mode (except CPU)
- Refer to no.1 in the note.



- Active (medium-speed) mode
- Sleep (medium-speed) mode (except A/D converter)
- Refer to no.2 in the note.



- Subactive mode
- Subsleep mode (except CPU)
- Watch mode (except CPU)

Notes: 1. The value in parentheses is the minimum operating frequency when an external clock is input. When using a resonator, the minimum operating frequency (ϕ) is 2 MHz.

2. The value in parentheses is the minimum operating frequency when an external clock is input. When using a resonator, the minimum operating frequency (ϕ) is 31.25 kHz.

24.4.2 DC Characteristics

Table 24.12 lists the DC characteristics.

Table 24.12 DC Characteristics

V_{CC} = 1.8 V to 3.6 V, AV_{CC} = 1.8 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, unless otherwise specified.

				Values				
Item	**Symbol**	**Applicable Pins**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**	**Notes**
Input high voltage	V_{IH}	$\overline{RES}$, $\overline{NMI}$, $\overline{WKP0}$ to $\overline{WKP7}$, $\overline{IRQ4}$, AEVL, AEVH, TMIF, $\overline{ADTRG}$, SCK32, SCK31		0.9V_{cc}	—	V_{cc} + 0.3	V	
		$\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{IRQ3}$		0.9V_{cc}	—	AV_{cc} + 0.3		
		RXD32, RXD31		0.8V_{cc}	—	V_{cc} + 0.3		
		OSC1		0.9V_{cc}	—	V_{cc} + 0.3		
		X1	V_{cc} = 2.7 to 3.6 V	0.9V_{cc}	—	V_{cc} + 0.3		
		P10 to P16, P30 to P32, P36, P37, P40 to P42, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P93, PA0 to PA3, TCLKA, TCLKB, TCLKC, TIOCA1, TIOCA2, TIOCB1, TIOCB2, SCL, SDA		0.8V_{cc}	—	V_{cc} + 0.3		
		PB0 to PB7		0.8V_{cc}	—	AV_{cc} + 0.3		
		IRQAEC		0.9V_{cc}	—	V_{cc} + 0.3		

24.4.5 LCD Characteristics

Table 24.17 shows the LCD characteristics.

Table 24.17 LCD Characteristics

V_{CC} = 1.8 V to 3.6 V, AV_{CC} = 1.8 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, unless otherwise specified.

Item	Symbol	Applicable Pins	Test Condition	Values			Unit	Notes
				Min.	Typ.	Max.		
Segment driver drop voltage	V_{DS}	SEG1 to SEG32	I_D = 2 µA V1 = 2.7 V to 3.6 V	—	—	0.6	V	*1
Common driver drop voltage	V_{DC}	COM1 to COM4	I_D = 2 µA V1 = 2.7 V to 3.6 V	—	—	0.3	V	*1
LCD power supply split-resistance	R_{LCD}		Between V1 and V_{SS}	1.5	3.0	7.0	MΩ	
LCD display voltage	V_{LCD}	V1		2.2	—	3.6	V	*2
V3 power supply voltage	V_{LCD3}	V3	Between V3 and V_{SS}	0.9	1.0	1.1	V	*3*4
V2 power supply voltage	V_{LCD2}	V2	Between V2 and V_{SS}	—	2.0 (V_{LCD3} × 2)	—	V	*3*4
V1 power supply voltage	V_{LCD1}	V1	Between V1 and V_{SS}	—	3.0 (V_{LCD3} × 3)	—	V	*3*4
3-V constant voltage LCD power supply circuit current consumption	I_{LCD}	Vcc	V_{CC} = 3.0 V Booster clock: 125 kHz	—	20	—	µA	Reference value*4*5

Notes:
1. The voltage drop from power supply pins V1, V2, V3, and V_{SS} to each segment pin or common pin.
2. When the LCD display voltage is supplied from an external power source, ensure that the following relationship is maintained: V1 ≥ V2 ≥ V3 ≥ V_{SS}.
3. The value when the LCD power supply split-resistor is separated and 3-V constant voltage power supply circuit is driven.
4. For details on the register (BGRMR) setting range when the voltage of the V3 pin is set to 1.0 V, refer to section 19.3.5, BGR Control Register (BGRMR).
5. Includes the current consumption of the band-gap reference circuit (BGR) (operation).

Table A.1 Instruction Set

1. Data Transfer Instructions

Mnemonic		Operand Size	Addressing Mode and Instruction Length (bytes)									Operation	Condition Code						No. of States*1	
			#xx	Rn	@ERn	@(d, ERn)	@–ERn/@ERn+	@aa	@(d, PC)	@@aa	—		I	H	N	Z	V	C	Normal	Advanced
MOV	MOV.B #xx:8, Rd	B	2									#xx:8 → Rd8	—	—	↕	↕	0	—	2	
	MOV.B Rs, Rd	B		2								Rs8 → Rd8	—	—	↕	↕	0	—	2	
	MOV.B @ERs, Rd	B			2							@ERs → Rd8	—	—	↕	↕	0	—	4	
	MOV.B @(d:16, ERs), Rd	B				4						@(d:16, ERs) → Rd8	—	—	↕	↕	0	—	6	
	MOV.B @(d:24, ERs), Rd	B				8						@(d:24, ERs) → Rd8	—	—	↕	↕	0	—	10	
	MOV.B @ERs+, Rd	B					2					@ERs → Rd8 ERs32+1 → ERs32	—	—	↕	↕	0	—	6	
	MOV.B @aa:8, Rd	B						2				@aa:8 → Rd8	—	—	↕	↕	0	—	4	
	MOV.B @aa:16, Rd	B						4				@aa:16 → Rd8	—	—	↕	↕	0	—	6	
	MOV.B @aa:24, Rd	B						6				@aa:24 → Rd8	—	—	↕	↕	0	—	8	
	MOV.B Rs, @ERd	B			2							Rs8 → @ERd	—	—	↕	↕	0	—	4	
	MOV.B Rs, @(d:16, ERd)	B				4						Rs8 → @(d:16, ERd)	—	—	↕	↕	0	—	6	
	MOV.B Rs, @(d:24, ERd)	B				8						Rs8 → @(d:24, ERd)	—	—	↕	↕	0	—	10	
	MOV.B Rs, @–ERd	B					2					ERd32–1 → ERd32 Rs8 → @ERd	—	—	↕	↕	0	—	6	
	MOV.B Rs, @aa:8	B						2				Rs8 → @aa:8	—	—	↕	↕	0	—	4	
	MOV.B Rs, @aa:16	B						4				Rs8 → @aa:16	—	—	↕	↕	0	—	6	
	MOV.B Rs, @aa:24	B						6				Rs8 → @aa:24	—	—	↕	↕	0	—	8	
	MOV.W #xx:16, Rd	W	4									#xx:16 → Rd16	—	—	↕	↕	0	—	4	
	MOV.W Rs, Rd	W		2								Rs16 → Rd16	—	—	↕	↕	0	—	2	
	MOV.W @ERs, Rd	W			2							@ERs → Rd16	—	—	↕	↕	0	—	4	
	MOV.W @(d:16, ERs), Rd	W				4						@(d:16, ERs) → Rd16	—	—	↕	↕	0	—	6	
	MOV.W @(d:24, ERs), Rd	W				8						@(d:24, ERs) → Rd16	—	—	↕	↕	0	—	10	
	MOV.W @ERs+, Rd	W					2					@ERs → Rd16 ERs32+2 → @ERd32	—	—	↕	↕	0	—	6	
	MOV.W @aa:16, Rd	W						4				@aa:16 → Rd16	—	—	↕	↕	0	—	6	
	MOV.W @aa:24, Rd	W						6				@aa:24 → Rd16	—	—	↕	↕	0	—	8	
	MOV.W Rs, @ERd	W			2							Rs16 → @ERd	—	—	↕	↕	0	—	4	
	MOV.W Rs, @(d:16, ERd)	W				4						Rs16 → @(d:16, ERd)	—	—	↕	↕	0	—	6	
	MOV.W Rs, @(d:24, ERd)	W				8						Rs16 → @(d:24, ERd)	—	—	↕	↕	0	—	10	

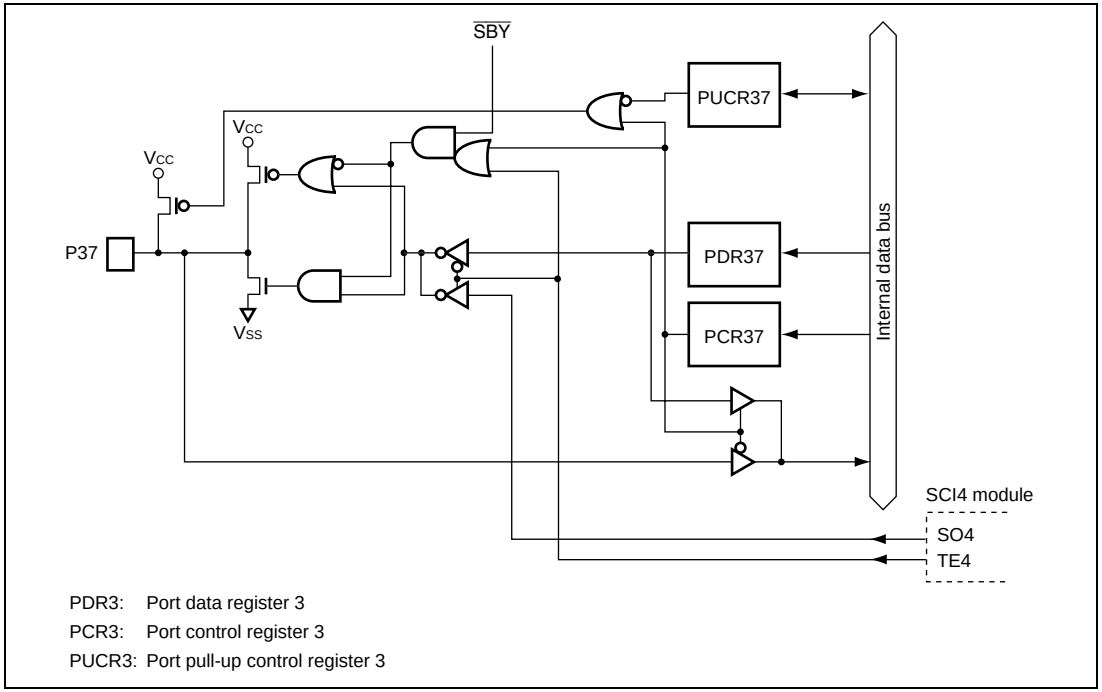


Figure B.2 (a) Port 3 Block Diagram (P37) (F-ZTAT Version)

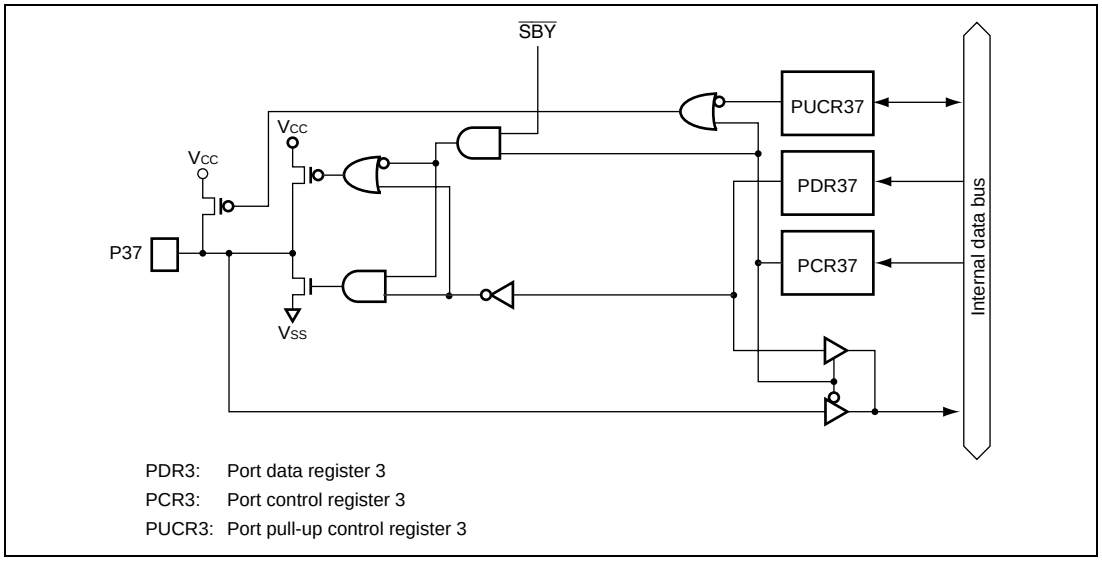


Figure B.2 (b) Port 3 Block Diagram (P37) (Masked ROM Version)

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