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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8/300H
Core Size	16-Bit
Speed	10MHz
Connectivity	I²C, IrDA, SCI
Peripherals	LCD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	52KB (52K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38076rw10wv

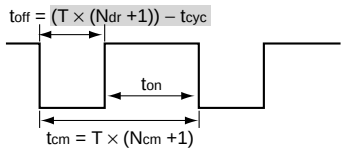
Item	Page	Revision (See Manual for Details)
13.3.6 Event Counter H (ECH)	287	Table amended

Bit	Bit Name	Initial Value	R/W	Description
7	ECH7	0	R	Either the external asynchronous event AEVH pin, φ/2, φ/4, or φ/8, or the overflow signal from lower 8-bit counter ECL can be selected as the input clock source. ECH can be cleared to H'00 by clearing CRCH in ESSCR to 0.
6	ECH6	0	R	
5	ECH5	0	R	
4	ECH4	0	R	
3	ECH3	0	R	
2	ECH2	0	R	
1	ECH1	0	R	
0	ECH0	0	R	

13.3.7 Event Counter L (ECL)		Table amended

Bit	Bit Name	Initial Value	R/W	Description
7	ECL7	0	R	Either the external asynchronous event AEVL pin, φ/2, φ/4, or φ/8 can be selected as the input clock source. ECL can be cleared to H'00 by clearing CRCL in ESSCR to 0.
6	ECL6	0	R	
5	ECL5	0	R	
4	ECL4	0	R	
3	ECL3	0	R	
2	ECL2	0	R	
1	ECL1	0	R	
0	ECL0	0	R	

13.4.4 Event Counter PWM Operation Figure 13.4 Event Counter Operation Waveform	290	Figure amended



t_{on}: Clock input enable time
t_{off}: Clock input disable time
t_{cm}: One conversion period
T: ECPWM input clock cycle
N_{dr}: Value of ECPWDR
Fixed low when N_{dr} =H'FFFF
N_{cm}: Value of ECPWCR
t_{cyc}: System cock (φ) cycle time

Table 13.2 Examples of Event Counter PWM Operation	291	Table amended

Clock Source Selection	Clock Source Cycle (T)*	ECPWCR Value (Ncm)	ECPWDR Value (Ndr)	toff = T x (Ndr + 1)	tcm = T x (Ncm + 1)	ton = tcm – toff
φ/2	0.5 µs	H'7A11	H'16E3	2.92975 ms	15.625 ms	12.69525 ms
φ/4	1 µs	D'31249	D'5859	5.85975 ms	31.25 ms	25.39025 ms
φ/8	2 µs			11.71975 ms	62.5 ms	50.78025 ms
φ/16	4 µs			23.43975 ms	125.0 ms	101.56025 ms
φ/32	8 µs			46.87975 ms	250.0 ms	203.12025 ms
φ/64	16 µs			93.75975 ms	500.0 ms	406.24025 ms

Item	Page	Revision (See Manual for Details)
15.3.8 Bit Rate Register (BRR) Table 15.3 Examples of BRR Settings for Various Bit Rates (Asynchronous Mode) (3)	322	Table amended

	4.9152MHz			5MHz			6MHz			6.144MHz		
Bit Rate (bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	86	0.31	2	88	–0.25	2	106	–0.44	2	108	0.08
150	3	15	0.00	2	64	0.16	2	77	0.16	3	19	0.00
200	3	11	0.00	2	48	–0.35	2	58	–0.69	3	14	0.00
250	2	37	1.05	2	38	0.16	2	46	–0.27	3	11	0.00
300	3	7	0.00	2	32	–1.36	2	38	0.16	3	9	0.00
600	3	3	0.00	0	255	1.73	3	4	–2.34	3	4	0.00
1200	3	1	0.00	0	129	0.16	0	155	0.16	2	9	0.00

Table 15.5 Maximum Bit Rate for Each Frequency (Asynchronous Mode)	324	Table amended

		Setting	
OSC (MHz)	Maximum Bit Rate (bit/s)	n	N
0.0328	512.5	0	0
0.0384	600	0	0
2	62500	0	0

Table 15.6 BRR Settings for Various Bit Rates (Clocked Synchronous Mode) (1)	325	Table amended

ϕ	32.8 kHz			38.4 kHz			2 MHz		
Bit Rate (bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
200	0	20	–2.38	0	23	0.00	2	155	0.16
250	0	15	2.50	0	18	1.05	2	124	0.00
300	0	13	–2.38	0	15	0.00	2	103	0.16
500	0	7	2.50	—	—	—	2	62	–0.79
1k	0	3	2.50	—	—	—	2	30	0.81

Table 15.6 BRR Settings for Various Bit Rates (Clocked Synchronous Mode) (2)	326	Table and note amended

ϕ	4 MHz			8 MHz			10 MHz		
Bit Rate (bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
10k	0	99	0.00	0	199	0.00	2	15	–2.34

Note: * Continuous transmission/reception is not possible.

The value set in BRR is given by the following formula:

Active (medium-speed/high-speed) or sleep (medium-speed/high-speed)

$$N = \frac{OSC}{4 \times 2^{2n} \times B} - 1$$

Subactive or subsleep

$$N = \frac{OSC}{8 \times 2^{2n} \times B} - 1$$

B: Bit rate (bit/s)

N: BRR setting for baud rate generator ($0 \le N \le 255$)

OSC: ϕ_{osc} value (Hz)

n: Baud rate generator input clock number (n = 0, 2, or 3)
(The relation between n and the clock is shown in table 15.7.)

Item	Page	Revision (See Manual for Details)
15.3.9 Serial Port Control Register (SPCR)	328	Table amended

Bit	Bit Name	Initial Value	R/W	Description
3	SCINV3	0	R/W	TXD32 Pin Output Data Inversion Switch Selects whether the polarity of output data of the TXD32 pin is inverted or not. 0: Output data of TXD32 pin is not inverted. 1: Output data of TXD32 pin is inverted.
2	SCINV2	0	R/W	RXD32 Pin Input Data Inversion Switch Selects whether the polarity of input data of the RXD32 pin is inverted or not. 0: Output data of RXD32 pin is not inverted. 1: Output data of RXD32 pin is inverted.
1	SCINV1	0	R/W	TXD31 Pin Output Data Inversion Switch Selects whether the polarity of output data of the TXD31 pin is inverted or not. 0: Output data of TXD31 pin is not inverted. 1: Output data of TXD31 pin is inverted.
0	SCINV0	0	R/W	RXD31 Pin Input Data Inversion Switch Selects whether the polarity of input data of the RXD31 pin is inverted or not. 0: Input data of RXD31 pin is not inverted. 1: Input data of RXD31 pin is inverted.

15.4.1 Clock Table 15.8 Data Transfer Formats (Asynchronous Mode)	332	Table amended

SMR				Serial Data Transfer Format and Frame Length
CHR	PE	MP	STOP	1 2 3 4 5 6 7 8 9 10 11 12
0	0	1	0	Setting prohibited
0	0	1	1	Setting prohibited
1	0	1	0	Setting prohibited
1	0	1	1	Setting prohibited

Table 15.9 SMR Settings and Corresponding Data Transfer Formats	333	Table amended

SMR						Data Transfer Format		
Bit 7 COM	Bit 6 CHR	Bit 2 MP	Bit 5 PE	Bit 3 STOP	Mode	Data Length	Parity Bit	Stop Bit Length
0	0	1	0	0	Asynchronous mode	Setting prohibited		
				1				
			1	0		5-bit data	No	1 bit
				1				2 bits
	1		0	0		Setting prohibited		
				1				
			1	0		5-bit data	Yes	1 bit
				1				2 bits

15.4.2 SCI3 Initialization Figure 15.4 Sample SCI3 Initialization Flowchart	335	Figure amended [4] Wait at least one bit interval, then set the TE bit or RE bit in SCR to 1. Setting bits TE and RE enables the TXD31 (TXD32) and RXD31 (RXD32) pins to be used. Also set the RIE, TIE, and TEIE bits,

Section 13 Asynchronous Event Counter (AEC)

Section 14 Watchdog Timer

Section 15 Serial Communication Interface 3 (SCI3, IrDA)

Type	Symbol	Pin No. FP-80A, TFP-80C	Pin No. TLP-85V	Pad No.*[1]	Pad No.*[2]	I/O	Functions
LCD controller/ driver	COM1 to COM4	27 to 30	J4, K5, H5, J6	28 to 31	27 to 30	Output	LCD common output pins.
	SEG1 to SEG8	31 to 38	J5, H6, H7, K6, J7, J8, K7, H8	32 to 39	31 to 38	Output	LCD segment output pins.
	SEG9 to SEG16	39 to 46	K9, K8, J10 H10, J9, H9, G8	40 to 47	39 to 46	Output	
	SEG17 to SEG24	47 to 54	G9, F10, F8, E9, F9, E8, D8, E10	48 to 55	47 to 54	Output	
	SEG25 to SEG32	55 to 62	D9, C9, D10, C8, B10, C10, A9, A8	56 to 63	55 to 62	Output	
I/O ports	P10 to P12	78 to 80	C3, A2, A3	79 to 81	78 to 80	I/O	7-bit I/O pins. Input or output can be designated for each bit by means of the port control register 1 (PCR1).
	P13 to P16	1 to 4	B1, C1, B2, C2	1 to 4	1 to 4		
	P30 to P32, P36, P37	5 to 9	D1, D3, D2, E1, E3	5 to 9	5 to 9	I/O	5-bit I/O pins. Input or output can be designated for each bit by means of the port control register 3 (PCR3).
	P40 to P42	18 to 20	H3, J1, H1	19 to 21	18 to 20	I/O	3-bit I/O pins. Input or output can be designated for each bit by means of the port control register 4 (PCR4).
	P50 to P57	31 to 38	J5, H6, H7, K6, J7, J8, K7, H8	32 to 39	31 to 38	I/O	8-bit I/O pins. Input or output can be designated for each bit by means of the port control register 5 (PCR5).
	P60 to P67	39 to 46	K9, K8, J10, H10, J9, H9, G10, G8	40 to 47	39 to 46	I/O	8-bit I/O pins. Input or output can be designated for each bit by means of the port control register 6 (PCR6).

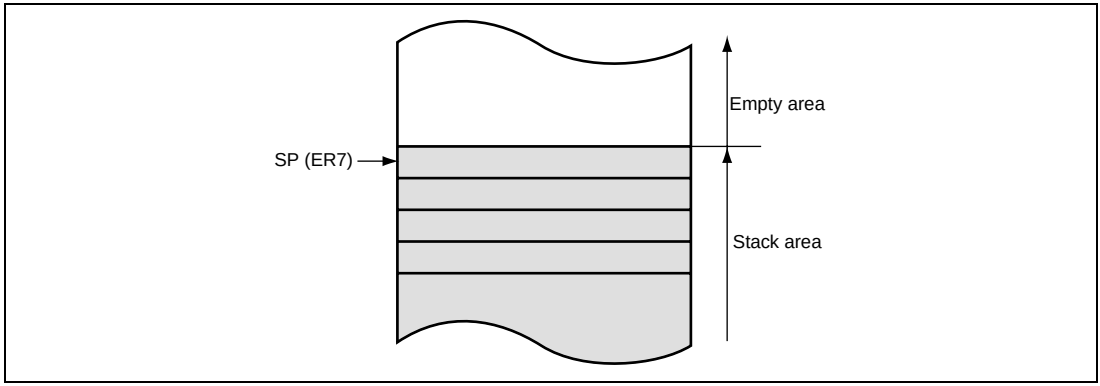


Figure 2.4 Relationship between Stack Pointer and Stack Area

2.2.2 Program Counter (PC)

This 24-bit counter indicates the address of the next instruction the CPU will execute. The length of all CPU instructions is 2 bytes (one word), so the least significant PC bit is ignored. (When an instruction is fetched, the least significant PC bit is regarded as 0). The PC is initialized when the start address is loaded by the vector address generated during reset exception-handling sequence.

2.2.3 Condition-Code Register (CCR)

This 8-bit register contains internal CPU status information, including an interrupt mask bit (I) and half-carry (H), negative (N), zero (Z), overflow (V), and carry (C) flags. The I bit is initialized to 1 by reset exception-handling sequence, but other bits are not initialized.

Some instructions leave flag bits unchanged. Operations can be performed on the CCR bits by the LDC, STC, ANDC, ORC, and XORC instructions. The N, Z, V, and C flags are used as branching conditions for conditional branch (Bcc) instructions.

For the action of each instruction on the flag bits, see Appendix A.1, Instruction List.

2.4.2 Basic Instruction Formats

H8/300H CPU instructions consist of 2-byte (1-word) units. An instruction consists of an operation field (op), a register field (r), an effective address extension (EA), and a condition field (cc).

Figure 2.7 shows examples of instruction formats.

(1) Operation Field

Indicates the function of the instruction, the addressing mode, and the operation to be carried out on the operand. The operation field always includes the first four bits of the instruction. Some instructions have two operation fields.

(2) Register Field

Specifies a general register. Address registers are specified by 3 bits, and data registers by 3 bits or 4 bits. Some instructions have two register fields. Some have no register field.

(3) Effective Address Extension

8, 16, or 32 bits specifying immediate data, an absolute address, or a displacement. A24-bit address or displacement is treated as a 32-bit data in which the first 8 bits are 0 (H'00).

(4) Condition Field

Specifies the branching condition of Bcc instructions.

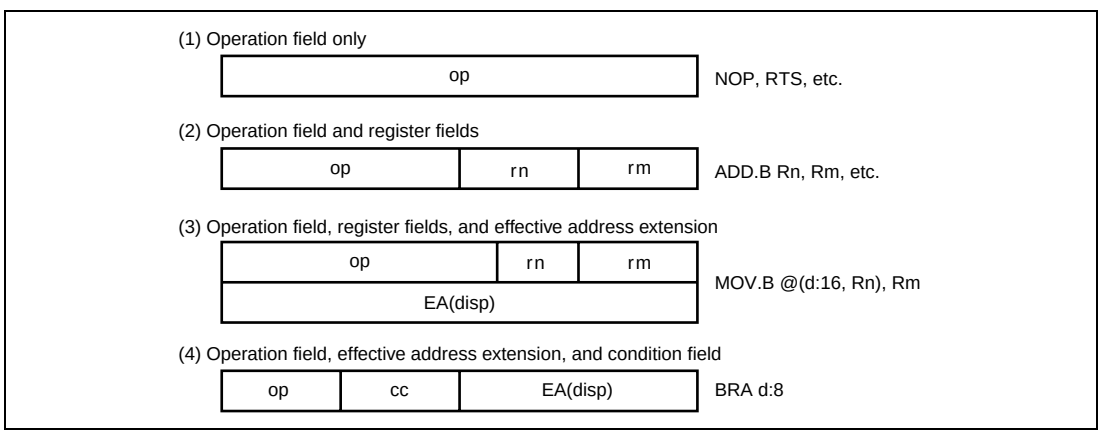


Figure 2.7 Instruction Formats

6.2.1 Sleep Mode

In sleep mode, CPU operation is halted but the system clock oscillator, subclock oscillator, and on-chip peripheral modules function. In sleep (medium-speed) mode, the on-chip peripheral modules function at the clock frequency set by the MA1 and MA0 bits in SYSCR1. CPU register contents are retained.

Sleep mode is cleared by an interrupt. When an interrupt is requested, sleep mode is cleared and interrupt exception handling starts. Sleep mode is not cleared if the I bit in CCR is set to 1 or the requested interrupt is disabled by the interrupt enable bit. After sleep mode is cleared, a transition is made from sleep (high-speed) mode to active (high-speed) mode or from sleep (medium-speed) mode to active (medium-speed) mode.

When the $\overline{\text{RES}}$ pin goes low, the CPU goes into the reset state and sleep mode is cleared. Since an interrupt request signal is synchronous with the system clock, the maximum time of $2/\phi$ (s) may be delayed from the point at which an interrupt request signal occurs until the interrupt exception handling is started.

Furthermore, it sometimes operates with half state early timing at the time of transition to sleep (medium-speed) mode.

6.2.2 Standby Mode

In standby mode, the system clock oscillator stops, so the CPU and on-chip peripheral modules stop functioning when the WDT disables the on-chip oscillator operation. However, as long as the rated voltage is supplied, the contents of CPU registers, on-chip RAM, and some on-chip peripheral module registers are retained. On-chip RAM contents will be retained as long as the voltage set by the RAM data retention voltage is provided. The I/O ports go to the high-impedance state.

Standby mode is cleared by an interrupt. When an interrupt is requested, the system clock pulse generator starts. After the time set in bits STS2 to STS0 in SYSCR1 has elapsed, standby mode is cleared and interrupt exception handling starts. After standby mode is cleared, a transition is made to active (high-speed) or active (medium-speed) mode according to the MSON bit in SYSCR2. Standby mode is not cleared if the I bit in CCR is set to 1 or the requested interrupt is disabled by the interrupt enable bit.

When the $\overline{\text{RES}}$ pin goes low, the system clock oscillator starts. Since system clock signals are supplied to the entire chip as soon as the system clock oscillator starts functioning, the $\overline{\text{RES}}$ pin must be kept low until the system clock oscillator output stabilizes (except when the power-on

6.3.4 Direct Transition from Active (Medium-Speed) Mode to Subactive Mode

The time from the start of SLEEP instruction execution to the end of interrupt exception handling (the direct transition time) is calculated by equation (4).

Direct transition time = {(Number of SLEEP instruction execution states) + (Number of internal processing states)} × (tcyc before transition) + (Number of interrupt exception handling execution states) × (tsubcyc after transition)

……(4)

Example: When ϕosc/8 is selected as the CPU operating clock before transition

Direct transition time = (2 + 1) × 8tosc + 14 × 1tsubcyc = 24tosc + 14tsubcyc

[Legend]
tosc: OSC clock cycle time
tsubcyc: Subclock (ϕ_{SUB}) cycle time

6.3.5 Direct Transition from Subactive Mode to Active (High-Speed) Mode

The time from the start of SLEEP instruction execution to the end of interrupt exception handling (the direct transition time) is calculated by equation (5).

Direct transition time = {(Number of SLEEP instruction execution states) + (Number of internal processing states)} × (tsubcyc before transition) + {(Wait time set in bits STS2 to STS0) + (Number of interrupt exception handling execution states)} × (tcyc after transition)

……..(5)

Example: When ϕw/8 is selected as the CPU operating clock before transition and wait time = 8192 states

Direct transition time = (2 + 1) × 8tw + (8192 + 14) × tosc = 24tw + 8206tosc

[Legend]
tosc: OSC clock cycle time
tw: Watch clock cycle time
tcyc: System clock (ϕ) cycle time
tsubcyc: Subclock (ϕ_{SUB}) cycle time

9.9 Port A

Port A is an I/O port also functioning as an LCD common output pin. Figure 9.9 shows its pin configuration.

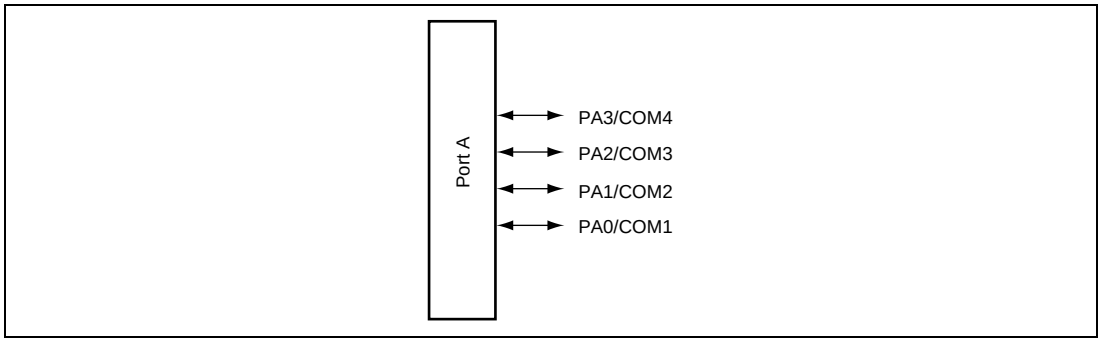


Figure 9.9 Port A Pin Configuration

Port A has the following registers.

- Port data register A (PDRA)
- Port control register A (PCRA)

9.9.1 Port Data Register A (PDRA)

PDRA is a register that stores data of port A.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 1	—	Reserved These bits are always read as 1 and cannot be modified.
3	PA3	0	R/W	If port A is read while PCRA bits are set to 1, the values stored in PDRA are read, regardless of the actual pin states. If port A is read while PCRA bits are cleared to 0, the pin states are read.
2	PA2	0	R/W	
1	PA1	0	R/W	
0	PA0	0	R/W	

15.4.1 Clock

Either an internal clock generated by the on-chip baud rate generator or an external clock input at the SCK31 (SCK32) pin can be selected as the SCI3's serial clock source, according to the setting of the COM bit in SMR and the CKE0 and CKE1 bits in SCR. When an external clock is input at the SCK31 (SCK32) pin, the clock frequency should be 16 times the bit rate used. For details on selection of the clock source, see table 15.10. When the SCI3 is operated on an internal clock, the clock can be output from the SCK31 (SCK32) pin. The frequency of the clock output in this case is equal to the bit rate, and the phase is such that the rising edge of the clock is in the middle of the transfer data, as shown in figure 15.3.

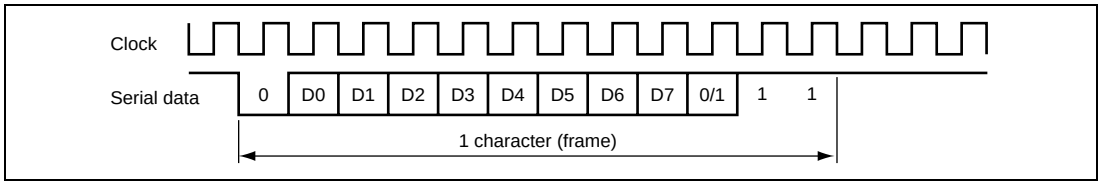


Figure 15.3 Relationship between Output Clock and Transfer Data Phase (Asynchronous Mode) (Example with 8-Bit Data, Parity, Two Stop Bits)

Section 19 LCD Controller/Driver

This LSI has an on-chip segment-type LCD control circuit, LCD driver, and power supply circuit, enabling it to directly drive an LCD panel.

19.1 Features

- Display capacity

Duty Cycle	Internal Driver
Static	32 SEG
1/2	32 SEG
1/3	32 SEG
1/4	32 SEG

- LCD RAM capacity
  8 bits × 16 bytes (128 bits)
- Word access to LCD RAM
- The segment output pins can be used as ports.
  SEG32 to SEG1 pins can be used as ports in groups of four.
- Common output pins not used because of the duty cycle can be used for common double-buffering (parallel connection).
  With 1/2 duty, parallel connection of COM1 to COM2, and of COM3 to COM4, can be used
  In static mode, parallel connection of COM1 to COM2, COM3, and COM4 can be used
- Choice of 11 frame frequencies
- A or B waveform selectable by software
- On-chip power supply split-resistor
- Display possible in operating modes other than standby mode
- On-chip 3-V constant-voltage power supply circuit
  This power circuit can constantly supply 3 V to LCD drive power supply without using Vcc voltage.
- Output of the 3-V constant-voltage power supply circuit adjustable
- Use of module standby mode enables this module to be placed in standby mode independently when not used. (For details, refer to section 6.4, Module Standby Function.)

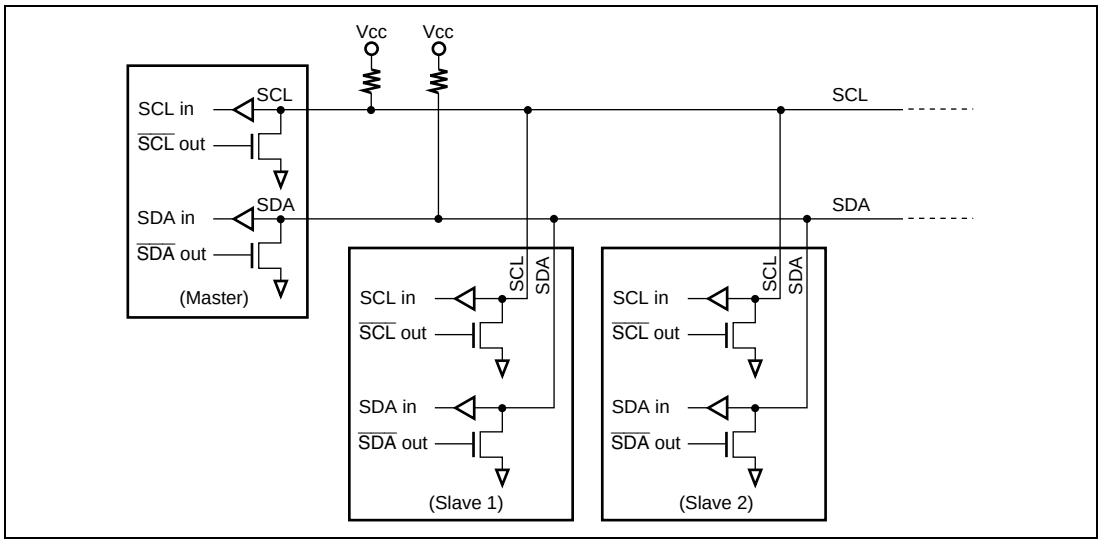


Figure 20.2 External Circuit Connections of I/O Pins

20.2 Input/Output Pins

Table 20.1 summarizes the input/output pins used by the I²C bus interface 2.

Table 20.1 Pin Configuration

Name	Abbreviation	I/O	Function
Serial clock pin	SCL	I/O	IIC serial clock input/output
Serial data pin	SDA	I/O	IIC serial data input/output

24.2.3 AC Characteristics

Table 24.3 lists the control signal timing, table 24.4 lists the serial interface timing, and table 24.5 lists the I^2C bus interface timing.

Table 24.3 Control Signal Timing

V_{CC} = 1.8 V to 3.6 V, AV_{CC} = 1.8 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, unless otherwise specified.

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Reference Figure
System clock oscillation frequency	f_{OSC}	OSC1, OSC2	V_{CC} = 2.7 to 3.6 V	2.0	—	10.0	MHz	
			V_{CC} = 1.8 to 3.6 V	2.0	—	4.2		
OSC clock (ϕ_{OSC}) cycle time	t_{OSC}	OSC1, OSC2	V_{CC} = 2.7 to 3.6 V	100	—	500 (1000)	ns	Figure 24.2 *2
			V_{CC} = 1.8 to 3.6 V	238	—	500 (1000)		
System clock (ϕ) cycle time	t_{cyc}			1	—	64	t_{OSC}	
				—	—	64	µs	
Subclock oscillation frequency	f_w	X1, X2		—	32.768 or 38.4	—	kHz	
Watch clock (ϕ_w) cycle time	t_w	X1, X2		—	30.5 or 26.0	—	µs	Figure 24.2
Subclock (ϕ_{SUB}) cycle time	t_{subcyc}			2	—	8	t_w	*1
Instruction cycle time				2	—	—	t_{cyc} t_{subcyc}	
Oscillation stabilization time	t_{rc}	OSC1, OSC2	Crystal resonator (V_{CC} = 2.7 to 3.6 V)	—	0.8	2.0	ms	
			Crystal resonator (V_{CC} = 2.2 to 3.6 V)	—	1.2	3		
			Ceramic resonator (V_{CC} = 2.2 to 3.6 V)	—	20	45	µs	
			Ceramic resonator (other than above)	—	80	—		
			Other than above	—	—	50	ms	
		×1, ×2	V_{CC} = 2.2 to 3.6 V	—	—	2.0	s	Figure 5.7
			Other than above	—	4	—		

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Reference Figure
Oscillation stabilization time	t_{rc}	OSC1, OSC2	Crystal resonator V_{cc} = 2.7 to 3.6 V	—	0.8	2.0	ms	
			Crystal resonator V_{cc} = 2.2 to 3.6 V	—	1.2	3.0		
			Ceramic resonator V_{cc} = 2.2 to 3.6 V	—	20	45	µs	
			Ceramic resonator Other than above	—	80	—		
			Other than above	—	—	50	ms	
			When on-chip oscillator is selected	—	—	100	µs	*4
		X1, X2	V_{cc} = 2.2 to 3.6 V	—	—	2.0	s	Figure 5.7
			Other than above	—	4	—		
External clock high width	t_{CPH}	OSC1	V_{cc} = 2.7 to 3.6 V	40	—	—	ns	Figure 24.2
			V_{cc} = 1.8 to 3.6 V	95	—	—		
		X1		—	15.26 or 13.02	—	µs	
External clock low width	t_{CPL}	OSC1	V_{cc} = 2.7 to 3.6 V	40	—	—	ns	Figure 24.2
			V_{cc} = 1.8 to 3.6 V	95	—	—		
		X1		—	15.26 or 13.02	—	µs	
External clock rise time	t_{CPr}	OSC1	V_{cc} = 2.7 to 3.6 V	—	—	10	ns	Figure 24.2
			V_{cc} = 1.8 to 3.6 V	—	—	24		
		X1		—	—	55.0	ns	
External clock fall time	t_{CPf}	OSC1	V_{cc} = 2.7 to 3.6 V	—	—	10	ns	Figure 24.2
			V_{cc} = 1.8 to 3.6 V	—	—	24		
		X1		—	—	55.0	ns	
$\overline{RES}$ pin low width	t_{REL}	$\overline{RES}$		10	—	—	t_{cyc}	Figure 24.3*3

Mnemonic		Operand Size	Addressing Mode and Instruction Length (bytes)									Operation	Condition Code						No. of States*1	
			#xx	Rn	@ERn	@(d, ERn)	@–ERn/@ERn+	@aa	@(d, PC)	@@aa	—		I	H	N	Z	V	C	Normal	Advanced
DEC	DEC.L #1, ERd	L		2								ERd32–1 → ERd32	—	—	↕	↕	↕	—	2	
	DEC.L #2, ERd	L		2								ERd32–2 → ERd32	—	—	↕	↕	↕	—	2	
DAS	DAS.Rd	B		2								Rd8 decimal adjust → Rd8	—	*	↕	↕	*	—	2	
MULXU	MULXU. B Rs, Rd	B		2								Rd8 × Rs8 → Rd16 (unsigned multiplication)	—	—	—	—	—	—	14	
	MULXU. W Rs, ERd	W		2								Rd16 × Rs16 → ERd32 (unsigned multiplication)	—	—	—	—	—	—	22	
MULXS	MULXS. B Rs, Rd	B		4								Rd8 × Rs8 → Rd16 (signed multiplication)	—	—	↕	↕	—	—	16	
	MULXS. W Rs, ERd	W		4								Rd16 × Rs16 → ERd32 (signed multiplication)	—	—	↕	↕	—	—	24	
DIVXU	DIVXU. B Rs, Rd	B		2								Rd16 ÷ Rs8 → Rd16 (RdH: remainder, RdL: quotient) (unsigned division)	—	—	(6)	(7)	—	—	14	
	DIVXU. W Rs, ERd	W		2								ERd32 ÷ Rs16 → ERd32 (Ed: remainder, Rd: quotient) (unsigned division)	—	—	(6)	(7)	—	—	22	
DIVXS	DIVXS. B Rs, Rd	B		4								Rd16 ÷ Rs8 → Rd16 (RdH: remainder, RdL: quotient) (signed division)	—	—	(8)	(7)	—	—	16	
	DIVXS. W Rs, ERd	W		4								ERd32 ÷ Rs16 → ERd32 (Ed: remainder, Rd: quotient) (signed division)	—	—	(8)	(7)	—	—	24	
CMP	CMP.B #xx:8, Rd	B	2									Rd8–#xx:8	—	↕	↕	↕	↕	↕	2	
	CMP.B Rs, Rd	B		2								Rd8–Rs8	—	↕	↕	↕	↕	↕	2	
	CMP.W #xx:16, Rd	W	4									Rd16–#xx:16	—	(1)	↕	↕	↕	↕	4	
	CMP.W Rs, Rd	W		2								Rd16–Rs16	—	(1)	↕	↕	↕	↕	2	
	CMP.L #xx:32, ERd	L	6									ERd32–#xx:32	—	(2)	↕	↕	↕	↕	4	
	CMP.L ERs, ERd	L		2								ERd32–ERs32	—	(2)	↕	↕	↕	↕	2	

A.4 Combinations of Instructions and Addressing Modes

Table A.5 Combinations of Instructions and Addressing Modes

Functions	Instructions	Addressing Mode												
		#xx	Rn	@ERn	@(d:16.ERn)	@(d:24.ERn)	@ERn+/@ERn	@aa:8	@aa:16	@aa:24	@(d:8.PC)	@(d:16.PC)	@@aa:8	—
Data transfer instructions	MOV	BWL	BWL	BWL	BWL	BWL	BWL	B	BWL	BWL	—	—	—	—
	POP, PUSH	—	—	—	—	—	—	—	—	—	—	—	—	WL
	MOVFPE, MOVTPE	—	—	—	—	—	—	—	—	—	—	—	—	—
Arithmetic operations	ADD, CMP	BWL	BWL	—	—	—	—	—	—	—	—	—	—	—
	SUB	WL	BWL	—	—	—	—	—	—	—	—	—	—	—
	ADDX, SUBX	B	B	—	—	—	—	—	—	—	—	—	—	—
	ADDS, SUBS	—	L	—	—	—	—	—	—	—	—	—	—	—
	INC, DEC	—	BWL	—	—	—	—	—	—	—	—	—	—	—
	DAA, DAS	—	B	—	—	—	—	—	—	—	—	—	—	—
	MULXU, MULXS, DIVXU, DIVXS	—	BW	—	—	—	—	—	—	—	—	—	—	—
	NEG	—	BWL	—	—	—	—	—	—	—	—	—	—	—
	EXTU, EXTS	—	WL	—	—	—	—	—	—	—	—	—	—	—
Logical operations	AND, OR, XOR	—	BWL	—	—	—	—	—	—	—	—	—	—	—
	NOT	—	BWL	—	—	—	—	—	—	—	—	—	—	—
Shift operations		—	BWL	—	—	—	—	—	—	—	—	—	—	—
Bit manipulations		—	B	B	—	—	—	B	—	—	—	—	—	—
Branching instructions	BCC, BSR	—	—	—	—	—	—	—	—	—	—	—	—	—
	JMP, JSR	—	—	◯	—	—	—	—	—	—	◯	◯	—	—
	RTS	—	—	—	—	—	—	—	—	◯	—	—	◯	—
System control instructions	RTE	—	—	—	—	—	—	—	—	—	—	—	—	◯
	SLEEP	—	—	—	—	—	—	—	—	—	—	—	—	◯
	LDC	B	B	W	W	W	W	—	W	W	—	—	—	◯
	STC	—	B	W	W	W	W	—	W	W	—	—	—	—
	ANDC, ORC, XORC	B	—	—	—	—	—	—	—	—	—	—	—	—
	NOP	—	—	—	—	—	—	—	—	—	—	—	—	◯
Block data transfer instructions		—	—	—	—	—	—	—	—	—	—	—	—	BW

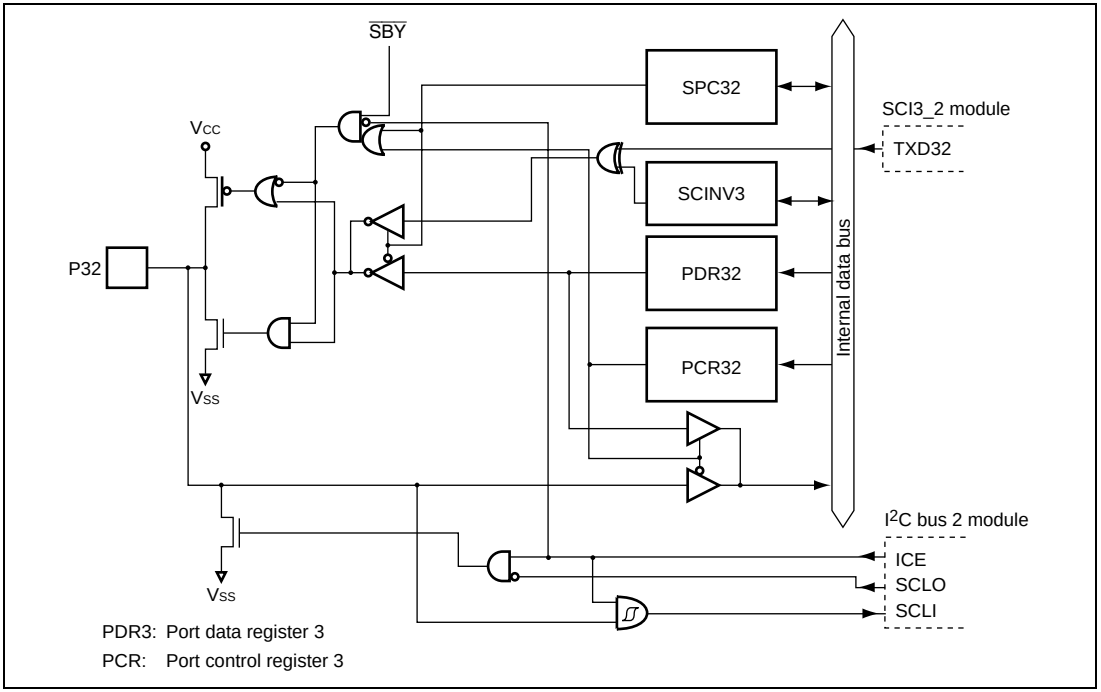


Figure B.2 (e) Port 3 Block Diagram (P32)