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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	Н8/300Н
Core Size	16-Bit
Speed	10MHz
Connectivity	I ² C, IrDA, SCI
Peripherals	LCD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	52KB (52K × 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38076rw10wv

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Item	Page	Revision (See Manual for Details)											
13.3.6 Event Counter	287	Table amended											
H (ECH)		Bit E	Bit Name	Initial Value	R/W	Descript	ion						
		7 E	CH7	0	R	Either the	external async	chronous event	AEVH pin, φ/2,				
		6 E	CH6	0	R	φ/4, or φ/8	3, or the overflo	or the overflow signal from lower 8-bit					
		5 E	CH5	0	R	ECH can	be cleared to H	be cleared to H'00 by clearing CRCH in					
		4 E	CH4	0	R	ESSCR to	o 0.						
		3 E	CH3	0	R								
		2 E	CH2	0	R								
		1 E	CH1	0	R								
		0 E	CH0	0	R								
13.3.7 Event Counter		Table	amende	ed									
		Bit	Bit Name	Initial Value	R/W	Descript	ion						
		7	ECL7	0	R	Either the	external async	chronous event	AEVL pin, ø/2,				
		6	ECL6	0	R	φ/4, or φ/8 ECL can	B can be selected to H	ed as the input o 100 by clearing (CRCL in ESSCR				
		5	ECL5	0	R	to 0.		oo by cloaning .					
		4	ECL4	0	R								
		3	ECL3	0	R								
		2	ECL2	0	R								
		1	ECL1	0	R								
		0	ECL0	0	R								
13.4.4 Event Counter PWM Operation	290	Figure	amend × (Ndr +1)		c		t : Clask	innut onchio	time				
Figure 13 / Event			→	,,,			toff: Clock	input enable	time				
Counter Operation							tcm: One conversion period						
			- to	on 🕨			T: ECPV	VM input cloc	k cycle				
waveform		-		►			Ndr: Value	of ECPWDR	1				
		tcm	= T × (Nc	m +1)			Fixed	low when Nd	r=H'FFFF				
							Ncm: Value of ECPWCR						
							tcyc: Syste	т соск (ф) су	cie time				
Table 13.2 Examples	291	Table	amende	ed									
Operation	I	Clock Source Selectior	Clock Source Cycle (T	ECF)* Val	PWCR ue (Ncm)	ECPWDR Value (Ndr)	toff = T x (Ndr + 1)	tcm = T x (Ncm + 1)	ton = tcm – toff				
		ф/2	0.5 µs	H'7/	A11	H'16E3	2.92975 ms	15.625 ms	12.69525 ms				
		φ/4	1 µs	D'3	1249	D'5859	5.85975 ms	31.25 ms	25.39025 ms				
		ф/8	2 µs				11.71975 ms	62.5 ms	50.78025 ms				
		ф/16	4 µs				23.43975 ms	125.0 ms	101.56025 ms				
		ф/32	8 µs				46.87975 ms	250.0 ms	203.12025 ms				
		φ/64	16 µs				93.75975 ms	500.0 ms	406.24025 ms				



Page Revision (See Manual for Details)

•		510	11 (0	ee wa	nua	TOF	Deta	iis)								
322	2 Table amended															
			4.915	4.9152MHz		5Mł	Ηz		6M	/Hz			6.144	MHz		
	Bit Rat	e	N	Error	- <u>-</u>	N	Error		N	Er	ror	<u>_</u>	N	Error		
	110	2	86	(%)	2	88	-0.25	2	106	(%) 44	2	108	0.08		
	150	3	15	0.00	2	64	0.16	2	77	0.1	.44	3	19	0.00		
	200	3	11	0.00	2	48	-0.35	2	58	-0	.69	3	14	0.00		
	250	2	37	1.05	2	38	0.16	2	46	-0	.27	3	11	0.00		
	300	3	7	0.00	2	32	-1.36	2	38	0.1	6	3	9	0.00		
	600	3	3	0.00	0	255	1.73	3	4	-2	.34	3	4	0.00		
	1200	3	1	0.00	0	129	0.16	0	155	0.1	6	2	9	0.00		
324	24 Table amended											Setti	ng			
	OSC (N	/Hz)		Ma	kimum	Bit Rat	e (bit/s)		n		Ν				
	0.0328			512	5					0		()			
	0.0384			600						0		()			
	2			625	00					0) 			
325	Table •	Table amended						2 MHz								
	Bit Rate															
	(bit/s)		ı	n N	Erro	r (%)	n	Ν	Error (%)	n	Ν	Erre	or (%)		
	200		() 20	-2.3	8	0	23	0.00		2	155	0.16	6		
	250		() 15	2.50		0	18	1.05		2	124	0.00)		
	300		() 13	-2.3	8	0	15	0.00		2	103	0.16	6		
	500		() 7	2.50		-	-	-		2	62	-0.7	79		
				, ,	2.50								0.0			
326	Table •	e a	nd no	ote arr 4	nend мнz	ed		8	3 MHz			1	0 MHz	2		
	Bit Rat (bit/s)	te	ı	n N	Erro	r (%)	n	N	Error (%)	n	N	Erre	or (%)		
	10k		() 99	0.00	····	0	199	0.00		2	15	-2.3	34		
	Note:	* (The B: N:	Value s Active (I N Subactiv N Bit ra BRR	bus trans et in BRF medium-s = $\frac{OS}{4 \times 2^2}$ we or sub- = $\frac{OS}{8 \times 2^2}$ ate (bit/s) setting fr	mission R is give peed/h SC $n \times B$ sleep SC $n \times B$ or bauc	n/recept en by th igh-spe - 1 - 1	ion is no e followi ed) or s	ot pos ing fo leep (0 ≤	ssible. ormula: (medium N ≤ 255)	-speed	l/high	-speed	D			
	322 324 324 325 326	322 Table Bit Rat (bit/s) 110 150 200 250 300 300 600 1200 120 324 Table 0SC (f) 0.0328 0.0384 2 325 Table Ø Bit Ra (bit/s) 200 250 300 500 1k 326 326 Table Ø Bit Ra (bit/s) 10k Note:	322 Table at Bit Rate (bit/s) n 110 2 150 3 200 3 250 2 300 3 600 3 1200 3 324 Table at 0.0328 0.0384 2 300 325 Table at	322 Table amend (bit/s) n N 110 2 86 150 3 15 200 3 11 250 2 37 300 3 7 600 3 3 1200 3 1 324 Table amend 0SC (MHz) 0.0328 0.0384 2 325 Table amend 0.0328 0.0384 2 326 Table amend 0.0328 0.0384 2 326 Table and no 500 c0 1k c0 326 Table and no 500 c0 1k c0 326 Table and no 500 c0 1k c0 Subactive (r Note: * Continue The value s Active (r N Subactive N Bit Rate (bit/s) N Bit Rate (bit/s) N	Table amended 4.9152MHz Bit Rate Error (bit/s) n N 110 2 86 0.31 150 3 15 0.00 200 3 11 0.00 250 2 37 1.05 300 3 7 0.00 600 3 3 0.00 1200 3 1 0.00 324 Table amended 0 0.0328 512 0.0384 600 2 625 625 325 Table amended 0 9 325 Table amended 9 0.0328 512 0.0384 600 2 250 0 15 300 0 15 300 0 11 10k 0 3 326 Table and note amended 9 Note: * Continuous trans The value set in BRF	Table amended 4.9152MHz Bit Rate Frror (bit/s) N (%) n 110 2 86 0.31 2 1200 3 11 0.00 2 200 3 11 0.00 2 200 3 11 0.00 2 200 3 1 0.00 2 300 3 7 0.00 2 600 3 3 0.00 0 1200 3 1 0.00 0 Maximum 0.0328 512.5 0.0384 600 2 2 62500 62500 325 Table amended Question of the second	Table amended 322 Table amended SMM Bit Rate SMM Bit Rate SMM 110 2 SMM 110 2 86 0.31 2 88 150 3 15 0.00 2 64 200 3 11 0.00 2 48 250 2 37 1.05 2 38 300 3 7 0.00 2 32 600 3 3 0.00 0 232 600 3 1 0.00 0 129 Maximum Bit Rate 0.0328 512.5 0.0384 600 2 62500 325 Table amended	322 Table amended 4.9152MHz SMHz Bit Rate Error n N Error ME 110 2 86 0.31 2 88 -0.25 150 3 15 0.00 2 64 0.16 200 3 11 0.00 2 32 -1.36 600 3 3 0.00 0 255 1.73 1200 3 1 0.00 0 129 0.16 324 Table amended OSC (MHz) Maximum Bit Rate (bit/s) 0.0328 512.5 0.0384 600 2 62500 325 Table amended \$\$\u0000 20 2.38 0 20 0 20 2.38 0 200 0 20 2.38 0 250 0 13 2.38 0 326 Table and note amended \$\$\u00000000000000	322 Table amended 322 Table amended 322 Table amended 323 Solution N Error M Error M (%) n N (%)	322 Table amended SMHz SMHz 6A Bit Rate Error n N (%) n N N N N N N N </td <td>322 Table amended SMHz SMHz 6MHz Bit Rate Fror N (%) n N Bit Rate Fror N % 6MHz 6MHz Bit Rate Fror N %</td> <td>322 Table amended 4.9152MHz 5MHz 6MHz Bit Rate Error n N (%) n N 6MHz 100 2 5MHz 6MHz 100 2 6MHz 100 2 288 0.025 2 100 -0.06 -0.06 -0.069 20 3 0.16 0 155 0.16 0.00 0 120 0.16 0 155 0.16 0.00 2 326 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0<!--</td--><td>322 Table amended MHz SMHz 6MHz Bit Rate Fror n N (%) n N <th <="" colspan="2" td=""><td>322 Table amended $\frac{4.9152MHz}{(bit/s) n N} \frac{5MHz}{(%) n N} \frac{5MHz}{(%) n N} \frac{6MHz}{(%) n N} \frac{6.144}{(%)} \frac{6.144}{2} \frac{6.144}{108} \frac{110 2 0.66 0.31 2 88 0.255 2 58 0.069 3 141}{150 3 15 0.00 2 64 0.16 2 77 0.16 3 19} \frac{100 0.02 2 48 0.255 2 58 0.069 3 141}{250 2 37 1.05 2 38 0.16 2 46 0.027 3 11} \frac{100 0.02 2 48 0.025 2 58 0.069 3 141}{250 3 3 0.00 0 2 32 -1.36 2 38 0.16 3 9} \frac{100 0.03 3 3 0.00 0 2 355 1.73 3 4 -2.34 3 4}{1200 3 1 0.00 0 0 129 0.16 0 155 0.16 2 9} \frac{100 0.0384 0.00 0 0 129 0.16 0 0 155 0.16 2 9}{120 0 0 0 0 0 0 0 0 0} \frac{129 0.16 0 0 155 0.16 2 9}{120 0 0 0 0 0 0} \frac{129 0.16 0 0 0 0 0}{12 0 0 0 0 0 0} \frac{129 0.16 0 0 0 0}{12 0 0 0 0 0 0} \frac{129 0.16 0 0 0}{12 0 0 0 0 0} \frac{129 0.16 0 0 0}{12 0 0 0 0 0} \frac{129 0.16 0 0 0}{12 0 0 0 0 0} \frac{129 0.16 0 0 0}{12 0 0 0 0 0} \frac{129 0.16 0 0 0}{12 0 0 0 0 0} \frac{129 0.16 0 0 0}{12 0 0 0 0 0} \frac{129 0.16 0 0 0}{12 0 0 0 0 0} \frac{129 0.00 0 0 0}{12 0 0 0 0 0} \frac{129 0.00 0 0 0}{12 0 0 0 0 0} \frac{129 0.00 0 0 0}{12 0 0 0 0 0} \frac{129 0.16 0 0 0}{12 0 0 0 0 0} \frac{129 0.16 0 0 0}{12 0 0 0 0 0} \frac{129 0.00 0 0}{12 0 0 0 0} \frac{129 0.00 0 0}{12 0 0 0 0} \frac{150 0.00 0}{15 0 0 0} \frac{110 0 0}{10 0 0} \frac{110 0}{10 0 0} \frac{110 0}{10 0} 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RENESAS

ltem	Page	Rev	isior	ı (Se	e Ma	nual	for Details	5)				
15.3.9 Serial Port	328	Table amended										
Control Register		Bit	Bit	Name	Initial Value	R/W	Description					
		3	SCI	VV3	0	R/W	TXD32 Pin Out	put Data Inversi	on Switch			
							Selects whethe TXD32 pin is in	r the polarity of verted or not.	output data o	fthe		
							0: Output data	of TXD32 pin is	not inverted.			
							1: Output data	of TXD32 pin is	inverted.			
		2	SCI	VV2	0	R/W	RXD32 Pin Inp	ut Data Inversio	n Switch			
							Selects whethe pin is inverted of	r the polarity of i or not.	input data of t	the RXD32		
							0: Output data	of RXD32 pin is	not inverted.			
							1: Output data	of RXD32 pin is	inverted.			
		1	SCI	NV1	0	R/W	TXD31 Pin Out	put Data Inversi	on Switch			
							Selects whethe TXD31 pin is in	r the polarity of verted or not.	output data o	fthe		
							0: Output data	of TXD31 pin is	not inverted.			
		0	0.01		0	DAA	1: Output data	of TXD31 pin is	inverted.			
		0	SCI	100	0	R/W	Selects whethe	r the polarity of i	n Switch	the RXD31		
							pin is inverted of	or not.				
							0: Input data of	0: Input data of RXD31 pin is not inverted.				
							1: Input data of	RXD31 pin is in	verted.			
15.4.1 Clock	332	Tab	le an	nend	ed							
Table 15.8 Data			SI	٨R			Serial Data Tra	nsfer Format and F	rame Length			
Transfer Formats		CHR	PE	MP	STOP	+ ¹ + ²	3 4 5	6 7 8	9 10	11 12		
(Asynchronous Mode)		0	0	1	0	i i		Setting prohibited				
(, logitoritorio de triodo)							+ + +					
		0	0	1	1		:	Setting prohibited				
			+							·		
		1	0	1	0			Setting prohibited				
									1 1			
		l	l	L	J'l							
Table 15.9 SMR	333	Tab	le an	nend	ed							
Settings and				SMI	3			Data 1	Fransfer For	mat		
Corresponding Data		Bit 7	Bit 6	Bit 2	Bit 5	Bit 3	Mode	Data Length	Parity Bit	Stop Bit		
Transfer Formats		0	0	1	0	0	Asynchronous	Setting		Length		
					-	1	-		Na	4.6.9		
					1	0	_	5-bit data	No	1 bit		
			1	_	0	0	_	Setting		2 bits		
					-	1	-	pronibited				
					1	0	_	5-bit data	Yes	1 bit		
						1				2 bits		
15.4.2 SCI3	335	Figu	ire ar	nen	hed							
Initialization	000	[4] V	Vait a	at lea	ast or	ne bit i	nterval. the	en set the	TE bit o	or RE bit in		
Figure 15.4 Sample		SCF	R to 1	Se	ttina	bits TI	E and RF	enables th		31 (TXD32)		
SCI3 Initialization		and	RXL	. 00	RXD	32) nir	ns to he us	ed Also	set the F	RIF TIF and	Ь	
Flowebart				-51 (ite	μι (Σ		ou. Aisu :			u	
		1 [[-	b	11 0 ,							

	11.4.3	TMOFH/TMOFL Output Timing	
	11.4.4	TCF Clear Timing	
	11.4.5	Timer Overflow Flag (OVF) Set Timing	
	11.4.6	Compare Match Flag Set Timing	
11.5	Timer	F Operating States	225
11.6	Usage 1	Notes	226
	11.6.1	16-Bit Timer Mode	
	11.6.2	8-Bit Timer Mode	
	11.6.3	Flag Clearing	
	11.6.4	Timer Counter (TCF) Read/Write	229
Sect	on 10	16 Dit Timor Dulco Unit (TDU)	221
		10-Dit Timer Puise Unit (TPU)	
12.1		Unitarit Ding	
12.2	Input/C	Duput Pins	
12.5		Timor Control Decistor (TCD)	
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RENESAS

		Pi	n No.				
_		FP-80A,		Pad	Pad		
Туре	Symbol	TFP-80C	TLP-85V	No.*'	No.* ²	I/O	Functions
LCD controller/ driver	COM1 to COM4	27 to 30	J4, K5, H5, J6	28 to 31	27 to 30	Output	LCD common output pins.
	SEG1 to SEG8	31 to 38	J5, H6, H7, K6, J7, J8, K7, H8	32 to 39	31 to 38	Output	LCD segment output pins.
	SEG9 to SEG16	39 to 46	K9, K8, J10 H10, J9, H9, G8	40 to 47	39 to 46	Output	-
	SEG17 to SEG24	47 to 54	G9, F10, F8, E9, F9, E8, D8, E10	48 to 55	47 to 54	Output	-
	SEG25 to SEG32	55 to 62	D9, C9, D10, C8, B10, C10, A9, A8	56 to 63	55 to 62	Output	
I/O ports	P10 to P12	78 to 80	C3, A2, A3	79 to 81	78 to 80	I/O	7-bit I/O pins. Input or output can be designated for each bit by means of
	P13 to P16	1 to 4	B1, C1, B2, C2	1 to 4	1 to 4	_	the port control register 1 (PCR1).
	P30 to P32, P36, P37	5 to 9	D1, D3, D2, E1, E3	5 to 9	5 to 9	I/O	5-bit I/O pins. Input or output can be designated for each bit by means of the port control register 3 (PCR3).
	P40 to P42	18 to 20	H3, J1, H1	19 to 21	18 to 20	I/O	3-bit I/O pins. Input or output can be designated for each bit by means of the port control register 4 (PCR4).
	P50 to P57	31 to 38	J5, H6, H7, K6, J7, J8, K7, H8	32 to 39	31 to 38	I/O	8-bit I/O pins. Input or output can be designated for each bit by means of the port control register 5 (PCR5).
	P60 to P67	39 to 46	K9, K8, J10, H10, J9, H9, G10, G8	40 to 47	39 to 46	I/O	8-bit I/O pins. Input or output can be designated for each bit by means of the port control register 6 (PCR6).

Renesas



Figure 2.4 Relationship between Stack Pointer and Stack Area

2.2.2 Program Counter (PC)

This 24-bit counter indicates the address of the next instruction the CPU will execute. The length of all CPU instructions is 2 bytes (one word), so the least significant PC bit is ignored. (When an instruction is fetched, the least significant PC bit is regarded as 0). The PC is initialized when the start address is loaded by the vector address generated during reset exception-handling sequence.

2.2.3 Condition-Code Register (CCR)

This 8-bit register contains internal CPU status information, including an interrupt mask bit (I) and half-carry (H), negative (N), zero (Z), overflow (V), and carry (C) flags. The I bit is initialized to 1 by reset exception-handling sequence, but other bits are not initialized.

Some instructions leave flag bits unchanged. Operations can be performed on the CCR bits by the LDC, STC, ANDC, ORC, and XORC instructions. The N, Z, V, and C flags are used as branching conditions for conditional branch (Bcc) instructions.

For the action of each instruction on the flag bits, see Appendix A.1, Instruction List.

2.4.2 Basic Instruction Formats

H8/300H CPU instructions consist of 2-byte (1-word) units. An instruction consists of an operation field (op), a register field (r), an effective address extension (EA), and a condition field (cc).

Figure 2.7 shows examples of instruction formats.

(1) **Operation Field**

Indicates the function of the instruction, the addressing mode, and the operation to be carried out on the operand. The operation field always includes the first four bits of the instruction. Some instructions have two operation fields.

(2) Register Field

Specifies a general register. Address registers are specified by 3 bits, and data registers by 3 bits or 4 bits. Some instructions have two register fields. Some have no register field.

(3) Effective Address Extension

8, 16, or 32 bits specifying immediate data, an absolute address, or a displacement. A24-bit address or displacement is treated as a 32-bit data in which the first 8 bits are 0 (H'00).

(4) Condition Field

Specifies the branching condition of Bcc instructions.



Figure 2.7 Instruction Formats

6.2.1 Sleep Mode

In sleep mode, CPU operation is halted but the system clock oscillator, subclock oscillator, and on-chip peripheral modules function. In sleep (medium-speed) mode, the on-chip peripheral modules function at the clock frequency set by the MA1 and MA0 bits in SYSCR1. CPU register contents are retained.

Sleep mode is cleared by an interrupt. When an interrupt is requested, sleep mode is cleared and interrupt exception handling starts. Sleep mode is not cleared if the I bit in CCR is set to 1 or the requested interrupt is disabled by the interrupt enable bit. After sleep mode is cleared, a transition is made from sleep (high-speed) mode to active (high-speed) mode or from sleep (medium-speed) mode to active (medium-speed) mode.

When the $\overline{\text{RES}}$ pin goes low, the CPU goes into the reset state and sleep mode is cleared. Since an interrupt request signal is synchronous with the system clock, the maximum time of $2/\phi$ (s) may be delayed from the point at which an interrupt request signal occurs until the interrupt exception handling is started.

Furthermore, it sometimes operates with half state early timing at the time of transition to sleep (medium-speed) mode.

6.2.2 Standby Mode

In standby mode, the system clock oscillator stops, so the CPU and on-chip peripheral modules stop functioning when the WDT disables the on-chip oscillator operation. However, as long as the rated voltage is supplied, the contents of CPU registers, on-chip RAM, and some on-chip peripheral module registers are retained. On-chip RAM contents will be retained as long as the voltage set by the RAM data retention voltage is provided. The I/O ports go to the high-impedance state.

Standby mode is cleared by an interrupt. When an interrupt is requested, the system clock pulse generator starts. After the time set in bits STS2 to STS0 in SYSCR1 has elapsed, standby mode is cleared and interrupt exception handling starts. After standby mode is cleared, a transition is made to active (high-speed) or active (medium-speed) mode according to the MSON bit in SYSCR2. Standby mode is not cleared if the I bit in CCR is set to 1 or the requested interrupt is disabled by the interrupt enable bit.

When the $\overline{\text{RES}}$ pin goes low, the system clock oscillator starts. Since system clock signals are supplied to the entire chip as soon as the system clock oscillator starts functioning, the $\overline{\text{RES}}$ pin must be kept low until the system clock oscillator output stabilizes (except when the power-on

6.3.4 Direct Transition from Active (Medium-Speed) Mode to Subactive Mode

The time from the start of SLEEP instruction execution to the end of interrupt exception handling (the direct transition time) is calculated by equation (4).

Direct transition	n time = {(Number of SLEEP instruction execution states) + (Number of internal
	processing states) $\} \times ($ tcyc before transition $) + ($ Number of interrupt
	exception handling execution states) × (tsubcyc after transition)
	(4)
Example:	When ϕ osc/8 is selected as the CPU operating clock before transition
	Direct transition time = $(2 + 1) \times 8$ tosc + 14×1 tsubcyc = 24 tosc + 14 tsubcyc

[Legend] tosc: OSC clock cycle time tsubcyc: Subclock (ϕ_{SUB}) cycle time

6.3.5 Direct Transition from Subactive Mode to Active (High-Speed) Mode

The time from the start of SLEEP instruction execution to the end of interrupt exception handling (the direct transition time) is calculated by equation (5).

Direct transition time = {(Number of SLEEP instruction execution states) + (Number	er of internal
processing states) $\} \times ($ tsubcyc before transition) + {(Wait ti	me set in bits
STS2 to STS0) + (Number of interrupt exception handling e	execution
states)} \times (tcyc after transition)	

.....(5)

Example: When $\phi w/8$ is selected as the CPU operating clock before transition and wait time = 8192 states

Direct transition time = $(2 + 1) \times 8tw + (8192 + 14) \times tosc = 24tw + 8206tosc$

[Legend] tosc: OSC clock cycle time tw: Watch clock cycle time tcyc: System clock (ϕ) cycle time tsubcyc: Subclock (ϕ_{SUB}) cycle time

9.9 Port A

Port A is an I/O port also functioning as an LCD common output pin. Figure 9.9 shows its pin configuration.



Figure 9.9 Port A Pin Configuration

Port A has the following registers.

- Port data register A (PDRA)
- Port control register A (PCRA)

9.9.1 Port Data Register A (PDRA)

PDRA is a register that stores data of port A.

		Initial		
Bit	Bit Name	Value	R/W	Description
7 to 4	_	All 1		Reserved
				These bits are always read as 1 and cannot be modified.
3	PA3	0	R/W	If port A is read while PCRA bits are set to 1, the values
2	PA2	0	R/W	stored in PDRA are read, regardless of the actual pin
1	PA1	0	R/W	the pin states are read.
0	PA0	0	R/W	





15.4.1 Clock

Either an internal clock generated by the on-chip baud rate generator or an external clock input at the SCK31 (SCK32) pin can be selected as the SCI3's serial clock source, according to the setting of the COM bit in SMR and the CKE0 and CKE1 bits in SCR. When an external clock is input at the SCK31 (SCK32) pin, the clock frequency should be 16 times the bit rate used. For details on selection of the clock source, see table 15.10. When the SCI3 is operated on an internal clock, the clock can be output from the SCK31 (SCK32) pin. The frequency of the clock output in this case is equal to the bit rate, and the phase is such that the rising edge of the clock is in the middle of the transfer data, as shown in figure 15.3.



Figure 15.3 Relationship between Output Clock and Transfer Data Phase (Asynchronous Mode) (Example with 8-Bit Data, Parity, Two Stop Bits)



Section 19 LCD Controller/Driver

This LSI has an on-chip segment-type LCD control circuit, LCD driver, and power supply circuit, enabling it to directly drive an LCD panel.

19.1 Features

• Display capacity

Duty Cycle	Internal Driver
Static	32 SEG
1/2	32 SEG
1/3	32 SEG
1/4	32 SEG

- LCD RAM capacity
 8 bits × 16 bytes (128 bits)
- Word access to LCD RAM
- The segment output pins can be used as ports. SEG32 to SEG1 pins can be used as ports in groups of four.
- Common output pins not used because of the duty cycle can be used for common doublebuffering (parallel connection).

With 1/2 duty, parallel connection of COM1 to COM2, and of COM3 to COM4, can be used In static mode, parallel connection of COM1 to COM2, COM3, and COM4 can be used

- Choice of 11 frame frequencies
- A or B waveform selectable by software
- On-chip power supply split-resistor
- Display possible in operating modes other than standby mode
- On-chip 3-V constant-voltage power supply circuit

This power circuit can constantly supply 3 V to LCD drive power supply without using Vcc voltage.

- Output of the 3-V constant-voltage power supply circuit adjustable
- Use of module standby mode enables this module to be placed in standby mode independently when not used. (For details, refer to section 6.4, Module Standby Function.)



Figure 20.2 External Circuit Connections of I/O Pins

20.2 Input/Output Pins

Table 20.1 summarizes the input/output pins used by the I^2C bus interface 2.

Table 20.1 Pin Configuration

Name	Abbreviation	I/O	Function
Serial clock pin	SCL	I/O	IIC serial clock input/output
Serial data pin	SDA	I/O	IIC serial data input/output



24.2.3 AC Characteristics

Table 24.3 lists the control signal timing, table 24.4 lists the serial interface timing, and table 24.5 lists the I^2C bus interface timing.

Table 24.3 Control Signal Timing

 $V_{cc} = 1.8 \text{ V}$ to 3.6 V, $AV_{cc} = 1.8 \text{ V}$ to 3.6 V, $V_{ss} = AV_{ss} = 0.0 \text{ V}$, unless otherwise specified.

		Applicable			Values			Reference		
Item	Symbol	Pins	Test Condition	Min.	Тур.	Max.	Unit	Figure		
System clock oscillation frequency	f _{osc}	OSC1, OSC2	V_{cc} = 2.7 to 3.6 V	2.0	_	10.0	MHz			
			V_{cc} = 1.8 to 3.6 V	2.0		4.2	-			
OSC clock ($\varphi_{\rm osc}$) cycle time	t _{osc}	OSC1, OSC2	V_{cc} = 2.7 to 3.6 V	100	_	500 (1000)	ns	Figure 24.2 *2		
			V_{cc} = 1.8 to 3.6 V	238	_	500 (1000)	_			
System clock (t _{cyc}			1	_	64	t _{osc}			
time				_	_	64	μs	-		
Subclock oscillation frequency	f _w	X1, X2		_	32.768 or 38.4	_	kHz			
Watch clock (φ_{w}) cycle time	t _w	X1, X2		_	30.5 or 26.0	_	μs	Figure 24.2		
Subclock ($\phi_{_{SUB}}$) cycle time	t _{subcyc}			2	_	8	t _w	* ¹		
Instruction cycle time				2	—	_	t _{cyc} t _{subcyc}			
Oscillation stabilization time	t _{rc}	OSC1, OSC2	Crystal resonator (V_{cc} = 2.7 to 3.6 V)	_	0.8	2.0	ms			
			Crystal resonator (V_{cc} = 2.2 to 3.6 V)	_	1.2	3	_			
			Ceramic resonator (V_{cc} = 2.2 to 3.6 V)	_	20	45	μs			
			Ceramic resonator (other than above)	_	80	_	_			
			Other than above	_	_	50	ms			
		×1, ×2	$V_{cc} = 2.2 \text{ to } 3.6 \text{ V}$	_	_	2.0	s	Figure 5.7		
			Other than above	_	4	_				



		Applicable			Values	5		Reference
ltem	Symbol	Pins	Test Condition	Min.	Тур.	Max.	Unit	Figure
Oscillation stabilization time	t _{rc}	OSC1, OSC2	Crystal resonator V_{cc} = 2.7 to 3.6 V	_	0.8	2.0	ms	
			Crystal resonator V_{cc} = 2.2 to 3.6 V	_	1.2	3.0		
			Ceramic resonator V_{cc} = 2.2 to 3.6 V	_	20	45	μs	
			Ceramic resonator Other than above	_	80	_		
			Other than above	_	_	50	ms	
			When on-chip oscillator is selected	_	_	100	μs	*4
		X1, X2	V_{cc} = 2.2 to 3.6 V	_	_	2.0	s	Figure 5.7
			Other than above	_	4	_		
External clock high	t _{cph}	OSC1	$\rm V_{cc}$ = 2.7 to 3.6 V	40	_		ns	Figure 24.2
width			$V_{\rm cc}$ = 1.8 to 3.6 V	95	_	_	_	
		X1		_	15.26 or 13.02	—	μs	
External clock low	t _{cpl}	OSC1	$V_{\rm cc}$ = 2.7 to 3.6 V	40	_	_	ns	Figure 24.2
width			V_{cc} = 1.8 to 3.6 V	95	_	_		
		X1		_	15.26 or 13.02	_	μs	_
External clock rise	t _{cPr}	OSC1	V_{cc} = 2.7 to 3.6 V	_	_	10	ns	Figure 24.2
time			V_{cc} = 1.8 to 3.6 V	_	_	24	_	
		X1		_	_	55.0	ns	
External clock fall time	t _{cPf}	OSC1	V_{cc} = 2.7 to 3.6 V	_	_	10	ns	Figure 24.2
			V_{cc} = 1.8 to 3.6 V	_	_	24	_	
		X1		_	_	55.0	ns	
RES pin low width	t _{REL}	RES		10	_	_	t _{cyc}	Figure 24.3*3

Mnemonic			Addressing Mode and Instruction Length (bytes)							nd /tes)								No Stat	. of es ^{*1}	
		perand Size	x	5	0ERn	@(d, ERn)	0-ERn/@ERn+	0aa	@(d, PC)	0 @ aa		Operation		Con	ditio	n Co	ode		lormal	dvanced	
			#	E						•				н	N	∠ ↑	v	C	~	4	
DEC	DEC.L #1, ERd			2								ER032-1 \rightarrow ER032	-	-	↓	↓	↓	_	2	2	
	DEC.L #2, ERd	L		2								$ERd32-2 \rightarrow ERd32$	_	-		↓	4	-	2	2	
DAS	DAS.Rd	В		2								Rd8 decimal adjust \rightarrow Rd8	_	*	Ţ	Ţ	*	_	2	2	
MULXU	MULXU. B Rs, Rd	В		2								$Rd8 \times Rs8 \rightarrow Rd16$ (unsigned multiplication)	-	-	-	-	—	-	1	4	
	MULXU. W Rs, ERd	W		2								$Rd16 \times Rs16 \rightarrow ERd32$ (unsigned multiplication)	-	-	-	-	—	-	2	2	
MULXS	MULXS. B Rs, Rd	В		4								$Rd8 \times Rs8 \rightarrow Rd16$ (signed multiplication)		-	\$	\$	—	-	1	6	
	MULXS. W Rs, ERd	W		4								$Rd16 \times Rs16 \rightarrow ERd32$ (signed multiplication)		-	\$	\$	—	-	2	4	
DIVXU	DIVXU. B Rs, Rd	В		2								Rd16 ÷ Rs8 → Rd16 (RdH: remainder, RdL: quotient) (unsigned division)		_	(6)	(7)	_		1	4	
	DIVXU. W Rs, ERd	w		2								ERd32 ÷ Rs16 → ERd32 (Ed: remainder, Rd: quotient) (unsigned division)		-	(6)	(7)	_	_	2	2	
DIVXS	DIVXS. B Rs, Rd	В		4								Rd16 ÷ Rs8 → Rd16 (RdH: remainder, RdL: quotient) (signed division)	—	_	(8)	(7)	_		1	6	
	DIVXS. W Rs, ERd	W		4								$ERd32 \div Rs16 \rightarrow ERd32$ (Ed: remainder, Rd: quotient) (signed division)			(8)	(7)	_		24		
CMP	CMP.B #xx:8, Rd	В	2									Rd8–#xx:8	—	\$	\$	\$	\$	\$	i 2		
	CMP.B Rs, Rd	В		2								Rd8–Rs8	—	\$	\$	\$	\uparrow	\$	2	2	
	CMP.W #xx:16, Rd	W	4									Rd16–#xx:16	—	(1)	\$	\$	\updownarrow	\$	4	4	
	CMP.W Rs, Rd	W		2								Rd16–Rs16	_	(1)	\$	\$	\$	\$	2	2	
	CMP.L #xx:32, ERd	L	6									ERd32-#xx:32	-	(2)	\$	\$	\$	\$	4	4	
	CMP.L ERs, ERd	L		2								ERd32–ERs32	-	(2)	\$	\$	\$	\$	2	2	

A.4 Combinations of Instructions and Addressing Modes

Table A.5 Combinations of Instructions and Addressing Modes

						Α	ddres	sing	Mode					
Functions	Instructions	XX#	Rn	@ERn	@(d:16.ERn)	@(d:24.ERn)	@ERn+/@ERn	@ aa:8	@aa:16	@ aa:24	@(d:8.PC)	@(d:16.PC)	@ @aa:8	
Data	MOV	BWL	BWL	BWL	BWL	BWL	BWL	В	BWL	BWL	_	_	—	_
transfer	POP, PUSH	-	_	_	—	_	_	_	_	-	_	_	—	WL
instructions	MOVFPE,	-	_	_	—	_	_	_	_	-	_	_	—	_
	MOVTPE													
Arithmetic	ADD, CMP	BWL	BWL	-	—	—	_	_	-	-	_	—	—	_
operations	SUB	WL	BWL	_	—	—	—	—	_	—	—	—	—	—
	ADDX, SUBX	В	В	_	—	—	—	—	_	—	_	—	—	—
	ADDS, SUBS	-	L	_	—	_	—	—	_	—	_	—	—	—
	INC, DEC	_	BWL	_	—	_	—	_	_	—	_	—	—	—
	DAA, DAS	_	В	_	—	_	—	_	_	—	_	—	—	—
	MULXU,	_	BW	_	—	_	_	_	_	_	_	_	_	_
	MULXS,													
	DIVXU,													
	DIVXS													
	NEG	—	BWL	—	—		—	—	_	—	—	—	—	—
	EXTU, EXTS	—	WL	—	—		—	—	_	—	—	—	—	—
Logical	AND, OR, XOR	—	BWL	-	—	—	—	_	-	-	—	—	—	—
operations	NOT	-	BWL	-	-	—	—	_	-	-	—	-	—	—
Shift operation	ons	—	BWL	-	—	—	—	—	—	—	—	—	—	—
Bit manipulat	tions	—	В	В	—	—	—	В	—	—	—	—	—	—
Branching	BCC, BSR	—	—	—	—	—	—	—	—	—	—	—	—	—
instructions	JMP, JSR	_	—	$ \circ $	—	—	—	_	—	—	0	\circ	—	—
	RTS	—	—	—	—	_	—	—	—	0	—	—	\bigcirc	—
System	RTE	-	—	—	—	—	—	—	—	—	—	—	—	\bigcirc
control	SLEEP	—	—	—	—	_	—	—	—	—	—	—	—	\bigcirc
Instructions	LDC	В	В	W	W	W	W	—	W	W	—	—	—	\bigcirc
	STC	—	В	W	W	W	W	—	W	W	—	—	—	—
	ANDC, ORC, XORC	В	-	-	-	-	-	-	-	-	-	-	-	-
	NOP	—	—	—	—	—	_	_	—	—	_	—	—	0
Block data tra	ansfer instructions	-	-	-	-	-	—	—	-	-	-	-	-	BW





Figure B.2 (e) Port 3 Block Diagram (P32)