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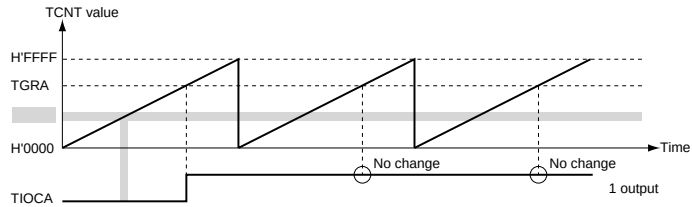
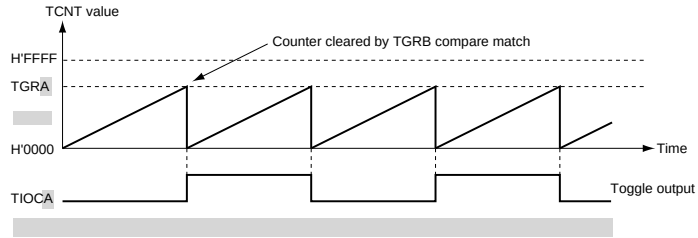
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8/300H
Core Size	16-Bit
Speed	4MHz
Connectivity	I²C, IrDA, SCI
Peripherals	LCD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	52KB (52K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38076rw4v

Item	Page	Revision (See Manual for Details)
12.4.2 8-Bit Registers	248	Description amended Registers other than TCNT and TGR are 8-bit. ... Examples of 8-bit register access operation are shown in figures 12.3 and 12.4.
Figure 12.5 8-Bit Register Access Operation [CPU ↔ TCR and TMDR (16 Bits)]		Deleted
12.5.1 Basic Functions (2) Waveform Output by Compare Match	252	Description amended Figure 12.9 shows an example of 1 output. … and settings have been made such that 1 is output by compare match A. ...
Figure 12.9 Example of 1 Output Operation	253	Figure title and figure amended 
	253	Description amended In this example, TCNT has been designated as a periodic counter (with counter clearing on compare match A), and settings have been made such that the output is toggled by compare match A.
Figure 12.10 Example of Toggle Output Operation		Figure amended 

- On-chip memory

Product Classification		Model	ROM	RAM
Flash memory version (F-ZTAT™ version)	H8/38076RF	HD64F38076R	52 kbytes*	2 kbytes
Masked ROM version	H8/38076R	HD64338076R	48 kbytes	2 kbytes
	H8/38075R	HD64338075R	40 kbytes	2 kbytes
	H8/38074R	HD64338074R	32 kbytes	1 kbyte
	H8/38073R	HD64338073R	24 kbytes	1 kbyte

Note: F-ZTAT™ is a trademark of Renesas Technology Corp.

* 4-kbyte area of 52-kbyte ROM is used for the on-chip debugging emulator. When the on-chip debugging emulator is not used, 52-kbyte area is available.

- General I/O ports
  I/O pins: 55 I/O pins, including 4 large current ports (I_{OL} = 15 mA, @V_{OL} = 1.0 V)
  Input-only pins: 8 input pins
- Supports various power-down states
- Compact package

Package	Code	Old Code	Body Size	Pin Pitch	Remarks
QFP-80	PRQP0080JB-A	FP-80A	14 × 14 mm	0.65 mm	
TQFP-80	PTQP0080KC-A	TFP-80C	12 × 12 mm	0.5 mm	
P-TFLGA-85	PTLG0085JA-A	TLP-85V	7 × 7 mm	0.65 mm	

Type	Symbol	Pin No. FP-80A, TFP-80C	Pin No. TLP-85V	Pad No.*[1]	Pad No.*[2]	I/O	Functions
Serial communication interface 4 (SCI4) (F-ZTAT version only)	SCK4	4	C2	4	—	I/O	Transfer clock pins for SCI4 data transmission/reception. When the E7 or on-chip emulator debugger is used, this pin is not available.
	SI4	8	E1	8	—	Input	SCI4 data input pins. When the E7 or on-chip emulator debugger is used, this pin is not available.
	SO4	9	E3	9	—	Output	SCI4 data output pins. When the E7 or on-chip emulator debugger is used, this pin is not available.
Serial communication interface 3 (SCI3)	SCK31	18	H3	19	18	I/O	SCI3_1 clock I/O pins.
	RXD31/ IrRXD	19	J1	20	19	Input	SCI3_1 data input pins or data input pins for the IrDA format.
	TXD31/ IrTXD	20	H1	21	20	Output	SCI3_1 data output pins or data output pins for the IrDA format.
	SCK32	5	D1	5	5	I/O	SCI3_2 clock I/O pins.
	RXD32	6	D3	6	6	Input	SCI3_2 data input pins.
	TXD32	7	D2	7	7	Output	SCI3_2 data output pins.
A/D converter	AN0 to AN2	70 to 68	B5, C6, A6	71 to 69	70 to 68	Input	Analog data input pins for the A/D converter.
	AN3 to AN7*[4]	67 to 63	B7, C7, A7, B8, B9	68 to 64	67 to 63	Input	
	$\overline{\text{ADTRG}}$	15	G2	16	15	Input	External trigger input pins for the A/D converter.
I^2C bus interface 2 (IIC2)	SDA	6	D3	6	6	I/O	IIC data I/O pins.
	SCL	7	D2	7	7	I/O	IIC clock I/O pins.

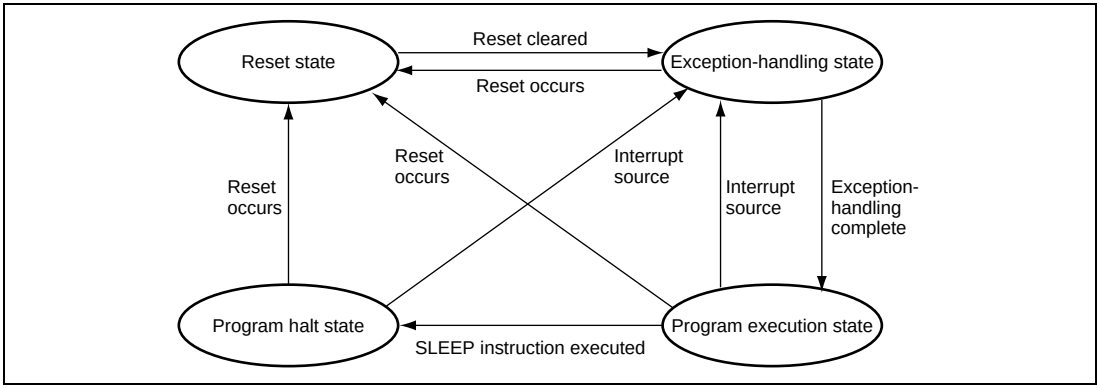


Figure 2.12 State Transitions

2.8 Usage Notes

2.8.1 Notes on Data Access to Empty Areas

The address space of this LSI includes empty areas in addition to the ROM, RAM, and on-chip I/O registers areas available to the user. When data is transferred from CPU to empty areas, the transferred data will be lost. This action may also cause the CPU to malfunction. When data is transferred from an empty area to CPU, the contents of the data cannot be guaranteed.

2.8.2 EEPMOV Instruction

EEPMOV is a block-transfer instruction and transfers the byte size of data indicated by R4L, which starts from the address indicated by R5, to the address indicated by R6. Set R4L and R6 so that the end address of the destination address (value of R6 + R4L) does not exceed H'FFFF (the value of R6 must not change from H'FFFF to H'0000 during execution).

4.3.4 Interrupt Enable Register 2 (IENR2)

IENR2 enables the direct transition, A/D converter, timer F, and asynchronous event counter interrupts.

Bit	Bit Name	Initial Value	R/W	Description
7	IENDT	0	R/W	Direct Transition Interrupt Request Enable The direct transition interrupt request is enabled when this bit is set to 1.
6	IENAD	0	R/W	A/D Converter Interrupt Request Enable The A/D converter interrupt request is enabled when this bit is set to 1.
5	—	0	R/W	Reserved This bit is read/write enable reserved bit.
4	—	1	R/W	Reserved This bit is always read as 1.
3	IENTFH	0	R/W	Timer FH Interrupt Request Enable The timer FH interrupt request is enabled when this bit is set to 1.
2	IENTFL	0	R/W	Timer FL Interrupt Request Enable The timer FL interrupt request is enabled when this bit is set to 1.
1	—	1	R/W	Reserved This bit is always read as 1.
0	IENEC	0	R/W	Asynchronous Event Counter Interrupt Request Enable The asynchronous event counter interrupt request is enabled when this bit is set to 1.

5.5.2 Notes on Board Design

When using a crystal resonator (ceramic resonator), place the resonator and its load capacitors as close as possible to the OSC1 and OSC2 pins. Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 5.11).

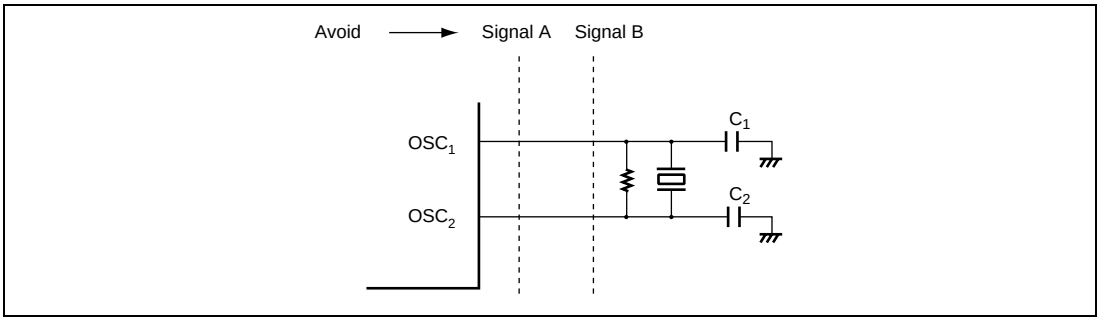


Figure 5.11 Example of Incorrect Board Design

Note: When a crystal resonator or ceramic resonator is connected, consult with the crystal resonator and ceramic resonator manufacturers to determine the circuit constants because the constants differ according to the resonator, stray capacitance of the mounting circuit, and so on.

5.5.3 Definition of Oscillation Stabilization Wait Time

Figure 5.12 shows the oscillation waveform (OSC2), system clock (ϕ), and microcomputer operating mode when a transition is made from standby mode, watch mode, or subactive mode, to active (high-speed/medium-speed) mode, with an resonator connected to the system clock oscillator.

As shown in figure 5.12, when a transition is made from a mode in which the system clock oscillator is halted to active (high-speed/medium-speed) mode, the sum of the following two times (oscillation start time and wait time) is required.

(1) Oscillation Start Time

The time from the point at which the system clock oscillator oscillation waveform starts to change when an interrupt is generated, until generation of the system clock starts.

Table 6.2 Transition Mode after SLEEP Instruction Execution and Interrupt Handling

State Before Transition	LSON	MSON	SSBY	TMA3	DTON	Transition Mode after SLEEP Instruction Execution	Transition Mode due to Interrupt	Symbol in Figure 6.1
Active (high-speed) mode	0	0	0	*	0	Sleep (high-speed) mode	Active (high-speed) mode	a
	0	1	0	*	0	Sleep (medium-speed) mode	Active (medium-speed) mode	b
	0	0	1	0	0	Standby mode	Active (high-speed) mode	d
	0	1	1	0	0	Standby mode	Active (medium-speed) mode	d
	0	0	1	1	0	Watch mode	Active (high-speed) mode	e
	0	1	1	1	0	Watch mode	Active (medium-speed) mode	e
	1	*	1	1	0	Watch mode	Subactive mode	e
	0	0	0	*	1	Active (high-speed) mode (direct transition)	—	—
	0	1	0	*	1	Active (medium-speed) mode (direct transition)	—	g
	1	*	1	1	1	Subactive mode (direct transition)	—	i

- P14/TIOCA2/TCLKC pin

  The pin function is switched as shown below according to the combination of the TPU channel 2 setting by the MD1 and MD0 bits in TMDR_2, IOA3 to IOA0 bits in TIOR_2, and CCLR1 and CCLR0 bits in TCR_2, the TPSC2 to TPSC0 bits in TCR_2, and the PCR14 bit in PCR1.

TPU Channel 2 Setting	Next table (1)	Next table (2)	
PCR14	—	0	1
Pin Function	TIOCA2 output pin	P14 input pin	P14 output pin
		TIOCA2 input pin*[1]	
	TCLKC input pin*[2]		

Notes: 1. When the MD1 and MD0 bits are set to B'00 and the IOA3 bit to 1, the pin function becomes the TIOCA2 input pin.
Clear PCR14 to 0 when using TIOCA2 as an input pin.

2. When the TPSC2 to TPSC0 bits in TCR_2 are set to B'110, the pin function becomes the TCLKC input pin.
Clear PCR14 to 0 when using TCLKC as an input pin.

TPU Channel 2 Setting	(2)	(1)	(2)	(1)	(1)	(2)
MD1, MD0	B'00		B'1x	B'10	B'11	
IOA3 to IOA0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00	Other than B'xx00	
CCLR1, CCLR0	—	—	—	—	Other than B'01	B'01
Output Function	—	Output compare output	—	PWM mode 1* output	PWM mode 2 output	—

[Legend] x: Don't care.

Note: * The output of the TIOCB2 pin is disabled.

- P11/AEVL pin

  The pin function is switched as shown below according to the combination of the AEVL bit in PMR1 and PCR11 bit in PCR.

AEVL	0		1
PCR11	0	1	x
Pin Function	P11 input pin	P11 output pin	AEVL input pin

[Legend] x: Don't care.

- P10/AEVH pin

  The pin function is switched as shown below according to the combination of the AEVH bit in PMR1 and PCR10 bit in PCR.

AEVH	0		1
PCR10	0	1	x
Pin Function	P10 input pin	P10 output pin	AEVH input pin

[Legend] x: Don't care.

9.1.6 Input Pull-Up MOS

Port 1 has an on-chip input pull-up MOS function that can be controlled by software. When a PCR1 bit is cleared to 0, setting the corresponding PUCR1 bit to 1 turns on the input pull-up MOS for that pin. The input pull-up MOS function is in the off state after a reset.

(n = 6 to 0)

PCR1n	0		1
PUCR1n	0	1	x
Input Pull-Up MOS	Off	On	Off

[Legend] x: Don't care.

9.9 Port A

Port A is an I/O port also functioning as an LCD common output pin. Figure 9.9 shows its pin configuration.

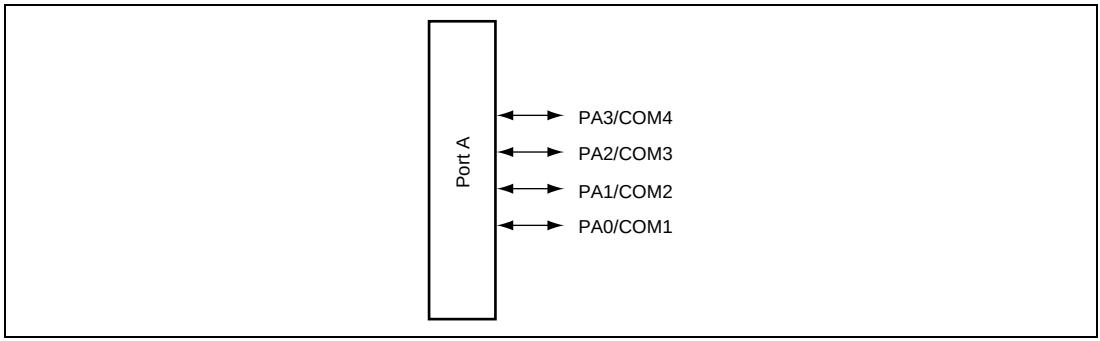


Figure 9.9 Port A Pin Configuration

Port A has the following registers.

- Port data register A (PDRA)
- Port control register A (PCRA)

9.9.1 Port Data Register A (PDRA)

PDRA is a register that stores data of port A.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 1	—	Reserved These bits are always read as 1 and cannot be modified.
3	PA3	0	R/W	If port A is read while PCRA bits are set to 1, the values stored in PDRA are read, regardless of the actual pin states. If port A is read while PCRA bits are cleared to 0, the pin states are read.
2	PA2	0	R/W	
1	PA1	0	R/W	
0	PA0	0	R/W	

10.3.5 RTC Control Register 1 (RTCCR1)

RTCCR1 controls start/stop and reset of the clock timer. For the definition of time expression, see figure 10.2.

Bit	Bit Name	Initial Value	R/W	Description
7	RUN	—	R/W	RTC Operation Start 0: Stops RTC operation 1: Starts RTC operation
6	12/24	—	R/W	Operating Mode 0: RTC operates in 12-hour mode. RHRDR counts on 0 to 11. 1: RTC operates in 24-hour mode. RHRDR counts on 0 to 23.
5	PM	—	R/W	A.m./P.m. 0: Indicates a.m. when RTC is in the 12-hour mode. 1: Indicates p.m. when RTC is in the 12-hour mode.
4	RST	0	R/W	Reset 0: Normal operation 1: Resets registers and control circuits except RTCCSR and this bit. Clear this bit to 0 after having been set to 1.
3	—	0	R/W*	Reserved
2 to 0	—	All 0	—	Reserved These bits are always read as 0.

Note: * Only 0 can be written to this bit.

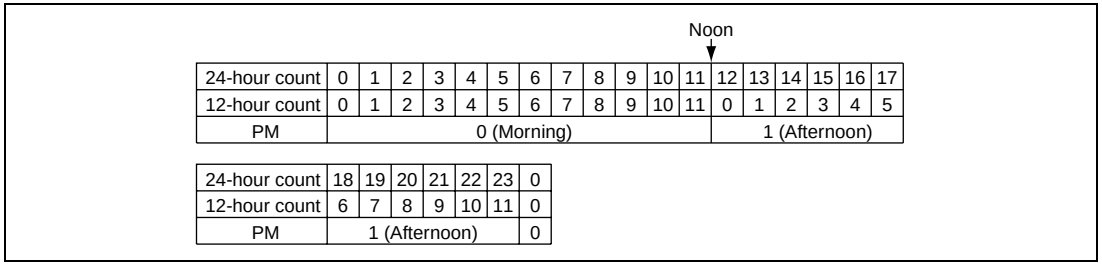


Figure 10.2 Definition of Time Expression

Note: Ndr and Ncm above must be set so that Ndr < Ncm. If the settings do not satisfy this condition, the output of the event counter PWM is fixed low.

Table 13.2 Examples of Event Counter PWM Operation

Conditions: fosc = 4 MHz, fϕ = 4 MHz, high-speed active mode, ECPWCR value (Ncm) = H'7A11, ECPWDR value (Ndr) = H'16E3

Clock Source Selection	Clock Source Cycle (T)*	ECPWCR Value (Ncm)	ECPWDR Value (Ndr)	toff = T × (Ndr + 1)	tcm = T × (Ncm + 1)	ton = tcm – toff
ϕ/2	0.5 µs	H'7A11	H'16E3	2.92975 ms	15.625 ms	12.69525 ms
ϕ/4	1 µs	D'31249	D'5859	5.85975 ms	31.25 ms	25.39025 ms
ϕ/8	2 µs			11.71975 ms	62.5 ms	50.78025 ms
ϕ/16	4 µs			23.43975 ms	125.0 ms	101.56025 ms
ϕ/32	8 µs			46.87975 ms	250.0 ms	203.12025 ms
ϕ/64	16 µs			93.75975 ms	500.0 ms	406.24025 ms

Note: * toff minimum width

13.4.5 Operation of Clock Input Enable/Disable Function

The clock input to the event counter can be controlled by the IRQAEC pin when ECPWME in AEGSR is 0, and by the event counter PWM output, IECPWM when ECPWME in AEGSR is 1. As this function forcibly terminates the clock input by each signal, a maximum error of one count will occur depending on the IRQAEC or IECPWM timing. Figure 13.5 shows an example of the operation.

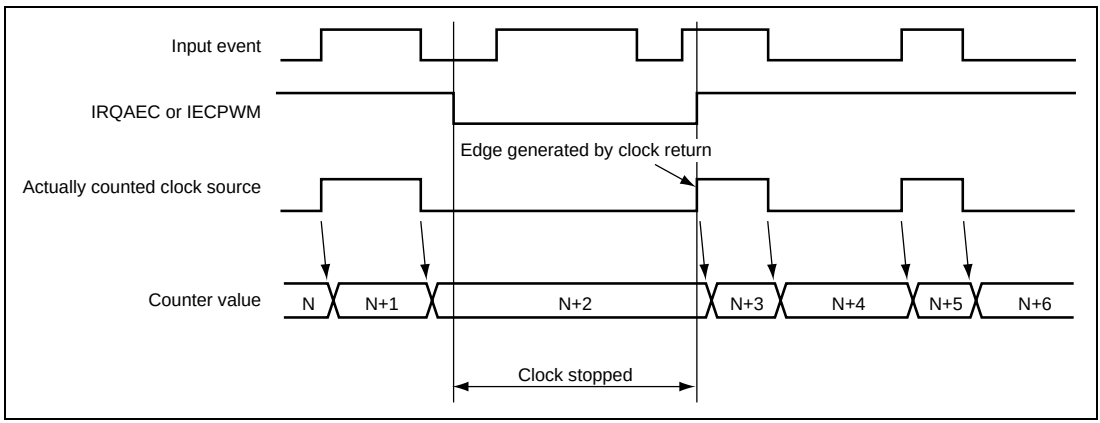


Figure 13.5 Example of Clock Control Operation

Clocked synchronous mode

- Data length: 8 bits
- Receive error detection: Overrun errors detected

Table 15.1 SCI3 Channel Configuration

Channel	Abbreviation	Pin*[1]	Register*[2]	Register Address
Channel 1	SCI3_1	SCK31	SMR3_1	H'FF98
		RXD31	BRR3_1	H'FF99
		TXD31	SCR3_1	H'FF9A
			TDR3_1	H'FF9B
			SSR3_1	H'FF9C
			RDR3_1	H'FF9D
			RSR3_1	—
			TSR3_1	—
			IrCR	H'FFA7
Channel 2	SCI3_2	SCK32	SMR3_2	H'FFA8
		RXD32	BRR3_2	H'FFA9
		TXD32	SCR3_2	H'FFAA
			TDR3_2	H'FFAB
			SSR3_2	H'FFAC
			RDR3_2	H'FFAD
			RSR3_2	—
			TSR3_2	—

Notes: 1. Pin names SCK3, RXD3, and TXD3 are used in the text for all channels, omitting the channel designation.
2. In the text, channel description is omitted for registers and bits.

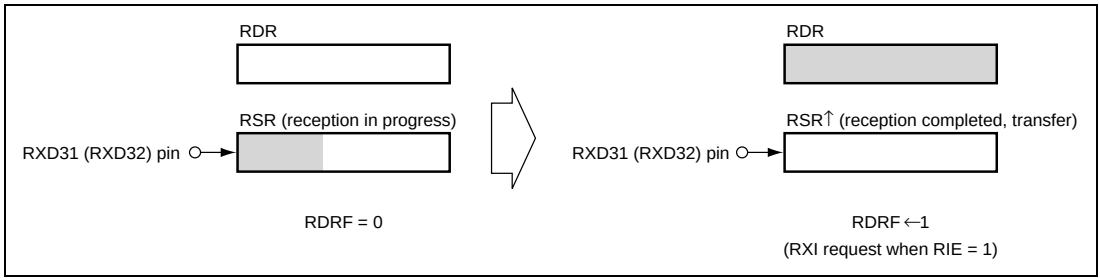


Figure 15.17 (a) RDRF Setting and RXI Interrupt

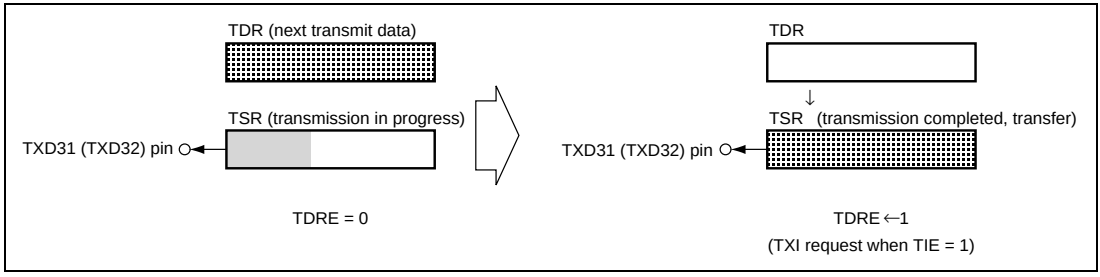


Figure 15.17 (b) TDRE Setting and TXI Interrupt

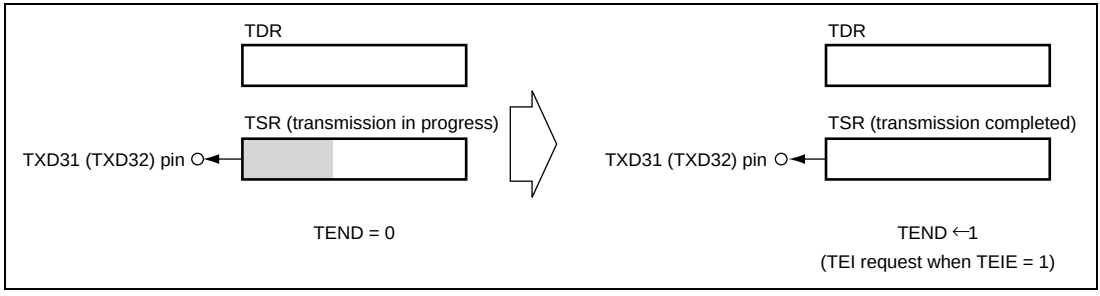


Figure 15.17 (c) TEND Setting and TEI Interrupt

16.3.2 Serial Control/Status Register 4 (SCSR4)

SCSR4 indicates the operating state and error state, selects the clock source, and controls the prescaler division ratio.

SCSR4 can be read from or written to by the CPU at any time. 1 cannot be written to flags TDRE, RDRF, ORER, and TEND. To clear these flags to 0, 1 should be read from them in advance.

Bit	Bit Name	Initial Value	R/W	Description
7	TDRE	1	R/(W)*	Transmit Data Empty Indicates that data is transferred from TDR4 to SR4 and the next serial transmit data can be written to TDR4. [Setting conditions] • When the TE bit in SCR4 is 0 • When data is transferred from TDR4 to SR4 and data can be written to TDR4 [Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When data is written to TDR4
6	RDRF	0	R/(W)*	Receive Data Full Indicates that the receive data is stored in RDR4. [Setting condition] • When serial reception ends normally and receive data is transferred from SR4 to RDR4 [Clearing conditions] • When 0 is written to RDRF after reading RDRF = 1 • When data is read from RDR4

Register Abbreviation	Reset	Active	Sleep	Watch	Subactive	Subsleep	Standby	Module
TCRF	Initialized	—	—	—	—	—	—	Timer F
TCSRF	Initialized	—	—	—	—	—	—	
TCFH	Initialized	—	—	—	—	—	—	
TCFL	Initialized	—	—	—	—	—	—	
OCRFH	Initialized	—	—	—	—	—	—	
OCRFL	Initialized	—	—	—	—	—	—	
ADRR	—	—	—	—	—	—	—	A/D converter
AMR	Initialized	—	—	—	—	—	—	
ADSR	Initialized	—	—	—	—	—	—	
PMR1	Initialized	—	—	—	—	—	—	I/O ports
PMR3	Initialized	—	—	—	—	—	—	
PMR4	Initialized	—	—	—	—	—	—	
PMR5	Initialized	—	—	—	—	—	—	
PMR9	Initialized	—	—	—	—	—	—	
PMRB	Initialized	—	—	—	—	—	—	
PWCR2	Initialized	—	—	—	—	—	—	14-bit PWM
PWDR2	Initialized	—	—	—	—	—	—	
PWCR1	Initialized	—	—	—	—	—	—	
PWDR1	Initialized	—	—	—	—	—	—	
PDR1	Initialized	—	—	—	—	—	—	I/O ports
OSCCR	Initialized	—	—	—	—	—	—	Clock pulse generator
PDR3	Initialized	—	—	—	—	—	—	I/O ports
PDR4	Initialized	—	—	—	—	—	—	
PDR5	Initialized	—	—	—	—	—	—	
PDR6	Initialized	—	—	—	—	—	—	
PDR7	Initialized	—	—	—	—	—	—	
PDR8	Initialized	—	—	—	—	—	—	
PDR9	Initialized	—	—	—	—	—	—	
PDRA	Initialized	—	—	—	—	—	—	
PDRB	Initialized	—	—	—	—	—	—	

24.4.2 DC Characteristics

Table 24.12 lists the DC characteristics.

Table 24.12 DC Characteristics

V_{CC} = 1.8 V to 3.6 V, AV_{CC} = 1.8 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, unless otherwise specified.

				Values				
Item	**Symbol**	**Applicable Pins**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**	**Notes**
Input high voltage	V_{IH}	$\overline{RES}$, $\overline{NMI}$, $\overline{WKP0}$ to $\overline{WKP7}$, $\overline{IRQ4}$, AEVL, AEVH, TMIF, $\overline{ADTRG}$, SCK32, SCK31		0.9V_{cc}	—	V_{cc} + 0.3	V	
		$\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{IRQ3}$		0.9V_{cc}	—	AV_{cc} + 0.3		
		RXD32, RXD31		0.8V_{cc}	—	V_{cc} + 0.3		
		OSC1		0.9V_{cc}	—	V_{cc} + 0.3		
		X1	V_{cc} = 2.7 to 3.6 V	0.9V_{cc}	—	V_{cc} + 0.3		
		P10 to P16, P30 to P32, P36, P37, P40 to P42, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P93, PA0 to PA3, TCLKA, TCLKB, TCLKC, TIOCA1, TIOCA2, TIOCB1, TIOCB2, SCL, SDA		0.8V_{cc}	—	V_{cc} + 0.3		
		PB0 to PB7		0.8V_{cc}	—	AV_{cc} + 0.3		
		IRQAEC		0.9V_{cc}	—	V_{cc} + 0.3		

24.4.6 Power-On Reset Circuit Characteristics

Table 24.18 lists the power-on reset circuit characteristics.

Table 24.18 Power-On Reset Circuit Characteristics

V_{CC} = 1.8 V to 3.6 V, AV_{CC} = 1.8 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V,
Ta = –20 to +75°C (regular specifications), Ta = –40 to +85°C (wide-range specifications), unless otherwise specified.

Item	Symbol	Test Condition	Values			Unit	Reference Figure
			Min.	Typ.	Max.		
Reset voltage	V_rst		0.7Vcc	0.8Vcc	0.9Vcc	V	Figure 24.1
Power supply rise time	t_vtr		The Vcc rise time should be shorter than half the $\overline{RES}$ rise time.				
Reset count time	t_out		0.8	—	4.0	µs	
Count start time	t_cr		Adjustable by the value of the external capacitor of the $\overline{RES}$ pin.				
On-chip pull-up resistance	Rp	Vcc = 3.0 V	60	100	—	kΩ	Figure 21.1

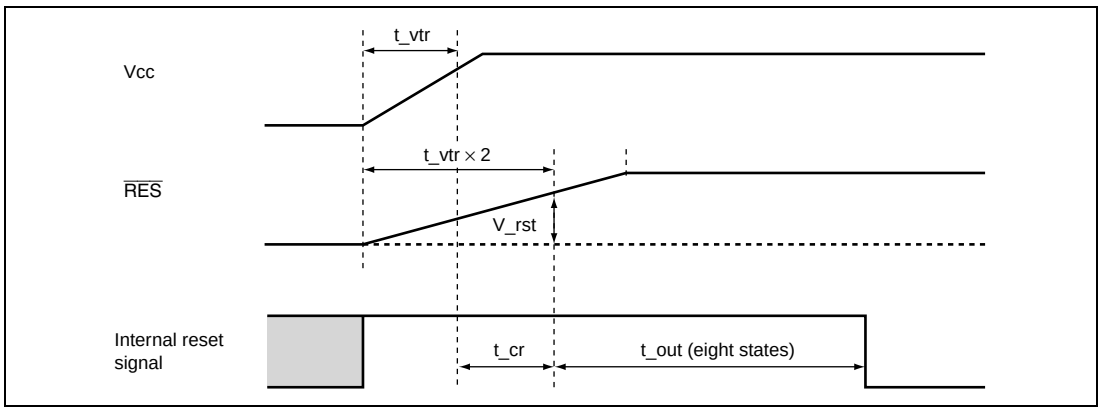


Figure 24.1 Power-On Reset Circuit Reset Timing

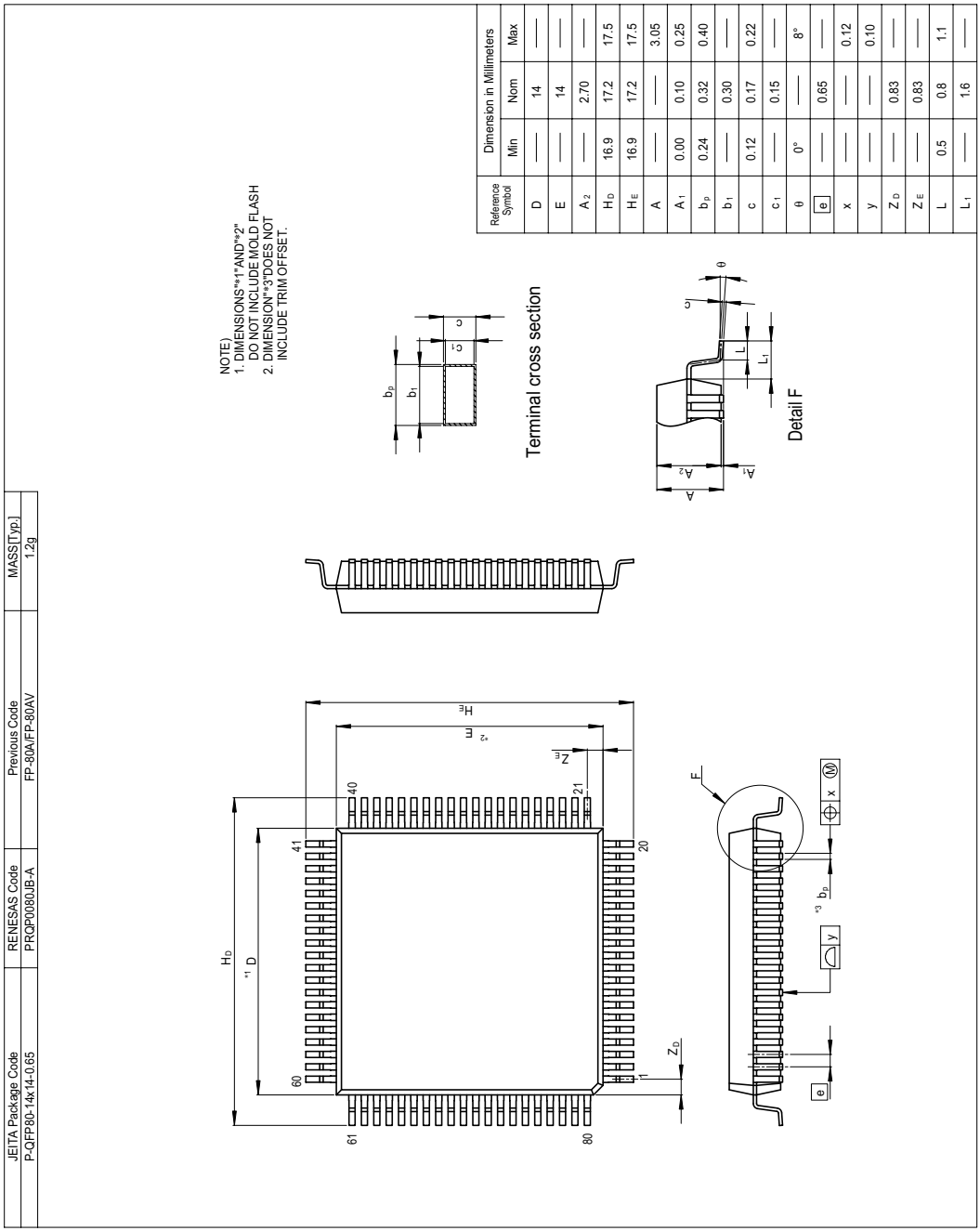
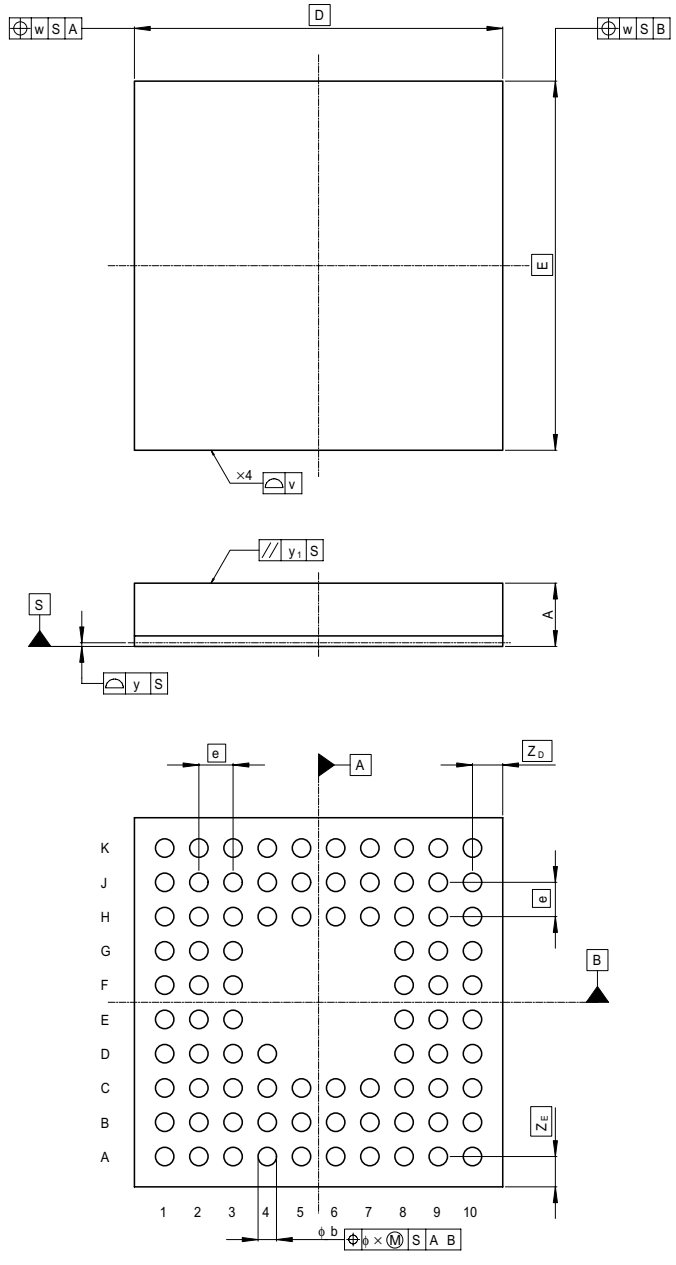


Figure D.1 Package Dimensions (FP-80A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA85-7x7-0.65	PTLG0085JA-A	TLP-85V	0.1g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.20
A_1	—	—	—
e	—	0.65	—
b	0.30	0.35	0.40
x	—	—	0.08
y	—	—	0.10
y_1	—	—	0.2
S_D	—	—	—
S_E	—	—	—
Z_D	—	0.575	—
Z_E	—	0.575	—

Figure D.3 Package Dimensions (TLP-85V)