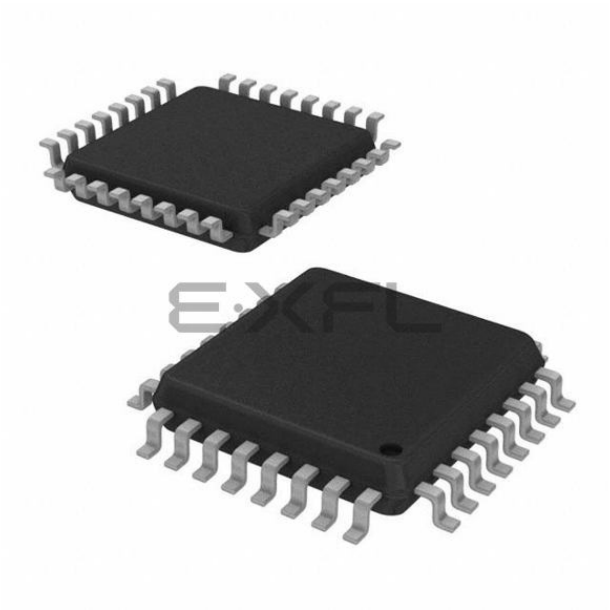

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	51.34MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 13x12b; D/A 3x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08mp16vlc

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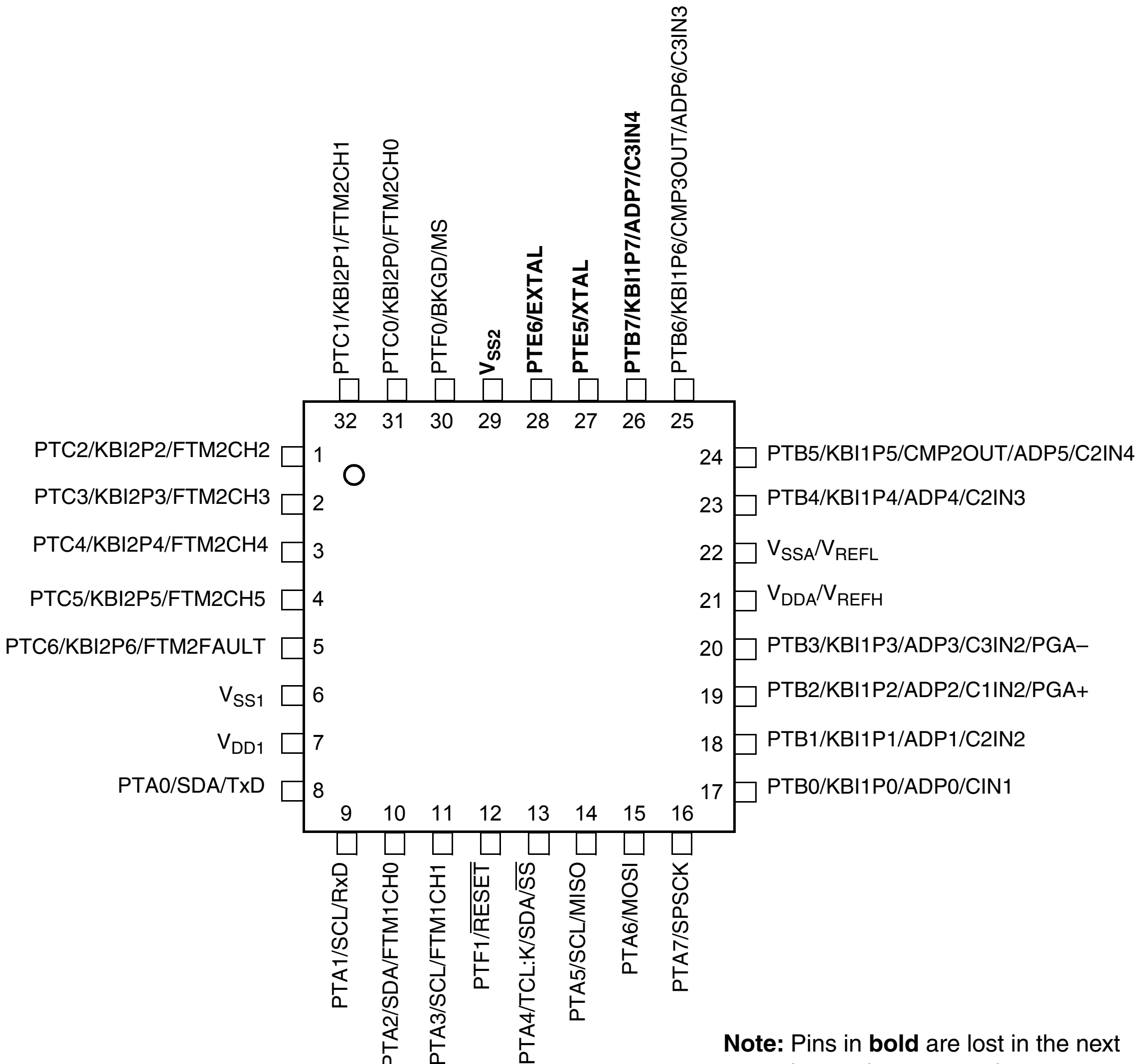


Note: Pins in **bold** are lost in the next lower pin count package.

Figure 3. MC9S08MP16 Series in 32-Pin LQFP Package

Table 1. Pin Availability by Package Pin-Count

Pin Number			<-- Lowest **Priority** --> Highest				
48	**32 LQFP**	**28**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt3**	**Alt4**
1	3	5	PTC4	KBI2P4	FTM2CH4		
2	4	6	PTC5	KBI2P5	FTM2CH5		
3	5	7	PTC6	KBI2P6	FTM2FAULT		
4	—	—	PTC7	KBI2P7	TCLK[1]		
5	—	—	PTD0	KBI3P0	SDA[5]		
6	—	—	PTD1	KBI3P1	SCL[5]		
7	—	—	PTD2	KBI3P2	PDB1OUT		
8	—	—	PTD3	KBI3P3	FTM1FAULT		
9	6	8					V_{SS1}
10	7	9					V_{DD1}
11	8	10	PTA0	SDA[5]	TxD		
12	9	11	PTA1	SCL[5]	RxD		
13	10	12	PTA2	SDA[5]	FTM1CH0		
14	11	13	PTA3	SCL[5]	FTM1CH1		
15	—	—	PTD4	KBI3P4	PDB2OUT		
16	—	—	PTD5	KBI3P5	CMP1OUT		
17	—	—	PTD6	KBI3P6	CMP2OUT[2]		
18	—	—	PTD7	KBI3P7	CMP3OUT[3]		
19	12	14	PTF1	$\overline{\text{RESET}}$[4]			
20	—	—	PTF2				
21	13	15	PTA4	TCLK[1]	SDA[5]	$\overline{\text{SS}}$	
22	14	16	PTA5		SCL[5]	MISO	
23	15	17	PTA6			MOSI	
24	16	18	PTA7			SPSCK	
25	—	—	PTE0		ADP8		
26	—	—	PTE1		ADP9		
27	—	—	PTE2		ADP10		
28	17	19	PTB0	KBI1P0	ADP0[6]	CIN1[6]	
29	18	20	PTB1	KBI1P1	ADP1[6]	C2IN2[6]	
30	19	21	PTB2	KBI1P2	ADP2[6]	C1IN2[6]	PGA+[6]
31	20	22	PTB3	KBI1P3	ADP3[6]	C3IN2[6]	PGA–[6]
32	21	23					V_{DDA}/V_{REFH}
33	22	24					V_{SSA}/V_{REFL}
34	—	—	PTE3		ADP11[6]	C1IN3[6]	

2.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

P	Those parameters that are guaranteed during production testing on each individual device.
C	Those parameters that are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters that are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters that are derived mainly from simulations.

NOTE

The classification is shown in the column labeled "C" in the parameter tables where appropriate.

2.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 3 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 3. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +5.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	± 25	mA
Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins, except for PTF1/$\overline{\text{RESET}}$ are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

2.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 4. Thermal Characteristics

Num	C	Rating		Symbol	Consumer & Industrial	Automotive	Unit
1	—	Operating temperature range (packaged)		T_A	–40 to 105	–40 to 125	°C
2	D	Maximum junction temperature		T_J	115	135	°C
3	D	Thermal resistance [1,2] single-layer board					
			48-pin LQFP	θ_{JA}	80	80	°C/W
			32-pin LQFP		85	—	
			28-pin SOIC		71	—	
4	D	Thermal resistance [1,2] four-layer board					
			48-pin LQFP	θ_{JA}	56	56	°C/W
			32-pin LQFP		57	—	
			28-pin SOIC		48	—	

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Junction-to-ambient natural convection

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} \ll P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

Table 7. DC Characteristics (continued)

Num	C	Characteristic		Symbol	Condition	Min	Typ[1]	Max	Unit
4	C	Output high voltage	All I/O pins (except PTF1/$\overline{\text{RESET}}$) low-drive strength	V_{OH}	5 V, I_{Load} = –4 mA	V_{DD} – 1.5	—	—	V
	P				5 V, I_{Load} = –2 mA	V_{DD} – 0.8	—	—	
	C				3 V, I_{Load} = –1 mA	V_{DD} – 0.8	—	—	
	C		high-drive strength		5 V, I_{Load} = –20 mA	V_{DD} – 1.5	—	—	
	P				5 V, I_{Load} = –10 mA	V_{DD} – 0.8	—	—	
	C				3 V, I_{Load} = –5 mA	V_{DD} – 0.8	—	—	
5	D	Output high current	Max total I_{OH} for all ports	I_{OHT}	$V_{OUT} < V_{DD}$	0	—	–100	mA
6	C	Output low voltage	All I/O pins (except PTF1/$\overline{\text{RESET}}$) low-drive strength	V_{OL}	5 V, I_{Load} = 4 mA	—	—	1.5	V
	P				5 V, I_{Load} = 2 mA	—	—	0.8	
	C				3 V, I_{Load} = 1 mA	—	—	0.8	
	C		All I/O pins (Except PTF1/$\overline{\text{RESET}}$) high-drive strength		5 V, I_{Load} = 20 mA	—	—	1.5	
	P				5 V, I_{Load} = 10 mA	—	—	0.8	
	C				3 V, I_{Load} = 5 mA	—	—	0.8	
7	C		PTF1/$\overline{\text{RESET}}$		5 V, I_{Load} = 3.2 mA	—	—	1.5	
8	P				5 V, I_{Load} = 1.6 mA	—	—	0.8	
9	C				3 V, I_{Load} = 0.8 mA	—	—	0.8	
10	D	Output low current	Max total I_{OL} for all ports	I_{OLT}	$V_{OUT} > V_{SS}$	0	—	100	mA
11	P	Input high voltage; all digital inputs		V_{IH}	5V	0.65 x V_{DD}	—	—	V
	C				3V	0.7 x V_{DD}	—	—	
12	P	Input low voltage; all digital inputs		V_{IL}	5V	—	—	0.35 x V_{DD}	V
	C				3V	—	—	0.35 x V_{DD}	
13	C	Input hysteresis		V_{hys}		0.06 x V_{DD}			V
14	P	Input leakage current (per pin)		$\|I_{In}\|$	$V_{In} = V_{DD}$ or V_{SS}	—	—	1	μA
15	P	Hi-Z (off-state) leakage current (per pin)	input/output port pins	$\|I_{OZ}\|$	$V_{In} = V_{DD}$ or V_{SS}	—	—	1	μA
			PTF1/$\overline{\text{RESET}}$, PTE5/XTAL pins		$V_{In} = V_{DD}$ or V_{SS}	—	—	2	μA
16	P	Pullup or Pulldown[3] resistors; when enabled	I/O pins	R_{PU},R_{PD}		17	37	52	kΩ
	C		PTF1/$\overline{\text{RESET}}$[4]	R_{PU}		17	37	52	kΩ
17	D	DC injection current[5, 6, 7, 8]	Single pin limit	I_{IC}	$V_{IN} > V_{DD}$	0	—	2	mA
					$V_{IN} < V_{SS}$	0	—	–0.2	mA
			Total MCU limit, includes sum of all stressed pins		$V_{IN} > V_{DD}$	0	—	25	mA
					$V_{IN} < V_{SS}$	0	—	–5	mA

Table 7. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit
13	C	Input Capacitance, all pins	C_{In}		—	—	8	pF
14	C	RAM retention voltage	V_{RAM}		—	0.6	1.0	V
15	C	POR re-arm voltage[9]	V_{POR}		0.9	1.4	2.0	V
16	D	POR re-arm time	t_{POR}		10	—	—	µs
17	P	Low-voltage detection threshold — high range V_{DD} falling V_{DD} rising	V_{LVD1}		 3.9 4.0	 4.0 4.1	 4.1 4.2	V
18	P	Low-voltage detection threshold — low range V_{DD} falling V_{DD} rising	V_{LVD0}		 2.48 2.54	 2.56 2.62	 2.64 2.70	V
19	P	Low-voltage warning threshold — high range 1 V_{DD} falling V_{DD} rising	V_{LVW3}		 4.5 4.6	 4.6 4.7	 4.7 4.8	V
20	P	Low-voltage warning threshold — high range 0 V_{DD} falling V_{DD} rising	V_{LVW2}		 4.2 4.3	 4.3 4.4	 4.4 4.5	V
21	P	Low-voltage warning threshold low range 1 V_{DD} falling V_{DD} rising	V_{LVW1}		 2.84 2.90	 2.92 2.98	 3.00 3.06	V
22	P	Low-voltage warning threshold — low range 0 V_{DD} falling V_{DD} rising	V_{LVW0}		 2.66 2.72	 2.74 2.80	 2.82 2.88	V
23	T	Low-voltage inhibit reset/recover hysteresis	V_{hys}	5 V	—	100	—	mV
				3 V	—	60	—	
24	P	Bandgap voltage reference at 25°C[10]	V_{BG}		1.18	1.202	1.21	V
25	P	Bandgap voltage reference across temperature range[10]			1.17	—	1.22	V

1 Typical values are measured at 25°C. Characterized, not tested

2 DC potential difference.

3 When keyboard interrupt is configured to detect rising edges, pulldown resistors are used in place of pullup resistors.

4 The specified resistor value is the actual value internal to the device. The pullup value may measure higher when measured externally on the pin.

5 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

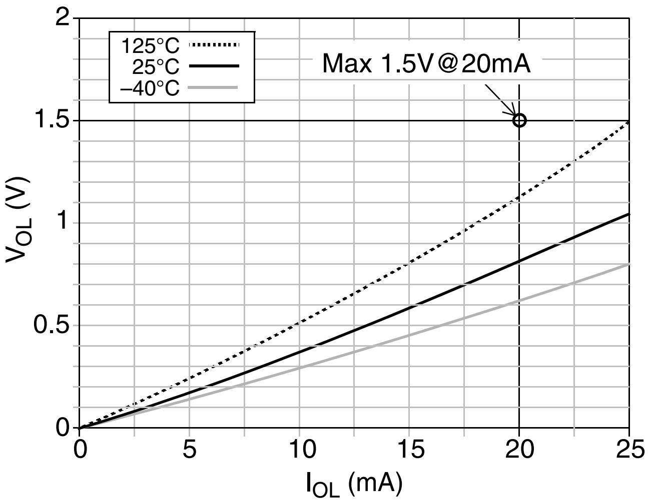
6 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

[7] All functional non-supply pins except PTF1/$\overline{\text{RESET}}$ are internally clamped to V_{SS} and V_{DD}.

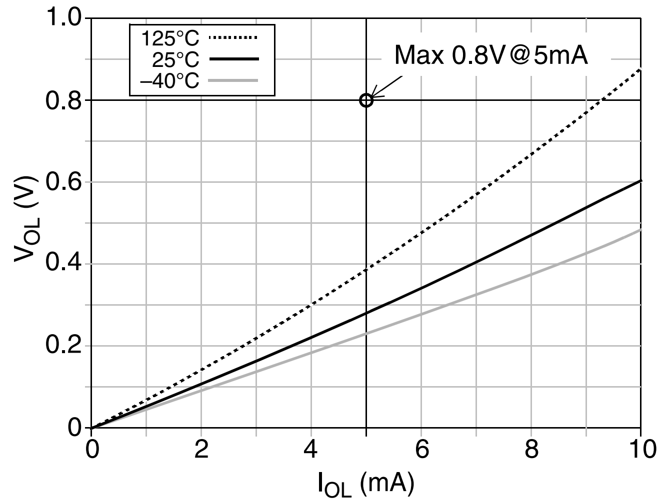
[8] The PTF1/$\overline{\text{RESET}}$ pin does not have a clamp diode to V_{DD}. Do not drive this pin above V_{DD}.

[9] Maximum is highest voltage that POR is guaranteed.

[10] Factory trimmed at V_{DD} = 5.0 V

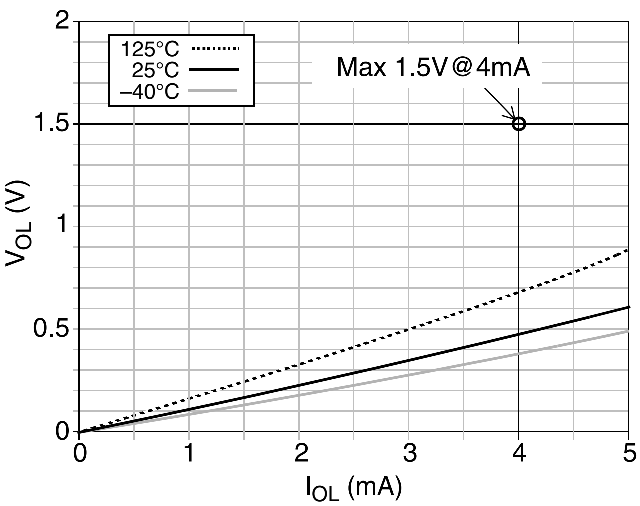


a) V_{DD} = 5V, High Drive

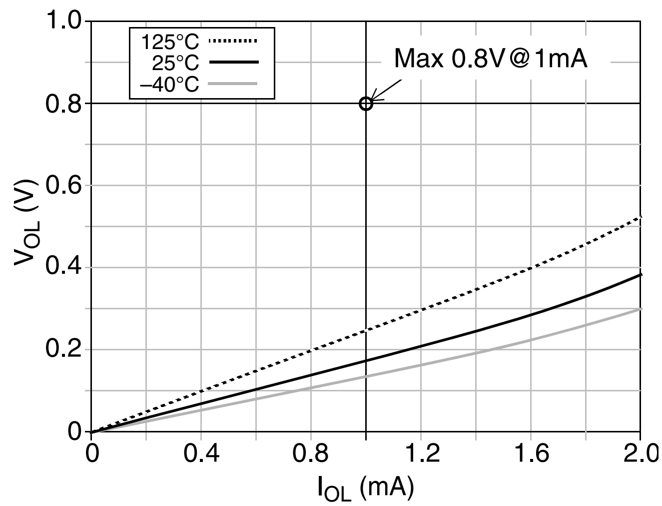


b) V_{DD} = 3V, High Drive

Figure 5. Typical V_{OL} vs I_{OL}, High Drive Strength (except PTF1/RESET)



a) V_{DD} = 5V, Low Drive



b) V_{DD} = 3V, Low Drive

Figure 6. Typical V_{OL} vs I_{OL}, Low Drive Strength (except PTF1/RESET)

Table 8. Supply Current Characteristics (continued)

Num	C	Parameter	Symbol	V_{DD} (V)	Typ[1]	Max[2]	Unit
3	C	Run supply current[4] measured at (CPU clock = 32 MHz, f_{Bus} = 16 MHz)	RI_{DD}	5	9.4	10	mA
	C			3	9	10	
4	P	Run supply current[5] measured at (CPU clock = 51.34 MHz, f_{Bus} = 25.67 MHz)	RI_{DD}	5	14.3	30	mA
	C			3	13.9	20	
5	P	Run supply current measured at (CPU clock = 40 MHz, f_{Bus} = 20 MHz)	RI_{DD}	5	16	30	mA
	—			3	—	—	
6	C	Wait mode supply current measured at (CPU clock = 8 MHz, f_{Bus} = 4 MHz) (FEI mode, all modules off)	WI_{DD}	5	2.7	—	mA
7		Stop3 mode supply current					
	C	–40°C	$S3I_{DD}$	5	0.96	—	μA
	P	25°C			1.3	—	
	C	85°C			7.5	25	
	P[6]	105°C			37	90	
	P	125°C			65	150	
	C	–40°C		3	0.85	—	μA
	P	25°C			1.2	—	
	C	85°C			6.5	20	
	P[6]	105°C			32.7	80	
	P	125°C			58	130	
8		Stop2 mode supply current					
	C	–40°C	$S2I_{DD}$	5	0.94	—	μA
	P	25°C			1.25	—	
	C	85°C			7	25	
	P[6]	105°C			30	65	
	P	125°C			64	120	
	C	–40°C		3	0.83	—	μA
	P	25°C			1.1	—	
	C	85°C			6.3	20	
	P[6]	105°C			25	55	
	P	125°C			57	100	
9	C	RTC adder to stop2 or stop3[7]	$S23I_{DDRTC}$	5	300	500	nA
				3	300	500	nA

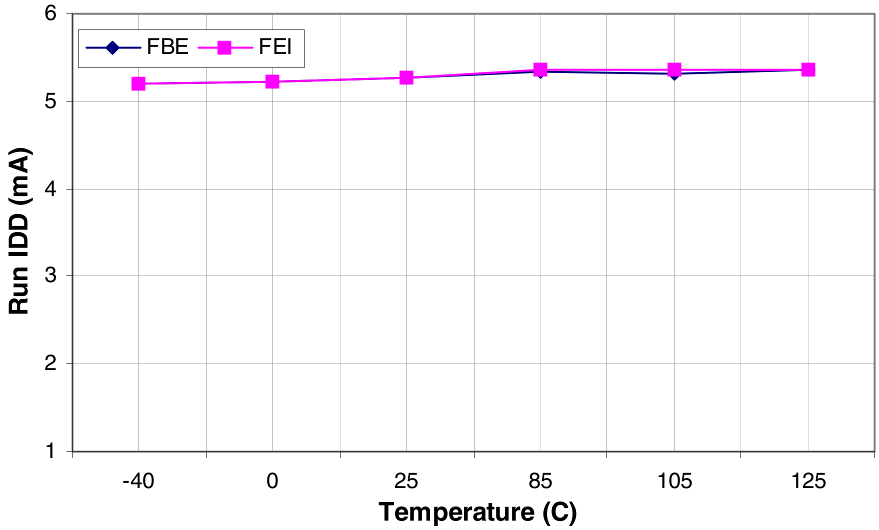


Figure 10. Typical Run I_{DD} vs. Temperature (V_{DD} = 5V, f_{bus} = 8MHz)

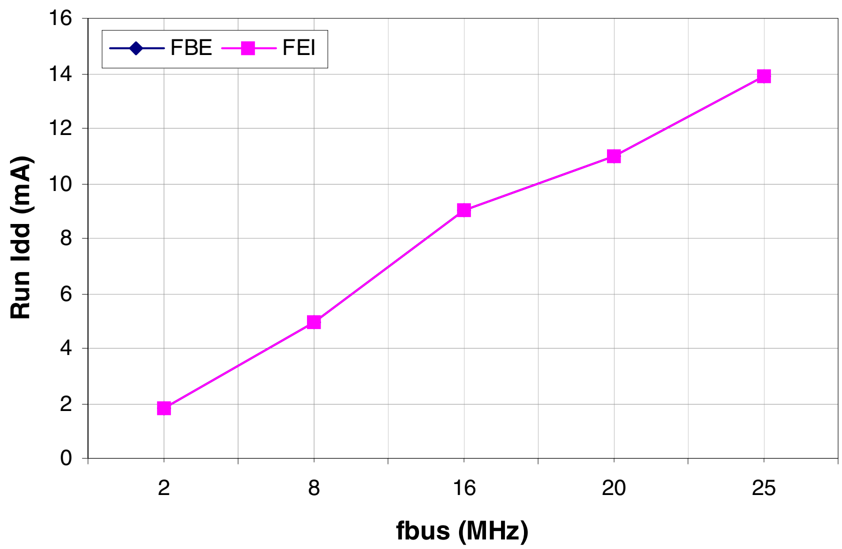


Figure 11. Typical Run I_{DD} vs. Bus Frequency (V_{DD} = 3V)

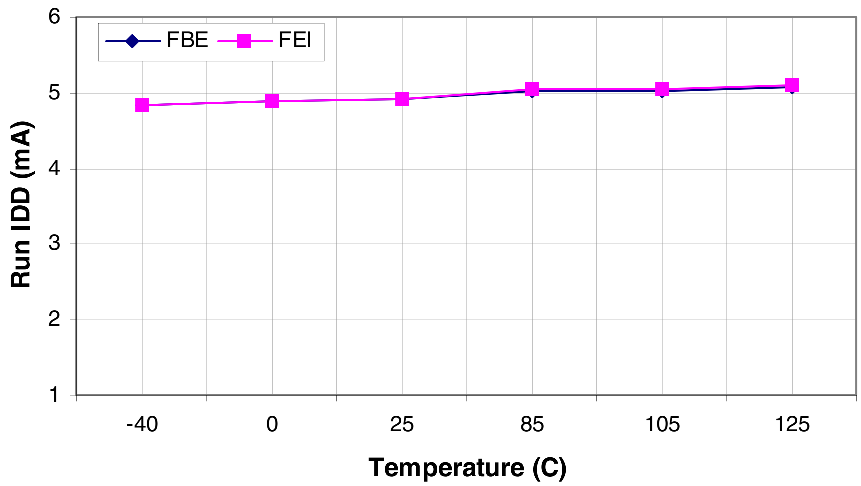


Figure 12. Typical Run I_{DD} vs. Temperature (V_{DD} = 3V, f_{bus} = 8MHz)

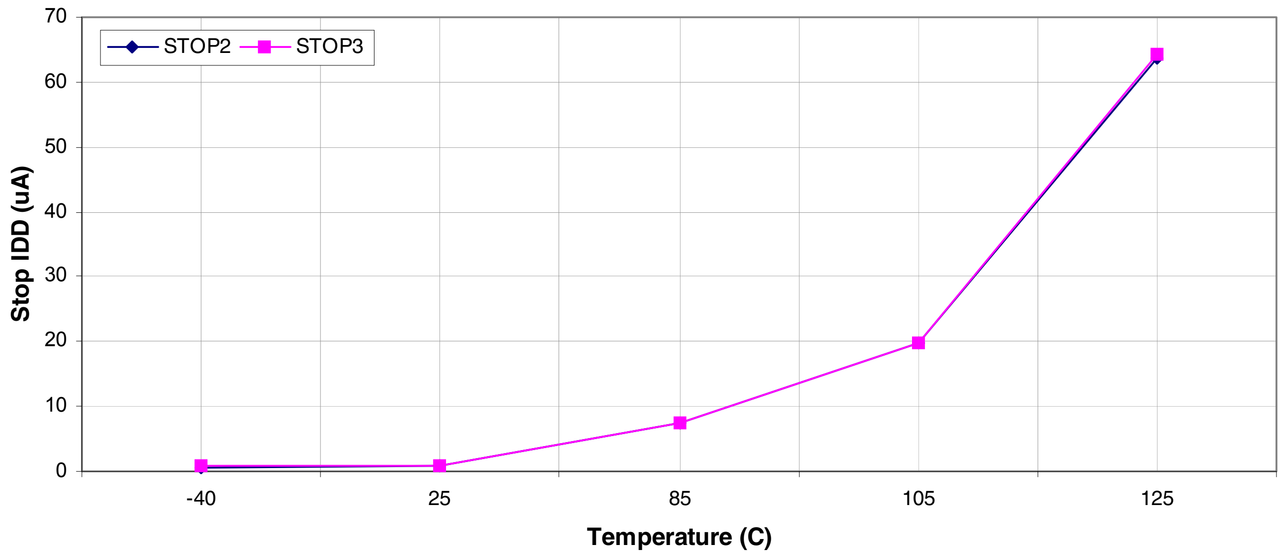


Figure 13. Typical Stop I_{DD} vs. Temperature (V_{DD} = 5V)

Table 9. Oscillator Electrical Specifications (continued)

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
5	T	Crystal start-up time [4]					ms
		Low range, low gain (RANGE = 0, HGO = 0)	$t_{CSTL\text{-}LP}$	—	200	—	
		Low range, high gain (RANGE = 0, HGO = 1)	$t_{CSTL\text{-}HGO}$	—	400	—	
		High range, low gain (RANGE = 1, HGO = 0)[5]	$t_{CSTH\text{-}LP}$	—	5	—	
		High range, high gain (RANGE = 1, HGO = 1)[4]	$t_{CSTH\text{-}HGO}$	—	20	—	
6	T	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1)	f_{extal}				
		FEE mode [2]		0.03125	—	51.34	MHz
		FBE mode [3]		0	—	51.34	MHz
		FBELP mode		0	—	51.34	MHz

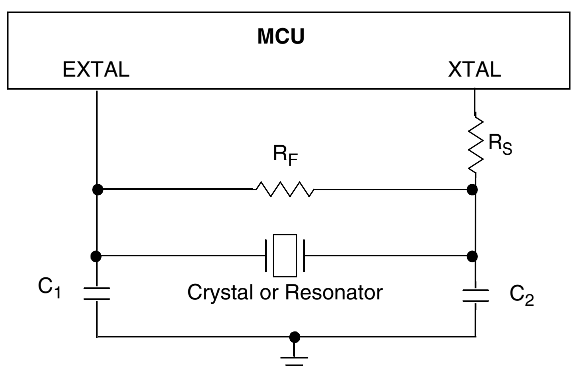
[1] Typical data was characterized at 5.0 V, 25°C or is recommended value.

[2] The input clock source must be divided using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

[3] The input clock source must be divided using RDIV to less than or equal to 39.0625 kHz.

[4] This parameter is characterized and not tested on each device. Proper PC board layout procedures must be followed to achieve specifications.

[5] 4 MHz crystal



2.9 Internal Clock Source (ICS) Characteristics

Table 10. ICS Frequency Specifications

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1a	P	Average internal reference frequency — factory trimmed (consumer- and industrial-qualified devices) at V_{DD} = 5 V and temperature = 25°C	f_{int_t}	—	32.768	—	kHz
1b	P	Average internal reference frequency — factory trimmed (automotive-qualified devices) at V_{DD} = 5 V and temperature = 25°C	f_{int_t}	—	31.25	—	kHz
2	P	Internal reference frequency — user trimmed	f_{int_t}	31.25	—	39.06	kHz
3	T	Internal reference start-up time	t_{irefst}	—	60	100	μs

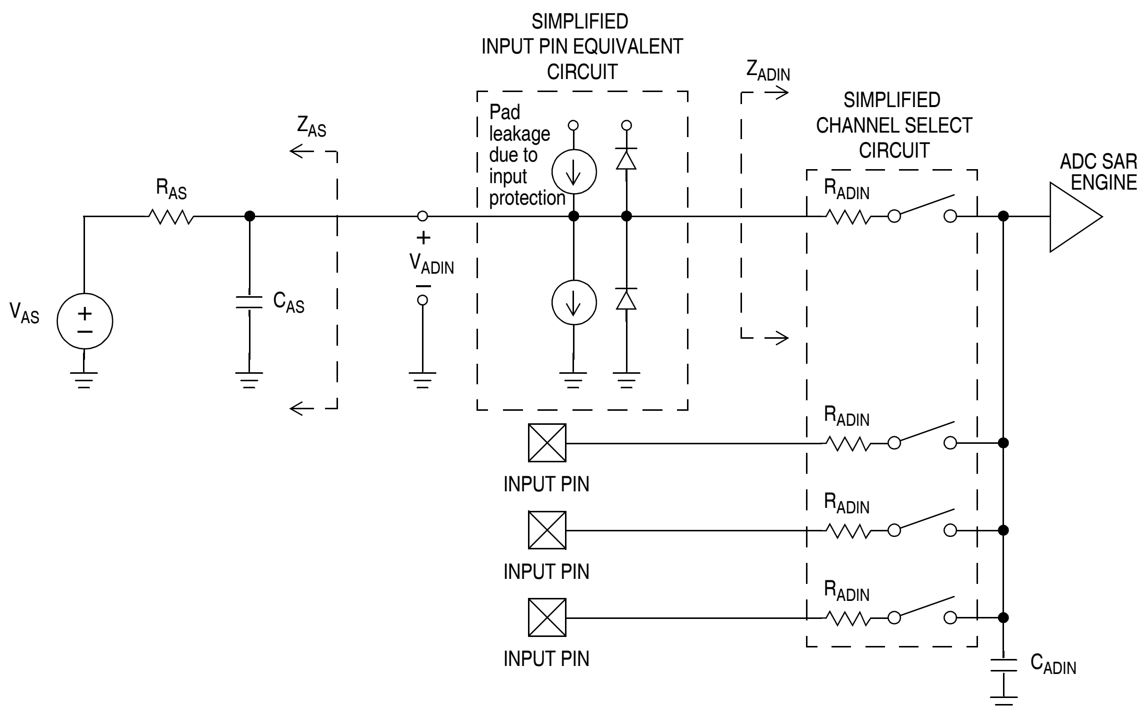


Figure 16. ADC Input Impedance Equivalency Diagram

Table 12. 12-bit ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$)

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
T	Supply Current ADLPC=1 ADLSMP=1 ADCO=1		I_{DDA}	—	133	—	μA	
T	Supply Current ADLPC=1 ADLSMP=0 ADCO=1		I_{DDA}	—	218	—	μA	
T	Supply Current ADLPC=0 ADLSMP=1 ADCO=1		I_{DDA}	—	327	—	μA	
T	Supply Current ADLPC=0 ADLSMP=0 ADCO=1		I_{DDA}	—	0.582	—	mA	
P	ADC Asynchronous Clock Source	High Speed (ADLPC=0)	f_{ADACK}	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
		Low Power (ADLPC=1)		1.25	2	3.3		

2.11 Digital to Analog (DAC) Characteristics

- The accuracy at worst case: +/- 1.5% maximum
- The settling time must be less than 100 ns
- When changing the output voltage level, the voltage glitch cannot be completely eliminated

Table 13. 5-bit DAC Characteristics

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
2	D	Supply current adder (enabled)	I_{DDAC}	—	—	20	μA
3	D	DAC reference inputs	Vin	V_{SSA}	—	V_{DDA}	V
5	D	DAC step size	V_{step}	$0.75 \times V_{in}/32$	$V_{in}/32$	$1.25 \times V_{in}/32$	V
6	D	DAC voltage range	V_{dacout}	$V_{in}/32$	—	V_{in}	V

2.12 High Speed Comparator (HSCMP) Characteristics

Table 14. High Speed Comparator Electrical Specifications

Num	C	Characteristic[1]	Symbol	Min	Typical	Max	Unit
1	D	Supply current, High Speed Mode (EN=1, PMODE=1)	I_{DDAHS}	—	200		μA
2	D	Supply current, Low Speed Mode (EN=1, PMODE=0)	I_{DDALS}	—	10		μA
3	—	Analog input voltage	V_{AIN}	V_{SSA}	—	V_{DDA}	V
4	P	Analog input offset voltage	V_{AIO}	—	5	40	mV
5	C	Analog Comparator hysteresis	V_H	3.0	9	20.0	mV
6	T	Propagation Delay, High Speed Mode (EN=1, PMODE=1)	t_{DHS}[2]	—	70	120	ns
7	T	Propagation Delay, Low Speed Mode (EN=1, PMODE=0)	t_{DLS}[2]	—	400	600	ns
8	D	Analog comparator initialization delay	t_{AINIT}	—	400	—	ns

[1] All timing assumes slew rate control disabled and high drive strength enabled.

[2] Delay from analog input to the CMPxOUT output pin. Measured with an input waveform that switches 30 mV above and below the reference.

2.13 Programmable Gain Amplifier (PGA) Characteristics

Table 15. Programmable Gain Amplifier Electrical Specifications

Num	C	Parameter	Symbol	Min	Typical	Max	Unit
1	T	Supply current adder • normal mode (LP=0) • low power mode (LP=1)	I_{DDON}	 — —	 450 250	 550 300	uA
2	T	Supply current adder (stand-by)	I_{DDAOFF}	—	1	10	nA
3	T	Absolute analog input level	V_{IL}	V_{SSA}	$V_{DDA}/2$	V_{DDA}	V

Table 16. Control Timing (continued)

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
7	D	Keyboard interrupt pulse width Asynchronous path[4] Synchronous path[5]	t_{ILIH}, t_{IHIL}	 100 1.5 x t_{cyc}	 — —	 — —	ns
8	C	Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF)[6] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 40 75	 — —	ns
		Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF)[6] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 11 35	 — —	ns

1 Typical values are based on characterization data at V_{DD} = 5.0V, 25°C unless otherwise stated.
2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request.
3 To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.
4 This is the minimum pulse width that is guaranteed to be recognized as a keyboard interrupt request in stop mode.
5 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.
6 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 125°C.

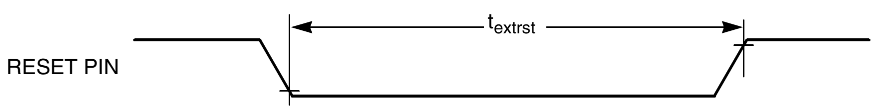


Figure 17. Reset Timing

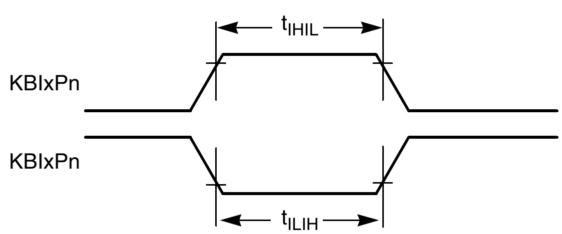


Figure 18. KBIxPn Timing

2.14.2 FTM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the FTM timer counter. These synchronizers operate from the current ICSOUT clock. The ICSOUT clock period = $0.5 \times t_{cyc} = 1/(f_{Bus} \times 2)$.

Table 17. FTM Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{ICSOUT}/4$[1]	Hz
2	D	External clock period	t_{TCLK}	2	—	t_{cyc}
3	D	External clock high time	t_{clkh}	0.75	—	t_{cyc}

2.14.4 SPI

Table 19 and Figure 22 through Figure 25 describe the timing requirements for the SPI system.

Table 19. SPI Electrical Characteristics

Num[1]	C	Rating[2]	Symbol	Min	Max	Unit
1	D	Cycle time Master Slave	t_{SCK} t_{SCK}	2 4	4096 —	t_{cyc} t_{cyc}
2	D	Enable lead time Master Slave	t_{Lead} t_{Lead}	— 1/2	1/2 —	t_{SCK} t_{SCK}
3	D	Enable lag time Master Slave	t_{Lag} t_{Lag}	— 1/2	1/2 —	t_{SCK} t_{SCK}
4	D	Clock (SPSCK) high time Master and Slave	t_{SCKH}	1/2 t_{SCK} – 25	—	ns
5	D	Clock (SPSCK) low time Master and Slave	t_{SCKL}	1/2 t_{SCK} – 25	—	ns
6	D	Data setup time (inputs) Master Slave	$t_{SI(M)}$ $t_{SI(S)}$	30 30	— —	ns ns
7	D	Data hold time (inputs) Master Slave	$t_{HI(M)}$ $t_{HI(S)}$	30 30	— —	ns ns
8	D	Access time, slave[3]	t_A	0	40	ns
9	D	Disable time, slave[4]	t_{dis}	—	40	ns
10	D	Data setup time (outputs) Master Slave	t_{SO} t_{SO}	— —	25 25	ns ns
11	D	Data hold time (outputs) Master Slave	t_{HO} t_{HO}	–10 –10	— —	ns ns
12	D	Operating frequency Master (SPIFE=0) Slave (SPIFE=0) Master (SPIFE=1) Slave (SPIFE=1)	f_{op}	f_{Bus}/4096 dc f_{Bus}/4096 dc	8[5] f_{Bus}/4 5[6] 5[6]	MHz MHz MHz

[1] Refer to Figure 22 through Figure 25.

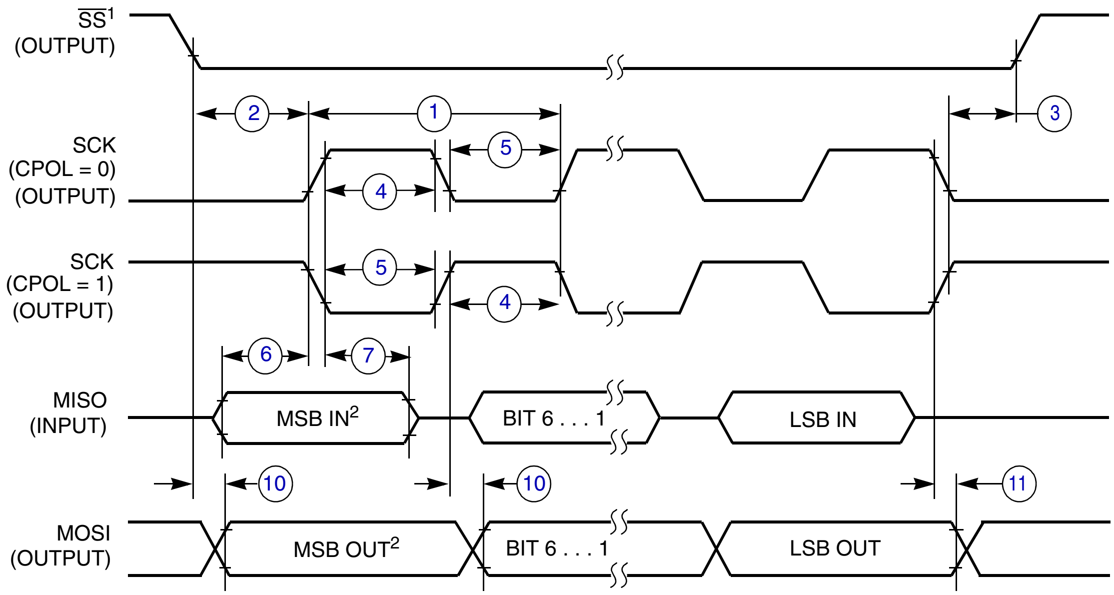
[2] All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless noted; 100 pF load on all SPI pins. All timing assumes slew rate control disabled and high drive strength enabled for SPI output pins.

[3] Time to data active from high-impedance state.

[4] Hold time to high-impedance state.

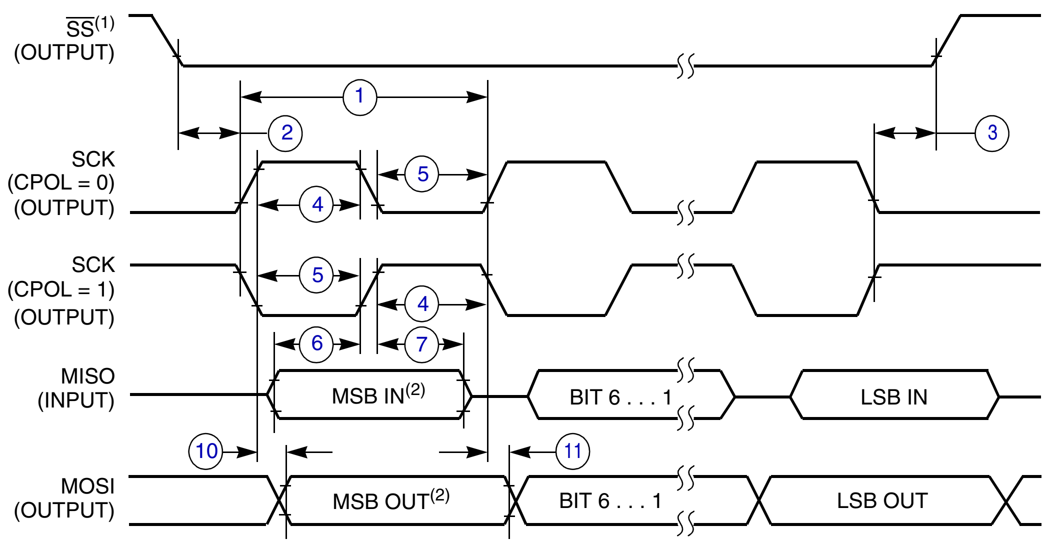
[5] Maximum baud rate must be limited to 8 MHz.

[6] Maximum baud rate must be limited to 5 MHz due to input filter characteristics.



NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 22. SPI Master Timing (CPHA = 0)



NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 23. SPI Master Timing (CPHA = 1)

custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East).

The maximum radiated RF emissions of the tested configuration in all orientations are less than or equal to the reported emissions levels.

Table 21. Radiated Emissions, Electric Field

Parameter	Symbol	Conditions	Frequency	f_{OSC}/f_{BUS}	Level[1] (Max)	Unit
Radiated emissions, electric field	V_{RE_TEM}	V_{DD} = 5V TA = +25°C package type 48 LQFP	0.15 – 50 MHz	4 MHz crystal 2 MHz bus	3	dBμV
			50 – 150 MHz		8	
			150 – 500 MHz		–4	
			500 – 1000 MHz		–8	
			IEC Level[2]		N	—
			SAE Level[3]		1	—

1 Data based on qualification test results. The reported emission level is the value of the maximum emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

2 IEC level maximums: N ≤ 12 dBμV, L ≤ 24 dBμV, I ≤ 36 dBμV

3 SAE level maximums: 1 ≤ 10 dBμV, 2 ≤ 20 dBμV, 3 ≤ 30 dBμV, 4 ≤ 40 dBμV

3 Ordering Information

This section contains ordering information for MC9S08MP16 and MC9S08MP12 devices.

Table 22. Device and Package Options

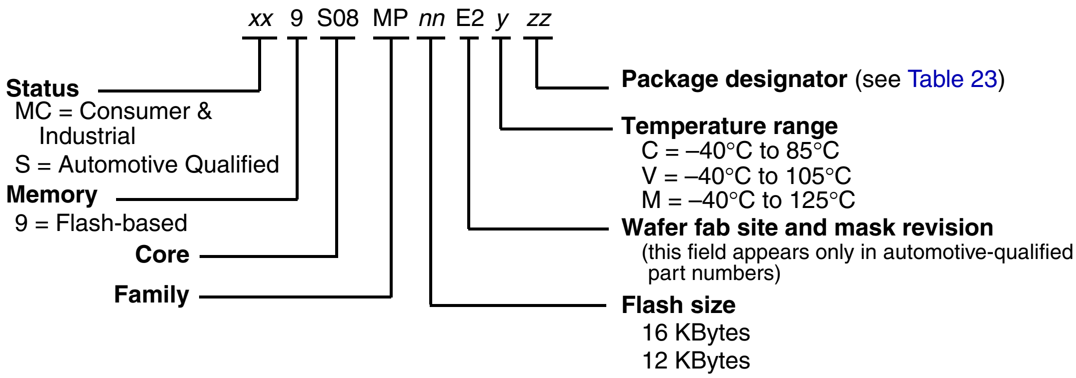
Device Number[1]	Temp Range	Memory		Available Packages[2]		
		Flash	RAM	48-Pin	32-Pin	28-Pin
Consumer and Industrial Qualification						
MC9S08MP16	V	16K	1024	48 LQFP	32 LQFP	28 SOIC
MC9S08MP12	V	12K	512	—	—	28 SOIC
Automotive Qualification						
S9S08MP16	C, V, M	16K	1024	48 LQFP	—	—

1 See the *MC9S08MP16RM Reference Manual* (MC9S08MP16RM) for a complete description of modules included on each device.

2 See Table 23 for package information.

3.1 Device Numbering Scheme

Example of the device numbering system:



4 Package Information

The latest package outline drawings are available on the product summary pages on our web site: http://www.freescale.com/8bit. The following table lists the document numbers per package. Use these numbers in the web page's keyword search engine to find the latest package outline drawings.

NOTE

The 32 LQFP and 28 SOIC are not qualified to meet automotive requirements.

Table 23. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
48	Low Quad Flat Pack	LQFP	LF	932-03	98ASH00962A
32	Low Quad Flat Pack	LQFP	LC	873A-03	98ASH70029A
28	Small Outline Integrated Circuit	SOIC	WL	751F-05	98ASB42345B

5 Related Documentation

Find the most current versions of all documents at http://www.freescale.com.

Reference Manual (MC9S08MP16RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

6 Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web are the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://www.freescale.com

Table 24 summarizes changes contained in this document.

Table 24. Revision History

Rev	Date	Description of Changes
1	10/15/2009	Initial public revision
2	08/09/2011	Updated Table 10. Changed the value of row 8 column “C” from to C to P.

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