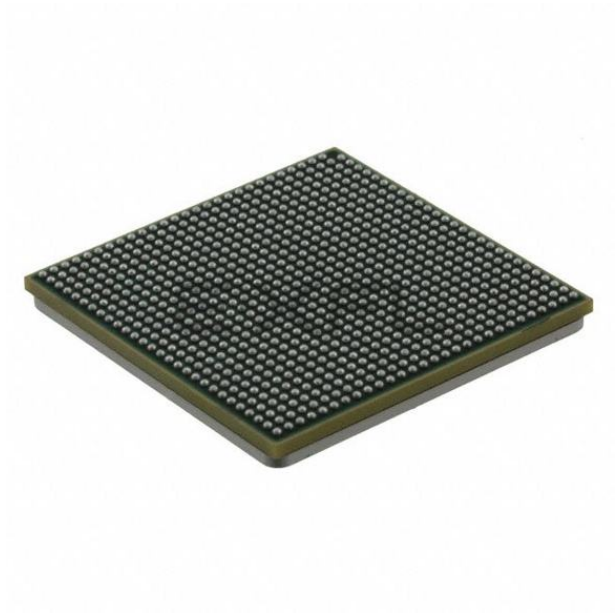

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e600
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	DIU, LCD
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmc8610vt1333jb

Figure 1 shows the major functional units within the MPC8610.

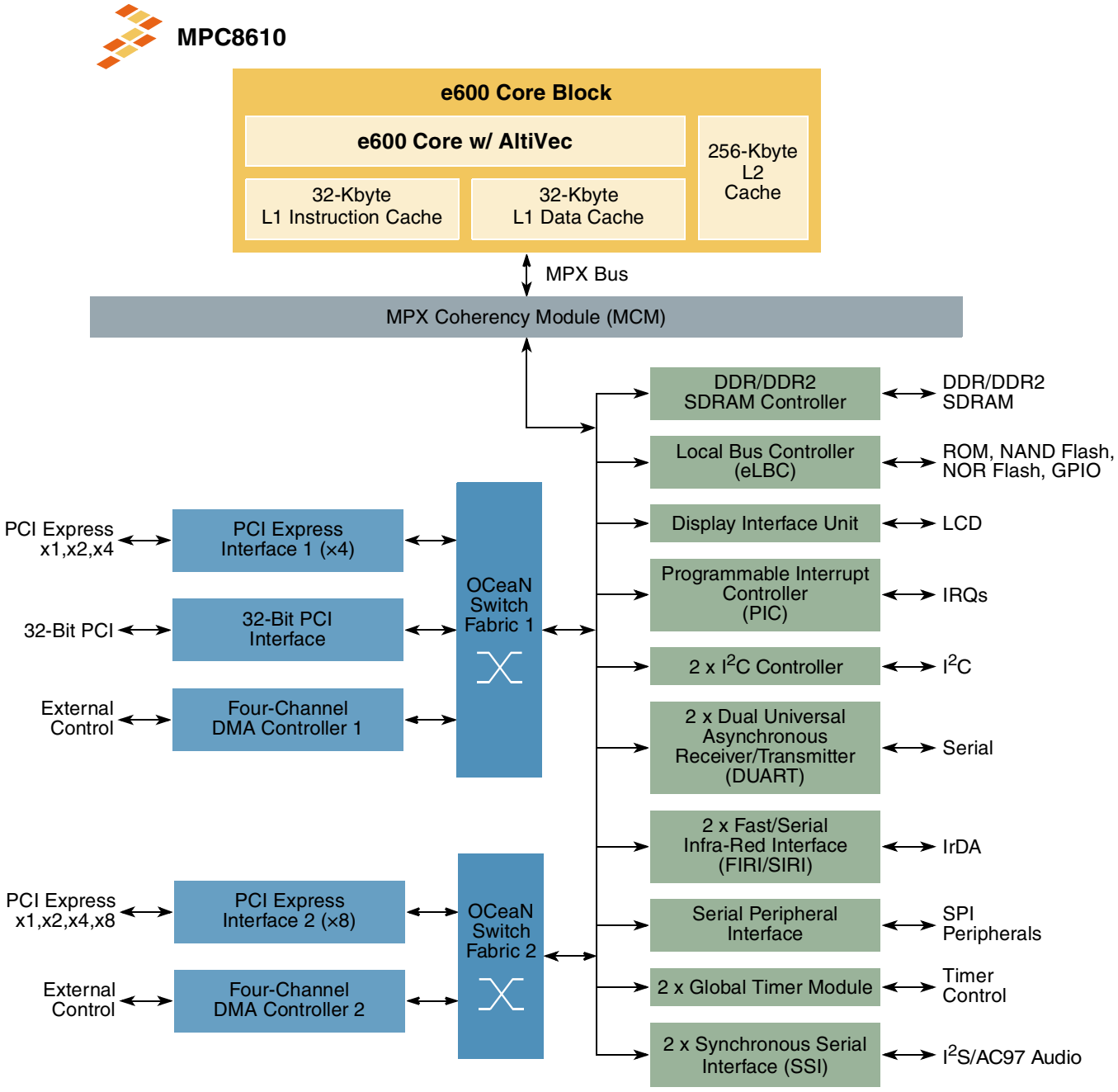


Figure 1. MPC8610 Block Diagram

Table 1. Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
DMA1_DREQ3/IRQ9/ GPIO2[26]	H26	I	OV_{DD}	23
DMA1_DACK0/IRQ7/ GPIO2[25]	J25	O	OV_{DD}	23
DMA1_DACK3/IRQ10/ GPIO2[27]	J26	O	OV_{DD}	23
DMA1_DDONE0/IRQ8	J27	O	OV_{DD}	23
DMA1_DDONE3/IRQ11/ GPIO2[28]	K27	O	OV_{DD}	23
DMA2_DREQ0/LCS5	R23	I	OV_{DD}	23
DMA2_DREQ3/ GPIO2[29]	H27	I	OV_{DD}	23
DMA2_DACK0/LCS6	N26	O	OV_{DD}	23
DMA2_DACK3/ GPIO2[30]	H28	O	OV_{DD}	23
DMA2_DDONE0/LCS7	R26	O	OV_{DD}	23
DMA2_DDONE3/ GPIO2[31]	J28	O	OV_{DD}	23
General-Purpose Timer Signals[4]				
GTM1_TIN1/GPIO2[15]	U3	I	OV_{DD}	23
GTM1_TIN3/GPIO2[21]	W2	I	OV_{DD}	23
GTM1_TGATE1/ GPIO2[16]	V2	I	OV_{DD}	23
GTM1_TGATE3/ GPIO2[22]	U1	I	OV_{DD}	23
GTM1_TOUT1/GPIO2[17]	W3	O	OV_{DD}	23
GTM1_TOUT3/GPIO2[23]	U2	O	OV_{DD}	23
GTM2_TIN1/GPIO2[18]	V1	I	OV_{DD}	23
GTM2_TGATE1/ GPIO2[19]	W1	I	OV_{DD}	23
GTM2_TOUT1/GPIO2[20]	V3	O	OV_{DD}	23
PCI Signals[4]				
PCI_AD[31:0]	M1, M2, M3, M4, M5,M7, L1, L6, J1, K2, K3, K4, K5, K6, K7, H1, H7, G1, G2, G3, G4, G5, G6, F1, F4, F6, F7, F8, D2, D3, E1, E2	I/O	OV_{DD}	
PCI_C/BE[3:0]	L2, J2, H6, F2	I/O	OV_{DD}	
PCI_PAR	H5	I/O	OV_{DD}	
PCI_FRAME	J3	I/O	OV_{DD}	
PCI_TRDY	J6	I/O	OV_{DD}	

Table 1. Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
PCI_IRDY	J5	I/O	OV_{DD}	
PCI_STOP	E4	I/O	OV_{DD}	
PCI_DEVSEL	J7	I/O	OV_{DD}	
PCI_IDSEL	L5	I	OV_{DD}	
PCI_PERR	H2	I/O	OV_{DD}	
PCI_SERR	H3	I/O	OV_{DD}	
PCI_REQ0	N3	I/O	OV_{DD}	
PCI_REQ1/GPIO1[0]	N1	I/O	OV_{DD}	23
PCI_REQ2/GPIO1[2]	P3	I/O	OV_{DD}	23
PCI_REQ3/GPIO1[4]	P1	I/O	OV_{DD}	23
PCI_REQ4/GPIO1[6]	P2	I/O	OV_{DD}	23
PCI_GNT0	N2	I/O	OV_{DD}	
PCI_GNT1/GPIO1[1]	T1	I/O	OV_{DD}	23
PCI_GNT2/GPIO1[3]	T2	I/O	OV_{DD}	23
PCI_GNT3/GPIO1[5]	R1	I/O	OV_{DD}	23
PCI_GNT4/GPIO1[7]	R2	I/O	OV_{DD}	23
PCI_CLK	C1	I	OV_{DD}	
SerDes 1 Signals				
SD1_TX[3:0]	J13, G12, F10, H9	O	$X1V_{DD}$	
SD1_TX[3:0]	H13, F12, G10, J9	O	$X1V_{DD}$	
SD1_RX[3:0]	B9, D8, D5, B4	I	$S1V_{DD}$	
SD1_RX[3:0]	A9, C8, C5, A4	I	$S1V_{DD}$	
SD1_REF_CLK	A7	I	$S1V_{DD}$	
SD1_REF_CLK	B7	I	$S1V_{DD}$	
SD1_PLL_TPD	C7	O	$X1V_{DD}$	9, 10
SD1_PLL_TPA	B6	Analog	$S1V_{DD}$	9, 11
SD1_IMP_CAL_TX	E11	Analog	$X1V_{DD}$	7
SD1_IMP_CAL_RX	B3	Analog	$S1V_{DD}$	8
SerDes 2 Signals				
SD2_TX[7:0]	F22, J21, F20, H19, J17, G16, H15, G14	O	$X2V_{DD}$	
SD2_TX[7:0]	G22, H21, G20, J19, H17, F16, J15, F14	O	$X2V_{DD}$	
SD2_RX[7:0]	B22, D21, B20, D19, C15, B14, C13, A12	I	$S2V_{DD}$	
SD2_RX[7:0]	A22, C21, A20, C19, D15, A14, D13, B12	I	$S2V_{DD}$	
SD2_REF_CLK	A18	I	$S2V_{DD}$	

Table 1. Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
No Connects	B1, B10, C2, C3, E22, F18, G11, G18, H8, H11, H14, J11, AA1, AA2, AA3, AA4	—	—	16
Power and Ground Signals				
MV_{REF}	AE14	DDR2 reference voltage	$GV_{DD}/2$	
OV_{DD}	C24, C26, D1, E25, F3, G7, G25, H4, J24, K1, L4, L7, N5, P10, P7, T4, T8, V5, V8	LCD, general purpose timer, PCI, MPIC, I^2C, DUART, IrDA, SPI, DMA, system control, clocking, debug, test, JTAG, & power management I/O supply	OV_{DD}	
GV_{DD}	Y2, Y16, AA7, AA24, AA26, AB14, AB17, AC2, AC5, AC6, AC9, AC12, AC18, AC21, AC24, AC27, AE4, AE7, AE10, AE13, AE16, AE19, AE22, AE25, AF2, AG5, AG8, AG11, AG14, AG17, AG20, AG23, AG26, AH1	DDR SDRAM I/O supply	GV_{DD}	
BV_{DD}	L27, M20, M24, P18, P22, P26, U19, U27, V24, W21, AA20	eLBC & SSI I/O voltage	BV_{DD}	
$S1V_{DD}$	A3, A10, B5, B8, D4, D7	Receiver and SerDes core power supply for port 1	$S1V_{DD}$	
$S2V_{DD}$	A11, A15, A19, A23, B13, B17, B21, C14, C18, D12, D16, D20	Receiver and SerDes core power supply for port 2	$S2V_{DD}$	
$X1V_{DD}$	F11, G9, H12, J10, K13	Transmitter power supply for SerDes port 1	$X1V_{DD}$	
$X2V_{DD}$	F13, F17, F21, G15, G19, H18, H22, J16, J20	Transmitter power supply for SerDes port 2	$X2V_{DD}$	
$L1V_{DD}$	K14	Digital logic power supply for SerDes port 1	$L1V_{DD}$	
$L2V_{DD}$	K16, K18	Digital logic power supply for SerDes port 2	$L2V_{DD}$	

2 Electrical Characteristics

This section provides the AC and DC electrical specifications for the MPC8610. The MPC8610 is currently targeted to these specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 2 provides the absolute maximum ratings.

Table 2. Absolute Maximum Ratings[1]

Characteristic		Symbol	Recommended Value	Unit	Notes
Core supply voltages		V_{DD}_Core	–0.3 to 1.21	V	
Core PLL supply		AV_{DD}_Core	–0.3 to 1.21	V	
SerDes receiver and core power supply (ports 1 and 2)		$S1V_{DD}$ $S2V_{DD}$	–0.3 to 1.21	V	
SerDes transmitter power supply (ports 1 and 2)		$X1V_{DD}$ $X2V_{DD}$	–0.3 to 1.21	V	
SerDes digital logic power supply (ports 1 and 2)		$L1V_{DD}$ $L2V_{DD}$	–0.3 to 1.21	V	
Serdes PLL supply voltage (ports 1 and 2)		$SD1AV_{DD}$ $SD2AV_{DD}$	–0.3 to 1.21	V	
Platform supply voltage		V_{DD}_PLAT	–0.3 to 1.21	V	
PCI and platform PLL supply voltage		AV_{DD}_PCI AV_{DD}_PLAT	–0.3 to 1.21	V	
DDR/DDR2 SDRAM I/O supply voltages		GV_{DD}	–0.3 to 2.75	V	
Local bus and SSI I/O voltage		BV_{DD}	–0.3 to 3.63	V	
LCD, PCI, general purpose timer, MPIC, IrDA, DUART, DMA, interrupts, system control and clocking, debug, test, JTAG, power management, I^2C, SPI, and miscellaneous I/O voltage		OV_{DD}	–0.3 to 3.63	V	
Input voltage	DDR/DDR2 SDRAM signals	MV_{IN}	(GND – 0.3) to (GV_{DD} + 0.3)	V	2
	DDR/DDR2 SDRAM reference	MV_{REF}	(GND – 0.3) to (GV_{DD}/2 + 0.3)	V	2
	Local bus I/O voltage	BV_{IN}	(GND – 0.3) to (BV_{DD} + 0.3)	V	2
	LCD, PCI, general purpose, MPIC, IrDA, DUART, DMA, interrupts, system control and clocking, debug, test, JTAG, power management, I^2C, SPI and miscellaneous I/O voltage	OV_{IN}	(GND – 0.3) to (OV_{DD} + 0.3)	V	2

2.3 Power Characteristics

The power dissipation for the MPC8610 device is shown in Table 5.

Table 5. MPC8610 Power Dissipation

Power Mode	Core/Platform Frequency (MHz)	V_{DD}_Core, V_{DD}_PLAT (V)	Junction Temperature (°C)	Power (Watts)	Notes
Typical	1333/533	1.025	65	10.7	1, 2
Thermal			105	12.1	1, 3
Maximum				16	1, 4
Typical	1066/533	1.00	65	8.4	1, 2
Thermal			105	9.8	1, 3
Maximum				13	1, 4
Typical	800/400	1.00	65	5.8	1, 2
Thermal			105	7.2	1, 3
Maximum				9.5	1, 4

Notes:

1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.
2. Typical power is an average value measured at the nominal recommended core voltage (V_{DD}_Core) and 65°C junction temperature (see Table 3) while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz with the core at 100% efficiency. This parameter is not 100% tested but periodically sampled.
3. Thermal power is the average power measured at nominal core voltage (V_{DD}_Core) and maximum operating junction temperature (see Table 3) while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz on the core and a typical workload on platform interfaces. This parameter is not 100% tested but periodically sampled.
4. Maximum power is the maximum power measured at nominal core voltage (V_{DD}_Core) and maximum operating junction temperature (see Table 3) while running a test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep all the execution units maximally busy on the core.

The estimated maximum power dissipation for individual power supplies of the MPC8610 is shown in Table 6.

Table 6. MPC8610 Individual Supply Maximum Power Dissipation[1]

Component Description	Supply Voltage (V)	Est. Power (Watts)	Notes
Core voltage supply	V_{DD}_Core = 1.025 V @ 1333 MHz	14.0	
	V_{DD}_Core = 1.00 V @ 1066 MHz	12.0	
Core PLL voltage supply	AV_{DD}_Core = 1.025 V @ 1333 MHz	0.0125	
	AV_{DD}_Core = 1.00 V @ 1066 MHz	0.0125	
Platform source supply	V_{DD}_PLAT = 1.025 V @ 1333 MHz	4.5	
	V_{DD}_PLAT = 1.00 V @ 1066 MHz	4.3	

Table 30. I^2C DC Electrical Characteristics (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max)	I_I	–10	10	µA	3
Capacitance for each I/O pin	C_I	—	10	pF	

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. Refer to the *MPC8610 Integrated Host Processor Reference Manual*, for information on the digital filter used.
3. I/O pins will obstruct the SDA and SCL lines if OV_{DD} is switched off.

2.9.2 I^2C AC Electrical Specifications

Table 31 provides the AC timing parameters for the I^2C interfaces.

Table 31. I^2C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 30).

Parameter	Symbol[1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}[4]	1.3	—	µs
High period of the SCL clock	t_{I2CH}[4]	0.6	—	µs
Setup time for a repeated START condition	t_{I2SVKH}[4]	0.6	—	µs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}[4]	0.6	—	µs
Data setup time	t_{I2DVKH}[4]	100	—	ns
Data input hold time: CBUS compatible masters I^2C bus devices	t_{I2DXKL}	 — 0[2]	 — —	µs
Data ouput delay time	t_{I2OVKL}	—	0.9 [3]	µs
Setup time for STOP condition	t_{I2PVKH}	0.6	—	µs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V

2.12.2.4 SSI Receiver Timing with External Clock

Table 38 provides the receiver timing parameters with external clock.

Table 38. SSI Receiver with External Clock Timing Parameters

Parameter	Symbol	Min	Max	Unit
External Clock Operation				
(Tx/Rx) CK clock period	SS22	81.4	—	ns
(Tx/Rx) CK clock high period	SS23	36.0	—	ns
(Tx/Rx) CK clock rise time	SS24	—	6.0	ns
(Tx/Rx) CK clock low period	SS25	36.0	—	ns
(Tx/Rx) CK clock fall time	SS26	—	6.0	ns
(Rx) CK high to FS high	SS32	–10.0	15.0	ns
(Rx) CK high to FS low	SS34	10.0	—	ns
(Tx/Rx) external FS rise time	SS35	—	6.0	ns
(Tx/Rx) external FS fall time	SS36	—	6.0	ns
SRXD setup time before (Rx) CK low	SS40	10.0	—	ns
SRXD hold time after (Rx) CK low	SS41	2.0	—	ns

Figure 20 provides the SSI receiver timing with external clock.

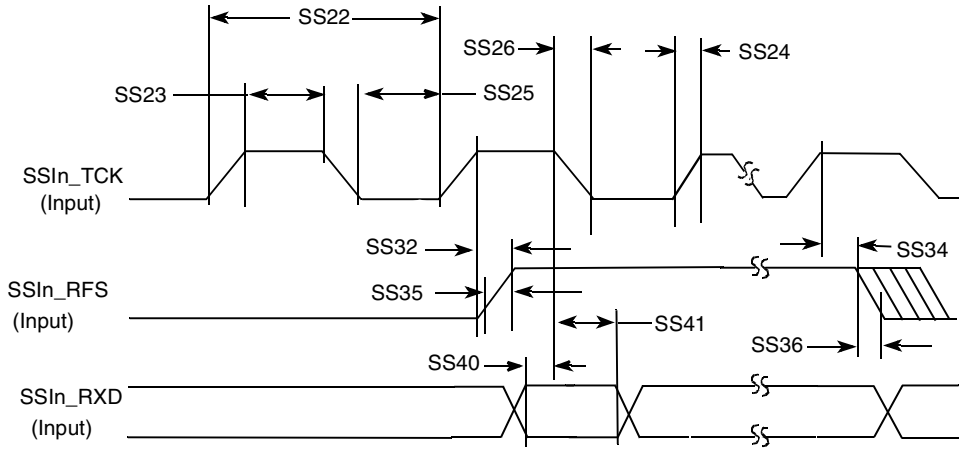


Figure 20. SSI Receiver with External Clock Timing Diagram

Figure 23 provides the AC test load for the SPI.

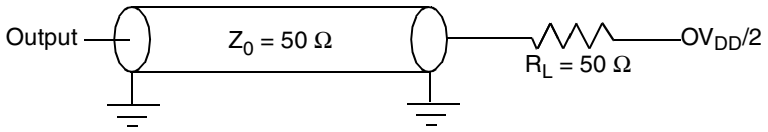
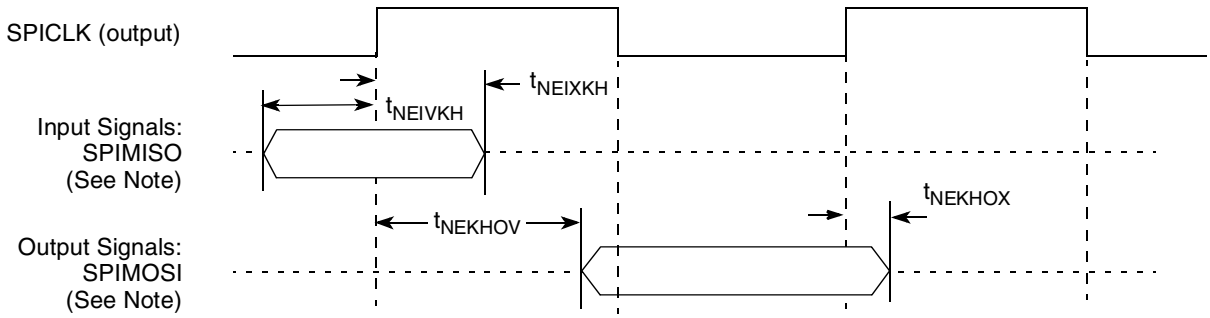


Figure 23. SPI AC Test Load

Figure 24 through Figure 25 represent the AC timings from Table 44. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

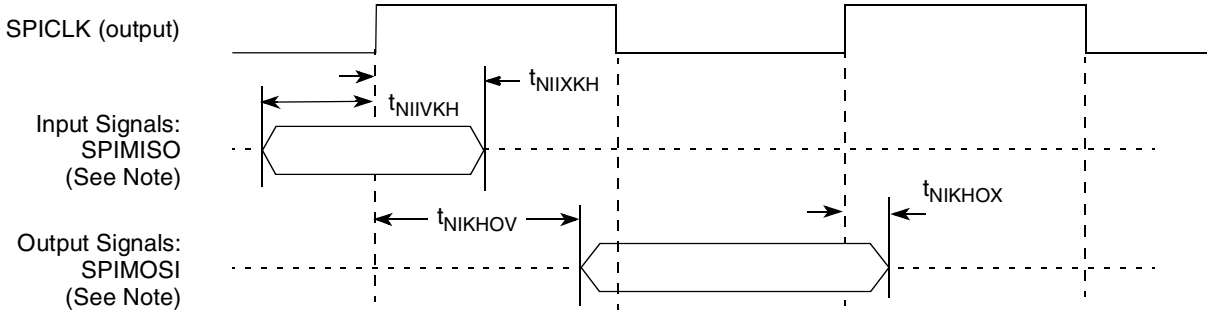
Figure 24 shows the SPI timings in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 24. SPI AC Timing in Slave Mode (External Clock) Diagram

Figure 25 shows the SPI timings in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 25. SPI AC Timing in Master Mode (Internal Clock) Diagram

2.16 PCI Interface

This section describes the DC and AC electrical specifications for the PCI bus interface.

2.16.1 PCI DC Electrical Characteristics

Table 45 provides the DC electrical characteristics for the PCI interface.

Table 45. PCI DC Electrical Characteristics[1]

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN} [2] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –100 μA)	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 μA)	V_{OL}	—	0.2	V

Notes:
1. Ranges listed do not meet the full range of the DC specifications of the *PCI 2.2 Local Bus Specifications*.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2 and Table 3.

2.16.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus. Note that the SYSCLK signal is used as the PCI input clock. Table 46 provides the PCI AC timing specifications at 66 MHz.

Table 46. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol[1]	Min	Max	Unit	Notes
SYSCLK to output valid	t_{PCKHOV}	1.5	7.4	ns	2, 3, 12
SYSCLK to output high impedance	t_{PCKHOZ}	—	14	ns	2, 4, 11
Input setup to SYSCLK	t_{PCIVKH}	3.7	—	ns	2, 5, 10, 13
Input hold from SYSCLK	t_{PCIXKH}	0.8	—	ns	2, 5, 10, 14
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ [9] setup time	t_{PCRVRH}	$10 \times t_{SYS}$	—	clocks	6, 7, 11
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	7, 11

— For external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SGND). Figure 32 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

- Single-ended mode
  — The reference clock can also be single-ended. The SD*n*_REF_CLK input amplitude (single-ended swing) must be between 400 and 800 mV peak-peak (from V_{min} to V_{max}) with $\overline{\text{SD}n\text{\_REF\_CLK}}$ either left unconnected or tied to ground.
  — The SD*n*_REF_CLK input average voltage must be between 200 and 400 mV. Figure 33 shows the SerDes reference clock input requirement for single-ended signaling mode.
  — To meet the input amplitude requirement, the reference clock inputs might need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase ($\overline{\text{SD}n\text{\_REF\_CLK}}$) through the same source impedance as the clock input (SD*n*_REF_CLK) in use.

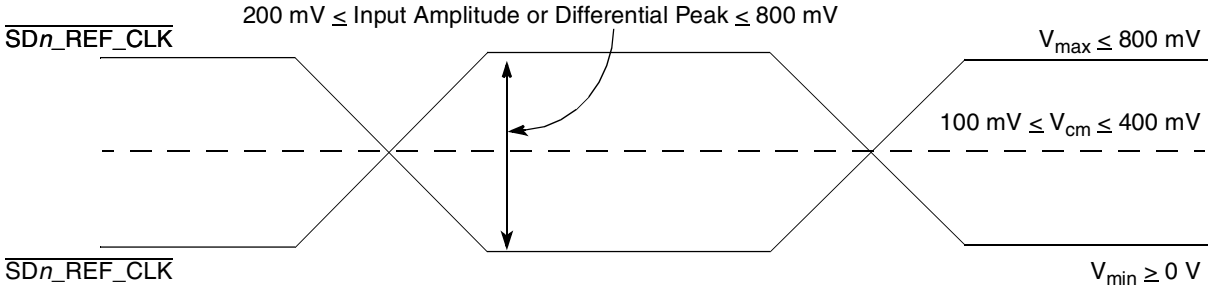


Figure 31. Differential Reference Clock Input DC Requirements (External DC-Coupled)

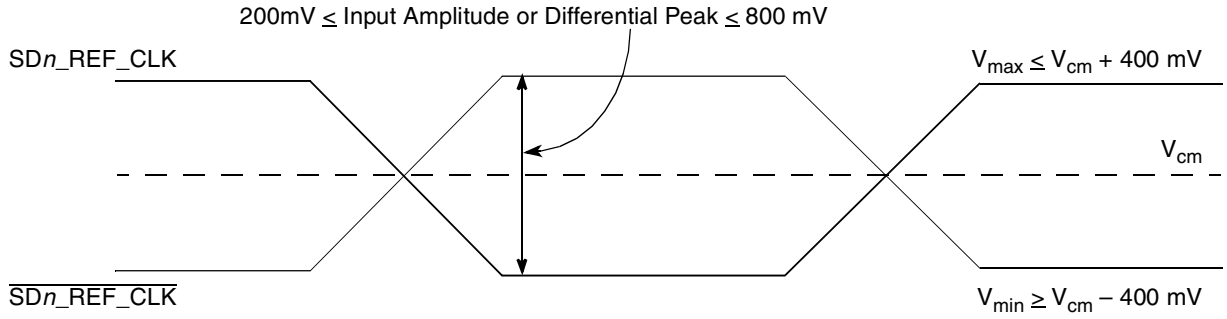


Figure 32. Differential Reference Clock Input DC Requirements (External AC-Coupled)

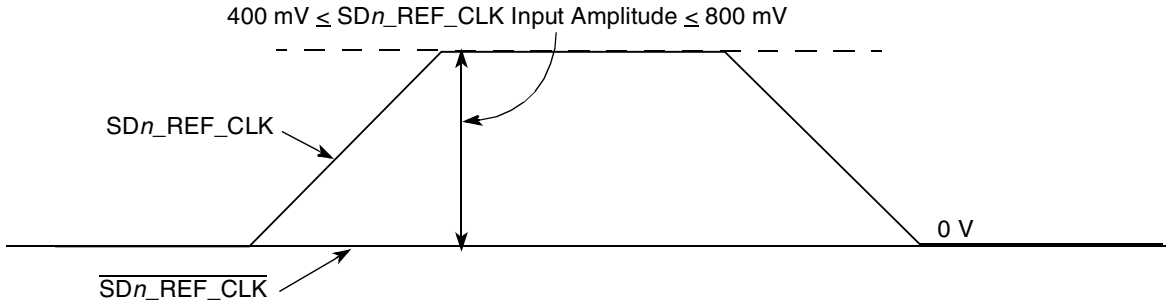


Figure 33. Single-Ended Reference Clock Input DC Requirements

Table 50. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$V_{RX-CM-ACp}$	AC peak common mode input voltage			150	mV	$V_{RX-CM-ACp} = \lvert V_{RXD+} - V_{RXD-}\rvert/2 - V_{RX-CM-DC}$ $V_{RX-CM-DC} = DC_{(avg)}$ of $\lvert V_{RX-D+} - V_{RX-D-}\rvert/2$ See Note 2
$RL_{RX-DIFF}$	Differential return loss	15			dB	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at +300 and –300 mV, respectively. See Note 4
RL_{RX-CM}	Common mode return loss	6			dB	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at 0 V. See Note 4
$Z_{RX-DIFF-DC}$	DC differential input impedance	80	100	120	Ω	RX DC differential mode impedance. See Note 5
Z_{RX-DC}	DC input impedance	40	50	60	Ω	Required RX D+ as well as D– DC impedance (50 ± 20% tolerance). See Notes 2 and 5
$Z_{RX-HIGH-IMP-DC}$	Powered down DC input impedance	200 k			Ω	Required RX D+ as well as D– DC Impedance when the receiver terminations do not have power. See Note 6
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65		175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2*\lvert V_{RX-D+} - V_{RX-D-}\rvert$ Measured at the package pins of the receiver
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected electrical idle enter detect threshold integration time			10	ms	An unexpected Electrical Idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition.

NOTE

The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (i.e., as measured by a vector network analyzer with 50-Ω probes—see Figure 43). Note that the series capacitors, CTX, are optional for the return loss measurement.

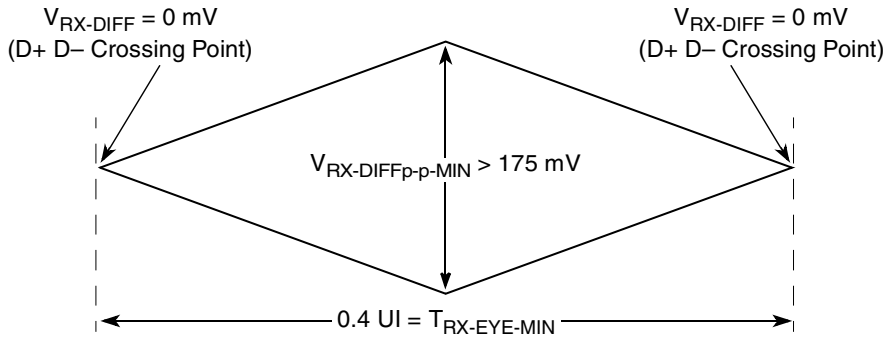


Figure 42. Minimum Receiver Eye Timing and Voltage Compliance Specification

2.18.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 43.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

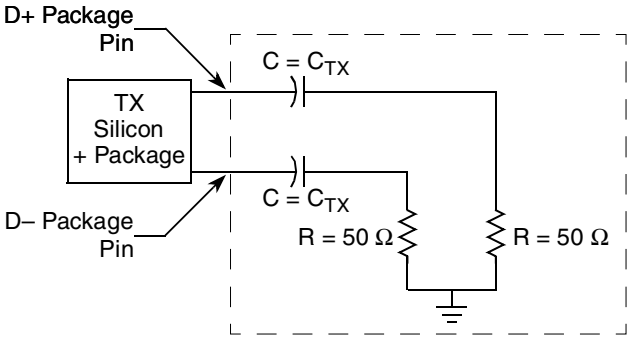


Figure 43. Compliance Test/Measurement Load

2.19 JTAG

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8610.

2.19.1 JTAG DC Electrical Characteristics

Table 51 provides the JTAG DC electrical characteristics for the JTAG interface.

Table 51. JTAG DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN}[1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = mn, I_{OH} = –100 μA)	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 μA)	V_{OL}	—	0.2	V

Note:
1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2 and Table 3.

2.19.2 JTAG AC Electrical Specifications

Table 52 provides the JTAG AC timing specifications as defined in Figure 45 through Figure 47.

Table 52. JTAG AC Timing Specifications (Independent of SYSCLK)[1]

At recommended operating conditions (see Table 3).

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	
JTAG external clock cycle time	t_{JTG}	30	—	ns	
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	6
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 0	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 20 25	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 4 4	 20 25	ns	5
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 30 30	 — —	ns	5

3.1.1 Clock Ranges

Table 53 provides the clocking specifications for the processor core.

Table 53. Processor Core Clocking Specifications

Characteristic	Maximum Processor Core Frequency						Unit	Notes
	800 MHz		1066 MHz		1333 MHz			
	Min	Max	Min	Max	Min	Max		
e600 core processor frequency	666	800	666	1066	666	1333	MHz	1, 2, 3

Notes:
1. **Caution:** The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 3.1.2, "Platform/MPX to SYSCLK PLL Ratio" and Section 3.1.3, "e600 Core to MPX/Platform Clock PLL Ratio," for ratio settings.
2. The minimum e600 core frequency is based on the minimum platform clock frequency of 333 MHz.
3. The reset config pin cfg_core_speed must be pulled low if the core frequency is 800 MHz or below.

Table 54 provides the clocking specifications for the memory bus.

Table 54. Memory Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	800, 1066, 1333 MHz			
	Min	Max		
Memory bus clock frequency	166	266	MHz	1, 2

Notes:
1. **Caution:** The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 3.1.2, "Platform/MPX to SYSCLK PLL Ratio."
2. The memory bus clock speed is half the DDR/DDR2 data rate, hence, half the MPX clock frequency.

Table 55 provides the clocking specifications for the local bus.

Table 55. Local Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	800, 1066, 1333 MHz			
	Min	Max		
Local bus clock speed	22	133	MHz	1

Note:
1. The local bus clock speed on LCLK[0:2] is determined by the MPX clock divided by the local bus ratio programmed in LCRR[CLKDIV]. Refer to the *MPC8610 Integrated Host Processor Reference Manual,* for more information.

3.2 Power Supply Design and Sequencing

3.2.1 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD}_Plat, AV_{DD}_Core, AV_{DD}_PCI, and SD*n*AV_{DD}, respectively). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages will be derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply, one to each of the AV_{DD} type pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} type pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} type pin, which is on the periphery of 783 FC-PBGA the footprint, without the inductance of vias.

Figure 48 shows the filter circuit for the platform PLL power supplies (AV_{DD}_PLAT).

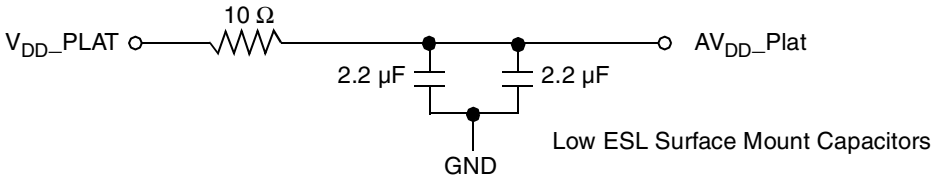


Figure 48. MPC8610 PLL Power Supply Filter Circuit (for Platform)

Figure 49 shows the filter circuit for the core PLL power supply (AV_{DD}_Core).

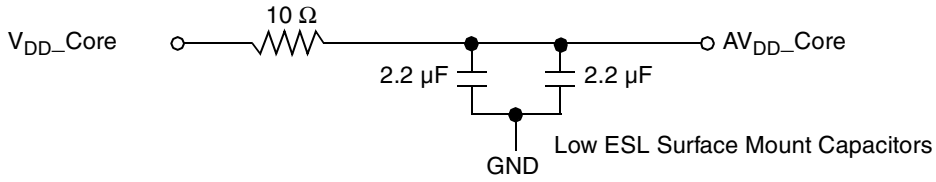
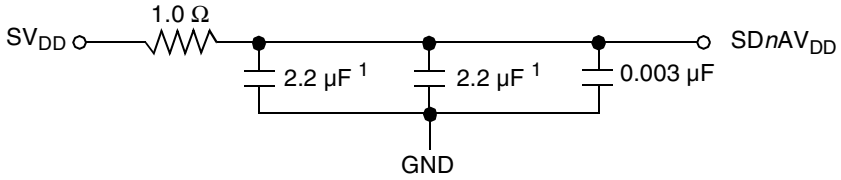


Figure 49. MPC8610 PLL Power Supply Filter Circuit (for Core)

The SD*n*AV_{DD} signals provide power for the analog portions of the SerDes PLLs. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in Figure 50. For maximum effectiveness, the filter circuit is placed as closely as possible to the SD*n*AV_{DD} balls to ensure it filters out as much noise as possible. The ground connection should be near the SD*n*AV_{DD} balls. The 0.003-µF capacitor is closest to the balls, followed by the two 2.2-µF capacitors, and finally the 1 ohm resistor to the board supply plane. The capacitors are connected from SD*n*AV_{DD} to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.



1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 50. SerDes PLL Power Supply Filter

To reduce the die-junction temperature, heat sinks are required; due to the potential large mass of the heat sink, attachment through the printed-circuit board is suggested. In any implementation of a heat sink solution, the force on the die should not exceed ten pounds force (45 newtons). Figure 54 shows a spring clip through the board. Occasionally the spring clip is attached to soldered hooks or to a plastic backing structure. Screw and spring arrangements are also frequently used.

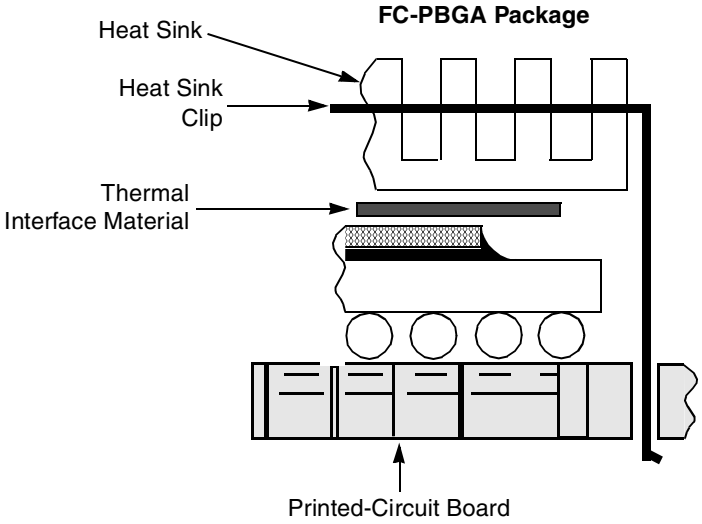


Figure 54. FC-PBGA Package Exploded Cross-Sectional View with Several Heat Sink Options

Suitable heat sinks are commercially available from the following vendors:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Advanced Thermal Solutions 89 Access Road #27. Norwood, MA02062 Internet: www.qats.com	781-769-2800
Alpha Novatech 473 Sapena Ct. #12 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-749-7601
Calgreg Thermal Solutions 60 Alhambra Road, Suite 1 Warwick, RI 02886 Internet: www.calgreg.com	888-732-6100
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-thermal.com	408-436-8770

Table 63. Part Numbering Nomenclature

MC	nnnn	w	xx	yyyy	M	z
Product Code	**Part Identifier**	**Temp [3]**	**Package [1]**	**Core Processor Frequency[2] (MHz)**	**DDR Speed (MHz)**	**Product Revision Level**
MC	8610	T = –40° to 105°C	PX = Leaded sphere FC-PBGA VT = RoHS lead free FC-PBGA	1066, 800	J = 533 MHz G = 400 MHz	Revision B = 1.1 System Version Register Value for Rev B: 0x80A0_0011—MPC8610
		Blank = 0 to 105°C		1333, 1066, 800		

Notes:
1. See Section 5, “Package Information,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
3. Extended temperature range devices are offered only with core frequencies of 1066 and 800 MHz.

Table 64 shows the parts that are available for ordering and their operating conditions.

Table 64. Part Offerings and Operating Conditions

Part Offerings[1]	Operating Conditions
MC8610xx1333Jz	Max CPU speed = 1333 MHz, Max DDR = 533 MHz
MC8610xx1066Jz	Max CPU speed = 1066 MHz, Max DDR = 533 MHz
MC8610Txx1066Jz	Max CPU speed = 1066 MHz, Max DDR = 533 MHz extended Temperature Rating
MC8610xx800Gz	Max CPU speed = 800 MHz, Max DDR = 400 MHz
MC8610Txx800Gz	Max CPU speed = 800 MHz, Max DDR = 400 MHz Extended temperature rating

Note:
[1] The xx in the part marking represents the package option.The ‘T’ represents the extended temperature rating. The ‘z’ represents the revision letter. For more information see Table 63.

6 Product Documentation

The following documents are required for a complete description of the device and are needed to design properly with the part.

- *MPC8610 Integrated Host Processor Reference Manual* (document number: MPC8610RM)
- *e600 PowerPC Core Reference Manual* (document number: E600CORERM)

7 Revision History

Table 65 summarizes revisions to this document.

Table 65. Revision History

Rev. No.	Date	Substantive Change(s)
2	1/2009	• Updated Table of Contents • Removed subheading Section 1.1. pin assignments. • Promoted section 4.3, “Ordering Information,” and associated subsections to Section 4, “Ordering Information.” Renumbered subsequent sections and subsections accordingly.
1	01/2009	• Updated Table of Contents • Removed Serial Rapid IO from Section 2.4.4, “Platform Frequency Requirements for PCI-Express” because SRIO is not available on MPC8610. • Removed note in Table 21 and Table 22 that states “Minimum DDR2 frequency is 400 MHz.” • In Table 31, removed rows for t_{i2cr} and t_{i2CF}. Added row for Cb. • Replaced 1067 with 1066 in Table 63. • Replaced CBGA with PBGA in Section 5.1, “Package Parameters for the MPC8610.”
0	10/2008	Initial release.

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