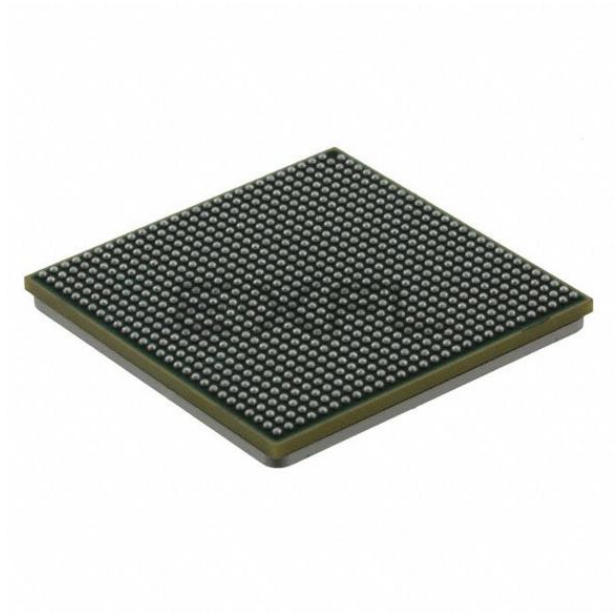

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e600 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 1.066GHz |
| Co-Processors/DSP | - |
| RAM Controllers | DDR, DDR2 |
| Graphics Acceleration | No |
| Display & Interface Controllers | DIU, LCD |
| Ethernet | - |
| SATA | - |
| USB | - |
| Voltage - I/O | 1.8V, 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | - |
| Package / Case | 783-BBGA, FCBGA |
| Supplier Device Package | 783-FCPBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8610px1066jb |

**Table 1. Signal Reference by Functional Block (continued)**

| Name[1] | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| LAD[0:31] | AA21, AA22, AA23, Y21, Y22, Y23, Y24, W23, W24, W25, V28, V27, V25, V23, V21, W22, U28, U26, U24, U22, U23, U20, U21, W20, V20, T24, T25, T27, T26, T21, T22, T23 | I/O | $BV_{DD}$ | 20 |
| LDP[0:3]/LA[6:9] | N28, M28, L28, P25 | I/O | $BV_{DD}$ | |
| LA10/SSI1_TXD | P19 | O | $BV_{DD}$ | 20, 23 |
| LA11/SSI1_TFS | M27 | O | $BV_{DD}$ | 23 |
| LA12/SSI1_TCK | U18 | O | $BV_{DD}$ | 23 |
| LA13/SSI1_RCK | P28 | O | $BV_{DD}$ | 23 |
| LA14/SSI1_RFS | R18 | O | $BV_{DD}$ | 23 |
| LA15/SSI1_RXD | R19 | O | $BV_{DD}$ | 23 |
| LA16/SSI2_TXD | R20 | O | $BV_{DD}$ | 23 |
| LA17/SSI2_TFS | M18 | O | $BV_{DD}$ | 23 |
| LA18/SSI2_TCK | N18 | O | $BV_{DD}$ | 23 |
| LA19/SSI2_RCK | N27 | O | $BV_{DD}$ | 23 |
| LA20/SSI2_RFS | P20 | O | $BV_{DD}$ | 23 |
| LA21/SSI2_RXD | P21 | O | $BV_{DD}$ | 23 |
| LA[22:31] | M19, M21, M22, M23, N23, N24, M26, N20, N21, N22 | O | $BV_{DD}$ | 20 |
| $\overline{\text{LCS}}$[0:4] | R24, R22, P23, P24, P27 | O | $BV_{DD}$ | 21 |
| $\overline{\text{LCS5}}$/$\overline{\text{DMA2\_DREQ0}}$ | R23 | O | $BV_{DD}$ | 21, 22, 23 |
| $\overline{\text{LCS6}}$/$\overline{\text{DMA2\_DACK0}}$ | N26 | O | $BV_{DD}$ | 21, 23 |
| $\overline{\text{LCS7}}$/$\overline{\text{DMA2\_DDONE0}}$ | R26 | O | $BV_{DD}$ | 21, 23 |
| $\overline{\text{LWE0}}$/$\overline{\text{LFWE}}$/$\overline{\text{LBS0}}$ | T19 | O | $BV_{DD}$ | 20 |
| $\overline{\text{LWE1}}$/$\overline{\text{LBS1}}$ | T20 | O | $BV_{DD}$ | 20 |
| $\overline{\text{LWE2}}$/$\overline{\text{LBS2}}$ | W19 | O | $BV_{DD}$ | 20 |
| $\overline{\text{LWE3}}$/$\overline{\text{LBS3}}$ | T18 | O | $BV_{DD}$ | 20 |
| LBCTL | T28 | O | $BV_{DD}$ | 20 |
| LALE | R28 | O | $BV_{DD}$ | 20 |
| LGPL0/LFCLE | L19 | O | $BV_{DD}$ | 20 |
| LGPL1/LFALE | L20 | O | $BV_{DD}$ | 20 |
| LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$ | L21 | O | $BV_{DD}$ | 20 |
| LGPL3/$\overline{\text{LFWP}}$ | L22 | O | $BV_{DD}$ | 20 |
| $\overline{\text{LGTA}}$/LFR$\overline{\text{B}}$/LGPL4/ LUPWAIT/LPBSE | L23 | I/O | $BV_{DD}$ | 24 |

**Table 1. Signal Reference by Functional Block (continued)**

| Name[1] | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| LGPL5 | L24 | O | $BV_{DD}$ | |
| LCLK[0:2] | R25, M25, L26 | O | $BV_{DD}$ | |
| **DIU/LCD Signals[4]** | | | | |
| DIU_LD[23:16]/ GPIO1[15:8] | R3, R10, T10, N7, N4, P6, P5, P4 | O | $OV_{DD}$ | 5, 23 |
| DIU_LD[15:0]/ GPIO1[31:16] | T3, R9, T9, R8, R7, R6, R4, T7, U5, T6, T5, W4, W5, W6, V4, V6 | O | $OV_{DD}$ | 5, 14, 20, 23 |
| DIU_VSYNC | V7 | O | $OV_{DD}$ | 20 |
| DIU_HSYNC | U7 | O | $OV_{DD}$ | 20 |
| DIU_DE | U4 | O | $OV_{DD}$ | 20 |
| DIU_CLK_OUT | N6 | O | $OV_{DD}$ | |
| **Programmable Interrupt Controller (PIC) Signals[4]** | | | | |
| IRQ[0:5] | L25, J23, K26, E23, K28, K22 | I | $OV_{DD}$ | |
| IRQ6/$\overline{\text{DMA1\_DREQ0}}$ | G27 | I | $OV_{DD}$ | 22, 23 |
| IRQ7/$\overline{\text{DMA1\_DACK0}}$ | J25 | I | $OV_{DD}$ | 23 |
| IRQ8/$\overline{\text{DMA1\_DDONE0}}$ | J27 | I | $OV_{DD}$ | 23 |
| IRQ9/$\overline{\text{DMA1\_DREQ3}}$ | H26 | I | $OV_{DD}$ | 22, 23 |
| IRQ10/$\overline{\text{DMA1\_DACK3}}$ | J26 | I | $OV_{DD}$ | 23 |
| IRQ11/$\overline{\text{DMA1\_DDONE3}}$ | K27 | I | $OV_{DD}$ | 23 |
| $\overline{\text{IRQ\_OUT}}$ | K23 | O | $OV_{DD}$ | 21, 25 |
| $\overline{\text{MCP}}$ | A24 | I | $OV_{DD}$ | |
| $\overline{\text{SMI}}$ | B24 | I | $OV_{DD}$ | |
| **$I^2C$ Signals** | | | | |
| IIC1_SDA/GPIO2[10] | D24 | I/O | $OV_{DD}$ | 21, 23, 25 |
| IIC1_SCL/GPIO2[9] | E24 | I/O | $OV_{DD}$ | 21, 23, 25 |
| IIC2_SDA/$\overline{\text{SPISEL}}$/ GPIO2[12] | E27 | I/O | $OV_{DD}$ | 21, 23, 25 |
| IIC2_SCL/SPICLK/ GPIO2[11] | E28 | I/O | $OV_{DD}$ | 21, 23, 25 |
| **DUART Signals[4]** | | | | |
| UART_SIN0/SPIMOSI/ GPIO2[5] | K24 | I | $OV_{DD}$ | 23 |
| UART_SOUT0/SPIMISO | H25 | O | $OV_{DD}$ | 23 |
| $\overline{\text{UART\_CTS0}}$/GPIO2[6] | G24 | I | $OV_{DD}$ | 23 |
| $\overline{\text{UART\_RTS0}}$ | G26 | O | $OV_{DD}$ | 20 |

**Table 1. Signal Reference by Functional Block (continued)**

| Name[1] | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| UART_SIN1/IR2_RXD/ GPIO2[7] | F25 | I | $OV_{DD}$ | 23 |
| UART_SOUT1/IR2_TXD | H24 | O | $OV_{DD}$ | 23 |
| $\overline{\text{UART_CTS}}$1/GPIO2[8] | C23 | I | $OV_{DD}$ | 23 |
| $\overline{\text{UART_RTS}}$1 | D23 | O | $OV_{DD}$ | |
| **IrDA Signals[4]** | | | | |
| IR1_TXD/GPIO2[13] | F27 | O | $OV_{DD}$ | 23 |
| IR1_RXD/GPIO2[14] | E26 | I | $OV_{DD}$ | 23 |
| IR_CLKIN | F28 | I | $OV_{DD}$ | |
| IR2_TXD/UART_SOUT1 | H24 | O | $OV_{DD}$ | 23 |
| IR2_RXD/UART_SIN1/ GPIO2[7] | F25 | I | $OV_{DD}$ | 23 |
| **SPI Signals** | | | | |
| SPIMOSI/UART_SIN0/ GPIO2[5] | K24 | I/O | $OV_{DD}$ | 23 |
| SPIMISO/UART_SOUT0 | H25 | I/O | $OV_{DD}$ | 23 |
| $\overline{\text{SPISEL}}$/IIC2_SDA/ GPIO2[12] | E27 | I | $OV_{DD}$ | 23 |
| SPICLK/IIC2_SCL/ GPIO2[11] | E28 | I | $OV_{DD}$ | 23 |
| **SSI Signals[3, 6]** | | | | |
| SSI1_RXD/LA15 | R19 | I | $BV_{DD}$ | 23 |
| SSI1_TXD/LA10 | P19 | O | $BV_{DD}$ | 23 |
| SSI1_RFS/LA14 | R18 | I/O | $BV_{DD}$ | 23 |
| SSI1_TFS/LA11 | M27 | I/O | $BV_{DD}$ | 23 |
| SSI1_RCK/LA13 | P28 | I/O | $BV_{DD}$ | 23 |
| SSI1_TCK/LA12 | U18 | I/O | $BV_{DD}$ | 23 |
| SSI2_RXD/LA21 | P21 | I | $BV_{DD}$ | 23 |
| SSI2_TXD/LA16 | R20 | O | $BV_{DD}$ | 23 |
| SSI2_RFS/LA20 | P20 | I/O | $BV_{DD}$ | 23 |
| SSI2_TFS/LA17 | M18 | I/O | $BV_{DD}$ | 23 |
| SSI2_RCK/LA19 | N27 | I/O | $BV_{DD}$ | 23 |
| SSI2_TCK/LA18 | N18 | I/O | $BV_{DD}$ | 23 |
| **DMA Signals[4]** | | | | |
| $\overline{\text{DMA1\_DREQ0}}$/IRQ6/ GPIO2[24] | G27 | I | $OV_{DD}$ | 22, 23 |

**Table 1. Signal Reference by Functional Block (continued)**

| Name[1] | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| $\overline{\text{SD2\_REF\_CLK}}$ | B18 | I | $S2V_{DD}$ | |
| SD2_PLL_TPD | D17 | O | $X2V_{DD}$ | 9, 10 |
| SD2_PLL_TPA | C17 | Analog | $S2V_{DD}$ | 9, 11 |
| SD2_IMP_CAL_TX | E21 | Analog | $X2V_{DD}$ | 7 |
| SD2_IMP_CAL_RX | B11 | Analog | $S2V_{DD}$ | 8 |
| **System Control Signals[4]** | | | | |
| $\overline{\text{HRESET}}$ | B23 | I | $OV_{DD}$ | |
| $\overline{\text{HRESET\_REQ}}$ | J22 | O | $OV_{DD}$ | |
| $\overline{\text{SRESET}}$ | A26 | I | $OV_{DD}$ | |
| $\overline{\text{CKSTP\_IN}}$ | C27 | I | $OV_{DD}$ | |
| $\overline{\text{CKSTP\_OUT}}$ | F24 | O | $OV_{DD}$ | 21, 25 |
| **Power Management Signals[4]** | | | | |
| ASLEEP | B26 | O | $OV_{DD}$ | 20 |
| **Debug Signals[4]** | | | | |
| TRIG_IN | K20 | I | $OV_{DD}$ | |
| TRIG_OUT/READY/ $\overline{\text{QUIESCE}}$ | C28 | O | $OV_{DD}$ | 14 |
| MSRCID[0:4] | Y20, AB23, AB20, AB21, AC23 | O | $BV_{DD}$ | 14, 20 |
| MDVAL | AC20 | O | $BV_{DD}$ | 20 |
| CLK_OUT | G28 | O | $OV_{DD}$ | 18 |
| **Test Signals[4]** | | | | |
| $\overline{\text{LSSD\_MODE}}$ | G23 | I | $OV_{DD}$ | 26 |
| TEST_MODE[0:1] | K12, K10 | I | $OV_{DD}$ | 26 |
| **JTAG Signals[4]** | | | | |
| TCK | D26 | I | $OV_{DD}$ | |
| TDI | B25 | I | $OV_{DD}$ | 27 |
| TDO | D27 | O | $OV_{DD}$ | 18 |
| TMS | C25 | I | $OV_{DD}$ | 27 |
| $\overline{\text{TRST}}$ | A28 | I | $OV_{DD}$ | 27 |
| **Additional Analog Signals** | | | | |
| TEMP_ANODE | C11 | Thermal | — | |
| TEMP_CATHODE | C10 | Thermal | — | |
| **Special Connection Requirement Pins** | | | | |

**Table 1. Signal Reference by Functional Block (continued)**

| Name[1] | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| ASLEEP<br>cfg_core_speed | B26 | — | $OV_{DD}$ | 13 |
| MSRCID0<br>cfg_mem_debug | Y20 | — | $BV_{DD}$ | |
| MDVAL<br>cfg_boot_vector | AC20 | — | $BV_{DD}$ | |

**Notes:**

1. Multi-pin signals such as LDP[0:3] have their physical package pin numbers listed in order corresponding to the signal names.
2. Stub series terminated logic type pins.
3. All SSI signals are multiplexed with eLBC signals.
4. Low voltage transistor-transistor logic (LVTTL) type pins.
5. DIU_LD[23:16] = RED[7:0].
   DIU_LD[15:8] = GREEN[7:0].
   DIU_LD[7:0] = BLUE[7:0].
6. The pins for the SSI interface on the device are multiplexed with certain eLBC signals, which have the ability to operate at a different voltage than the other standard I/O signals. If the device is configured such that the eLBC uses a different voltage than standard I/O and an SSI port on the device is used, then level shifters are required on the SSI signals to ensure they correctly interface to other devices on the board at the proper voltage.
7. This pin should be pulled to ground with a 100-Ω resistor.
8. This pin should be pulled to ground with a 200-Ω resistor.
9. These pins should be left floating.
10. This is a SerDes PLL/DLL digital test signal and is only for factory use.
11. This is a SerDes PLL/DLL analog test signal and is only for factory use.
12. This pin should be pulled down if the platform frequency is 400 MHz or below.
13. This pin should be pulled down if the core frequency is 800 MHz or below.
14. MSRCID[1:2], DIU_LD[5:6] and TRIG_OUT/READY should NOT be pulled down (or driven low) during reset.15. The pins in this section are reset configuration pins. Each pin has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
16. These pins should be left floating.
17. Must be tied low if unused.
18. This output is actively driven during reset rather than being tri-stated during reset.
19. MDIC[0] should be connected to ground with an 18-Ω resistor ± 1 Ω and MDIC[1] should be connected to $GV_{DD}$ with an 18-Ω resistor ± 1 Ω. These pins are used for automatic calibration of the DDR IOs.
20. This pin is a reset configuration pin and appears again in the Reset Configuration Signals section of this table. See the Reset Configuration Signals section of this table for config name and connection details.
21. Recommend a weak pull-up resistor (1–10 kΩ) be placed from this pin to its power supply.
22. This multiplexed pin has input status in one mode and output in another.
23. This pin is a multiplexed signal for different functional blocks and appears more than once in this table.
24. For systems which boot from local bus (GPCM)-controlled flash, a pullup on LGPL4 is required.
25. This pin is open drain signal.
26. These are test signals for factory use only and must be pulled up (100 Ω to 1 kΩ) to $OV_{DD}$ for normal machine operation.
27. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
28. These pins are connected to the power/ground planes internally and may be used by the core power supply to improve tracking and regulation.

**Table 2. Absolute Maximum Ratings[1] (continued)**

| Characteristic | Symbol | Recommended Value | Unit | Notes |
|---|---|---|---|---|
| Storage temperature range | $T_{STG}$ | –55 to 150 | °C | |

**Notes:**

1 Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2 During run time (M, B, O)$V_{IN}$ and $MV_{REF}$ may overshoot/undershoot to a voltage and for a maximum duration as shown in Table 2.

## 2.1.2 Recommended Operating Conditions

Table 3 provides the recommended operating conditions for the MPC8610. Note that the values in Table 3 are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed. For details on order information and specific operating conditions for parts, see Section 4, "Ordering Information."

**Table 3. Recommended Operating Conditions**

| Characteristic | Symbol | Recommended Value | Unit | Notes |
|---|---|---|---|---|
| Core supply voltages | $V_{DD}$_Core | 1.025 ± 50 mV | V | 1 |
| | | 1.00 ± 50 mV | | 2 |
| Core PLL supply | $AV_{DD}$_Core | 1.025 ± 50 mV | V | 1, 3 |
| | | 1.00 ± 50 mV | | 2, 3 |
| SerDes receiver and core power supply (ports 1 and 2) | $S1V_{DD}$<br>$S2V_{DD}$ | 1.025 ± 50 mV | V | 1, 4 |
| | | 1.00 ± 50 mV | | 2 |
| SerDes transmitter power supply (ports 1 and 2) | $X1V_{DD}$<br>$X2V_{DD}$ | 1.025 ± 50 mV | V | 1 |
| | | 1.00 ± 50 mV | | 2 |
| SerDes digital logic power supply (ports 1 and 2) | $L1V_{DD}$<br>$L2V_{DD}$ | 1.025 ± 50 mV | V | 1 |
| | | 1.00 ± 50 mV | | 2 |
| Serdes PLL supply voltage (ports 1 and 2) | $SD1AV_{DD}$<br>$SD2AV_{DD}$ | 1.025 ± 50 mV | V | 1, 3 |
| | | 1.00 ± 50 mV | | 2, 3 |
| Platform supply voltage | $V_{DD}$_PLAT | 1.025 ± 50 mV | V | 1 |
| | | 1.00 ± 50 mV | | 2 |
| PCI and platform PLL supply voltage | $AV_{DD}$_PCI<br>$AV_{DD}$_PLAT | 1.025 ± 50 mV | V | 1, 3 |
| | | 1.00 ± 50 mV | | 2, 3 |
| DDR and DDR2 SDRAM I/O supply voltages | $GV_{DD}$ | 2.5 V ± 125 mV,<br>1.8 V ± 90 mV | V | 5 |
| Local bus and SSI I/O voltage | $BV_{DD}$ | 3.3 V ± 165 mV<br>2.5 V ± 125 mV<br>1.8 V ± 90 mV | V | |

**Table 27. DIU DC Electrical Characteristics (continued)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Low-level output voltage ($OV_{DD}$ = min, $I_{OL}$ = 100 µA) | $V_{OL}$ | — | 0.2 | V |

**Note:**
1. The symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 2 and Table 3.

## 2.8.2 DIU AC Timing Specifications

Figure 12 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and the data. All parameters shown in the diagram are programmable. This timing diagram corresponds to positive polarity of the DIU_CLK_OUT signal and active-high polarity of the DIU_HSYNC, DIU_VSYNC, and DIU_DE signals. By default, all control signals and the display data are generated at the rising edge of the internal pixel clock, and the DIU_CLK_OUT output to drive the panel has the same polarity with the internal pixel clock. User can select the polarity of the DIU_HSYNC and DIU_VSYNC signal (via the SYN_POL register), whether active-high or active-low, the default is active-high. The DIU_DE signal is always active-high.

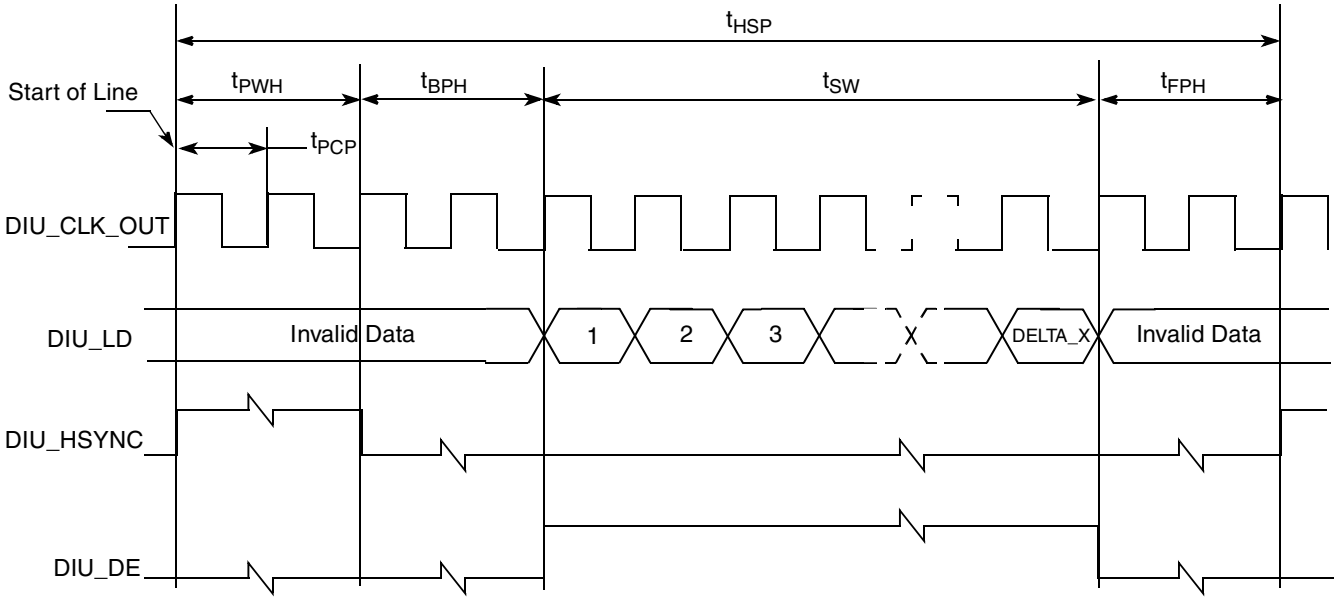



**Figure 12. TFT DIU/LCD Interface Timing Diagram—Horizontal Sync Pulse**

## 2.14 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8610.

### 2.14.1 GPIO DC Electrical Characteristics

Table 41 provides the DC electrical characteristics for the GPIO.

**Table 41. GPIO DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| Input current ($V_{IN}$[1] = 0 V or $V_{IN}$ = $V_{DD}$) | $I_{IN}$ | — | ±5 | μA |
| High-level output voltage ($OV_{DD}$ = min, $I_{OH}$ = –100 μA) | $V_{OH}$ | $OV_{DD}$ – 0.2 | — | V |
| Low-level output voltage ($OV_{DD}$ = min, $I_{OL}$ = 100 μA) | $V_{OL}$ | — | 0.2 | V |

**Note:**
1. The symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 2 and Table 3.

### 2.14.2 GPIO AC Timing Specifications

Table 42 provides the GPIO input and output AC timing specifications.

**Table 42. GPIO Input and Output AC Timing Specifications[1]**

| Characteristic | Symbol[2] | Min | Unit | Notes |
|---|---|---|---|---|
| GPIO inputs—minimum pulse width | $t_{GPIWID}$ | 7.5 | ns | 3 |
| GPIO outputs—minimum pulse width | $t_{GPOWID}$ | 12 | ns | |

**Notes:**
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least $t_{PIWID}$ ns to ensure proper operation.
3. The minimum pulse width is a function of the MPX/platform clock. The minimum pulse width must be greater than or equal to 4 times the MPX/platform clock period.

Figure 22 provides the AC test load for the GPIO.

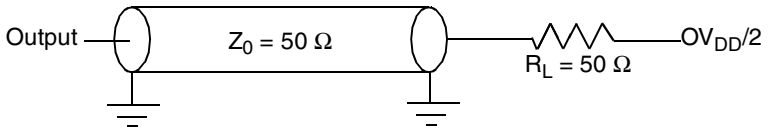



**Figure 22. GPIO AC Test Load**

### 2.17.2.3 Interfacing With Other Differential Signaling Levels

- With on-chip termination to SGND, the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC-coupled.
- Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

**NOTE**

Figure 34 to Figure 37 are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the MPC8610 SerDes reference clock receiver requirement provided in this document.

Figure 34 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with MPC8610 SerDes reference clock input's DC requirement.

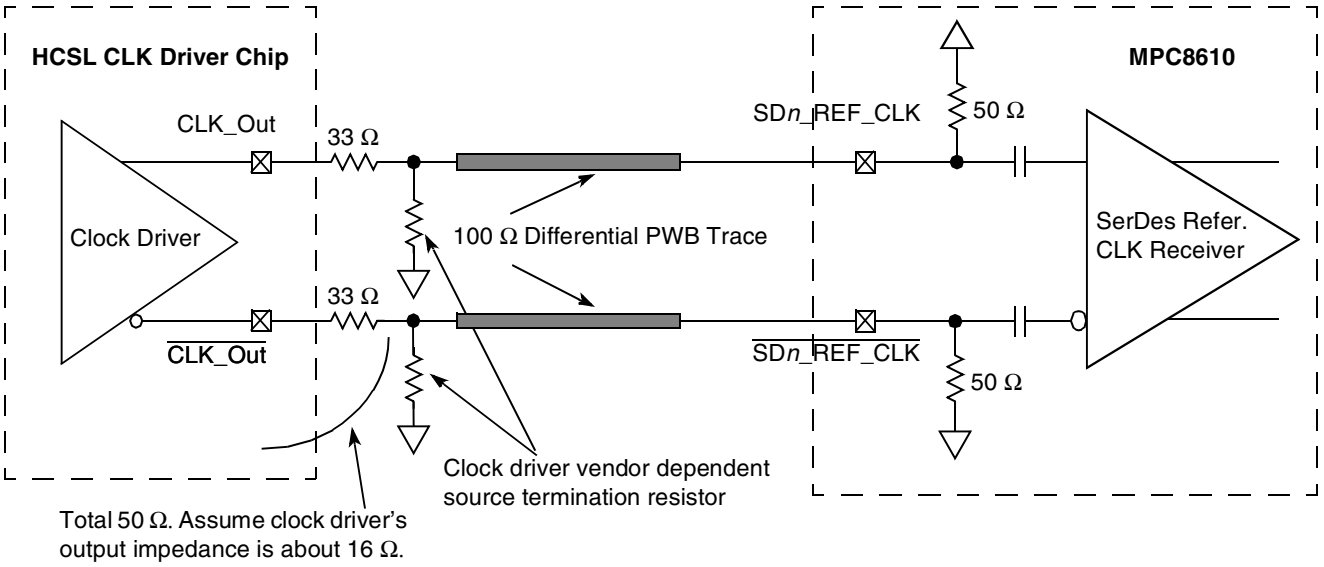



**Figure 34. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)**

Figure 35 shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the MPC8610 SerDes reference clock input's allowed range (100 to 400 mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

## 2.18.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the transport and data link layer, use the *PCI Express Base Specification*, Rev. 1.0a.

### 2.18.4.1 Differential Transmitter (TX) Output

Table 49 defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

**Table 49. Differential Transmitter (TX) Output Specifications**

| Symbol | Parameter | Min | Nom | Max | Units | Comments |
|---|---|---|---|---|---|---|
| UI | Unit interval | 399.88 | 400 | 400.12 | ps | Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1 |
| $V_{TX-DIFFp-p}$ | Differential peak-to-peak output voltage | 0.8 | | 1.2 | V | $V_{TX-DIFFp-p} = 2*\|V_{TX-D+} - V_{TX-D-}\|$ See Note 2 |
| $V_{TX-DE-RATIO}$ | De- emphasized differential output voltage (ratio) | -3.0 | -3.5 | -4.0 | dB | Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 2 |
| $T_{TX-EYE}$ | Minimum TX eye width | 0.70 | | | UI | The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3$ UI. See Notes 2 and 3 |
| $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ | Maximum time between the jitter median and maximum deviation from the median. | | | 0.15 | UI | Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3 |
| $T_{TX-RISE}$, $T_{TX-FALL}$ | D+/D– TX output rise/fall time | 0.125 | | | UI | See Notes 2 and 5 |
| $V_{TX-CM-ACp}$ | RMS AC peak common mode output voltage | | | 20 | mV | $V_{TX-CM-ACp} = RMS(\|V_{TXD+} - V_{TXD-}\|/2 - V_{TX-CM-DC})$<br>$V_{TX-CM-DC} = DC_{(avg)}$ of $\|V_{TX-D+} - V_{TX-D-}\|/2$<br>See Note 2 |
| $V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$ | Absolute delta of DC common mode voltage during LO and electrical idle | 0 | | 100 | mV | $\|V_{TX-CM-DC\ (during\ LO)} - V_{TX-CM-Idle-DC\ (During\ Electrical\ Idle)}\|$<=100 mV<br>$V_{TX-CM-DC} = DC_{(avg)}$ of $\|V_{TX-D+} - V_{TX-D-}\|/2$ [LO]<br>$V_{TX-CM-Idle-DC} = DC_{(avg)}$ of $\|V_{TX-D+} - V_{TX-D-}\|/2$ [Electrical Idle]<br>See Note 2 |
| $V_{TX-CM-DC-LINE-DELTA}$ | Absolute delta of DC common mode between D+ and D– | 0 | | 25 | mV | $\|V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-}\|$ <= 25 mV<br>$V_{TX-CM-DC-D+} = DC_{(avg)}$ of $\|V_{TX-D+}\|$<br>$V_{TX-CM-DC-D-} = DC_{(avg)}$ of $\|V_{TX-D-}\|$<br>See Note 2 |

**Table 49. Differential Transmitter (TX) Output Specifications (continued)**

| Symbol | Parameter | Min | Nom | Max | Units | Comments |
|---|---|---|---|---|---|---|
| $T_{crosslink}$ | Crosslink random timeout | 0 | | 1 | ms | This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one downstream and one upstream port. See Note 7 |

**Notes:**

1.) No test load is necessarily associated with this value.

2.) Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 43 and measured over any 250 consecutive TX UIs. (Also refer to the transmitter compliance eye diagram shown in Figure 41.)

3.) A $T_{TX-EYE}$ = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

4.) The transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes—see Figure 43). Note that the series capacitors $C_{TX}$ is optional for the return loss measurement.

5.) Measured between 20–80% at transmitter package pins into a test load as shown in Figure 43 for both $V_{TX-D+}$ and $V_{TX-D-}$.

6.) See Section 4.3.1.8 of the *PCI Express Base Specifications,* Rev. 1.0a.

7.) See Section 4.2.6.3 of the *PCI Express Base Specifications*, Rev. 1.0a.

### 2.18.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in Figure 41 is specified using the passive compliance/test measurement load (see Figure 43) in place of any real PCI Express interconnect + RX component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit will always be relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

**NOTE**

It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (i.e., least squares and median deviation fits).

**Table 50. Differential Receiver (RX) Input Specifications (continued)**

| Symbol | Parameter | Min | Nom | Max | Units | Comments |
|---|---|---|---|---|---|---|
| $L_{TX-SKEW}$ | Total skew | | | 20 | ns | Skew across all lanes on a link. This includes variation in the length of SKP ordered set (e.g., COM and one to five symbols) at the RX as well as any delay differences arising from the interconnect itself. |

**Notes:**

1.)No test load is necessarily associated with this value.

2.)Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 43 should be used as the RX device when taking measurements (also refer to the receiver compliance eye diagram shown in Figure 42). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.

3.)A $T_{RX-EYE}$ = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.

4.)The receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D– line biased to –300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D– line (that is, as measured by a Vector Network Analyzer with 50-Ω probes—see Figure 43). Note that the series capacitors CTX is optional for the return loss measurement.

5.)Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.

6.)The RX DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit will not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.

7.)It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

## 2.18.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 42 is specified using the passive compliance/test measurement load (see Figure 43) in place of any real PCI Express RX component.

Note: In general, the minimum receiver eye diagram measured with the compliance/test measurement load (see Figure 43) will be larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum receiver eye diagram (shown in Figure 42) expected at the input receiver based on some adequate combination of system simulations and the return loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

**Table 52. JTAG AC Timing Specifications (Independent of SYSCLK)[1] (continued)**

At recommended operating conditions (see Table 3).

| Parameter | Symbol[2] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| JTAG external clock to output high impedance:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDZ}$<br>$t_{JTKLOZ}$ | <br>3<br>3 | <br>19<br>9 | ns | 5, 6 |

**Notes:**

1. All outputs are measured from the midpoint voltage of the falling/rising edge of $t_{TCLK}$ to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 15). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{JTDVKH}$ symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{JTDXKH}$ symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to $t_{TCLK}$.
5. Non-JTAG signal output timing with respect to $t_{TCLK}$.
6. Guaranteed by design.

Figure 15 provides the AC test load for TDO and the boundary-scan outputs.

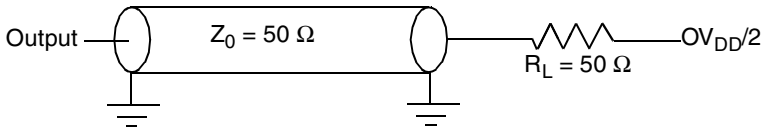



**Figure 44. AC Test Load for the JTAG Interface**

Figure 45 provides the JTAG clock input timing diagram.

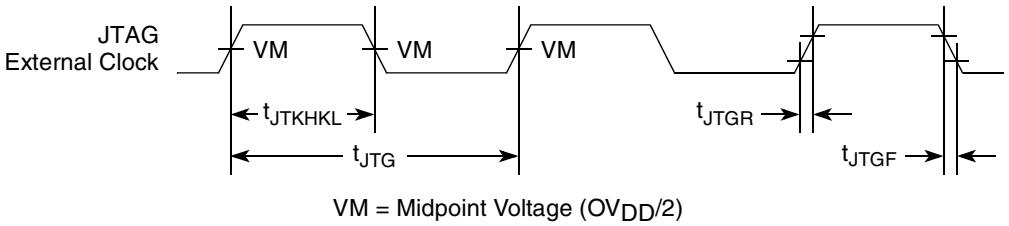



**Figure 45. JTAG Clock Input Timing Diagram**

Figure 46 provides the $\overline{\text{TRST}}$ timing diagram.

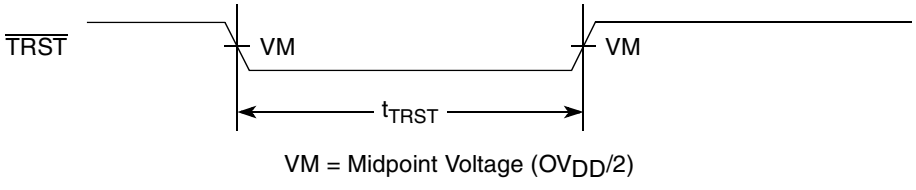



**Figure 46. $\overline{\text{TRST}}$ Timing Diagram**

### 3.1.3 e600 Core to MPX/Platform Clock PLL Ratio

The clock ratio between the e600 core and the platform clock is determined by the binary value of LBCTL, LALE, LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$, DIU_LD4 (cfg_core_pll[0:3]–reset config) signals at power up. Table 58 describes the supported ratios. Note that cfg_core_speed must be pulled low if the core frequency is 800 MHz or below.

**Table 58. e600 Core/Platform Clock Ratios**

| Binary Value of LBCTL, LALE, LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$, DIU_LD4 Signals | e600 core: MPX/Platform Ratio |
|---|---|
| 1000 | 2:1 |
| 1010 | 2.5:1 |
| 1100 | 3:1 |
| 1110 | 3.5:1 |
| 0000 | 4:1 |
| 0010 | 4.5:1 |
| All Others | Reserved |

### 3.1.4 Frequency Options

#### 3.1.4.1 SYSCLK and Platform Frequency Options

Table 59 shows the expected frequency options for SYSCLK and platform frequencies.

**Table 59. SYSCLK and Platform Frequency Options**

| Platform: SYSCLK Ratio | SYSCLK (MHz) | | | | | |
|---|---|---|---|---|---|---|
| | 33.33 | 66.66 | 83.33 | 100.00 | 111.11 | 133.33 |
| | Platform/MPX Frequency (MHz)[1] | | | | | |
| 3:1 | | | | | 333 | 400 |
| 4:1 | | | 333 | 400 | | 533 |
| 5:1 | | 333 | | 500 | | |
| 6:1 | | 400 | 500 | | | |
| 8:1 | | 533 | | | | |
| 10:1 | 333 | | | | | |
| 12:1 | 400 | | | | | |
| 16:1 | 533 | | | | | |

1 Platform/MPX Frequency values are shown rounded down to the nearest whole number (decimal place accuracy removed)

## 3.2 Power Supply Design and Sequencing

### 3.2.1 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins ($AV_{DD}$_Plat, $AV_{DD}$_Core, $AV_{DD}$_PCI, and SD*n*$AV_{DD}$, respectively). The $AV_{DD}$ level should always be equivalent to $V_{DD}$, and preferably these voltages will be derived directly from $V_{DD}$ through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply, one to each of the $AV_{DD}$ type pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific $AV_{DD}$ type pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the $AV_{DD}$ type pin, which is on the periphery of 783 FC-PBGA the footprint, without the inductance of vias.

Figure 48 shows the filter circuit for the platform PLL power supplies ($AV_{DD}$_PLAT).

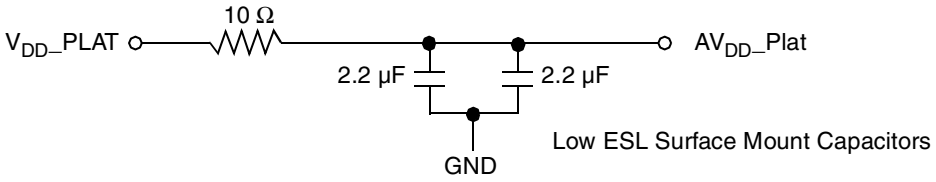



**Figure 48. MPC8610 PLL Power Supply Filter Circuit (for Platform)**

Figure 49 shows the filter circuit for the core PLL power supply ($AV_{DD}$_Core).

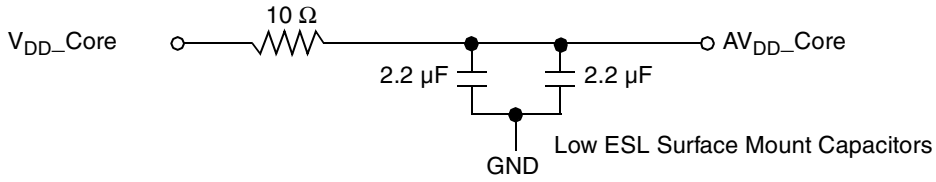
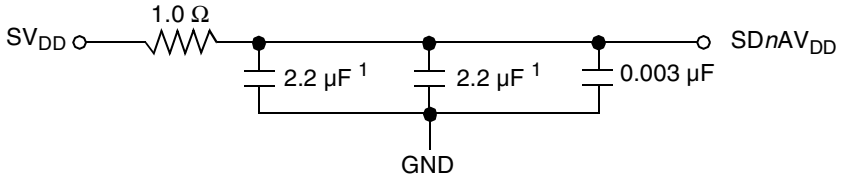



**Figure 49. MPC8610 PLL Power Supply Filter Circuit (for Core)**

The SD*n*$AV_{DD}$ signals provide power for the analog portions of the SerDes PLLs. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in Figure 50. For maximum effectiveness, the filter circuit is placed as closely as possible to the SD*n*$AV_{DD}$ balls to ensure it filters out as much noise as possible. The ground connection should be near the SD*n*$AV_{DD}$ balls. The 0.003-µF capacitor is closest to the balls, followed by the two 2.2-µF capacitors, and finally the 1 ohm resistor to the board supply plane. The capacitors are connected from SD*n*$AV_{DD}$ to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.




1. An 0805 sized capacitor is recommended for system initial bring-up.

**Figure 50. SerDes PLL Power Supply Filter**

Note the following:

- SD*n*AV$_{DD}$ should be a filtered version of SV$_{DD}$.
- Signals on the SerDes interface are fed from the SV$_{DD}$ power plane.

## 3.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8610 system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V$_{DD}$, BV$_{DD}$, OV$_{DD}$, GV$_{DD}$, V$_{DD}$_Core, and V$_{DD}$_PLAT pin of the device. These decoupling capacitors should receive their power from separate V$_{DD,}$ BV$_{DD}$, OV$_{DD}$, GV$_{DD}$, V$_{DD}$_Core, V$_{DD}$_PLAT, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V$_{DD}$, BV$_{DD}$, OV$_{DD}$, GV$_{DD}$, V$_{DD}$_Core, and V$_{DD}$_PLAT planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

## 3.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (S*n*V$_{DD}$ and X*n*V$_{DD}$) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

- First, the board should have at least 10 x 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there should be a 1-µF ceramic chip capacitor on each side of the device. This should be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there should be a 10-µF, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

## 3.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs should be tied to V$_{DD}$, BV$_{DD}$, OV$_{DD}$, GV$_{DD}$, V$_{DD}$_Core, V$_{DD}$_PLAT, X*n*V$_{DD}$, and S*n*V$_{DD}$ as required. All unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external V$_{DD}$, BV$_{DD}$, OV$_{DD}$, GV$_{DD}$, V$_{DD}$_Core, V$_{DD}$_PLAT, X*n*V$_{DD}$, S*n*V$_{DD}$, and GND pins of the device.

Special cases:

- Local Bus—If parity is not used, tie LDP[0:3] to ground via a 4.7-kΩ resistor, tie LPBSE to OV$_{DD}$ via a 4.7-kΩ resistor (pull-up resistor). For systems which boot from local bus (GPCM)-controlled Flash, a pull up on LGPL4 is required.

$R_P$ is trimmed until the voltage at the pad equals $OV_{DD}/2$. $R_P$ then becomes the resistance of the pull-up devices. $R_P$ and $R_N$ are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

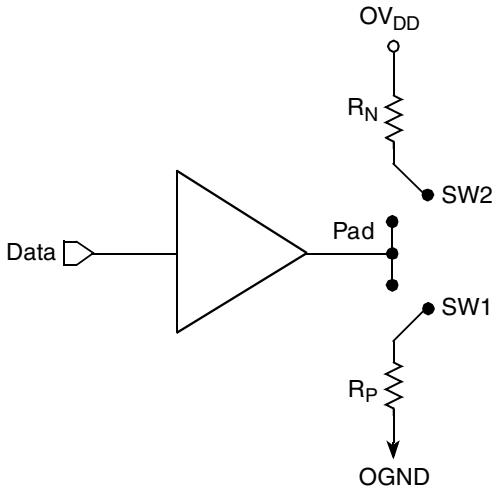



**Figure 51. Driver Impedance Measurement**

Table 60 summarizes the signal impedance targets. The driver impedances are targeted at minimum $V_{DD}$, nominal $OV_{DD}$, 105°C.

**Table 60. Impedance Characteristics**

| Impedance | Local Bus, DUART, Control, Configuration, Power Management | PCI Express | DDR DRAM | Symbol | Unit |
|---|---|---|---|---|---|
| $R_N$ | 43 Target | 25 Target | 20 Target | $Z_0$ | W |
| $R_P$ | 43 Target | 25 Target | 20 Target | $Z_0$ | W |

**Note:** Nominal supply voltages. See Table 3, $T_j$ = 105°C.

## 3.8 Configuration Pin Muxing

The MPC8610 provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform /system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e600 core PLL ratio configuration pins are not equipped with these default pull-up devices.

# 3.10 Guidelines for High-Speed Interface Termination

## 3.10.1 SerDes Interface

The high-speed SerDes interface can be disabled through the POR input cfg_io_ports[0:2] and through the DEVDISR register in software. If a SerDes port is disabled through the POR input the user can not enable it through the DEVDISR register in software. However, if a SerDes port is enabled through the POR input the user can disable it through the DEVDISR register in software. Disabling a SerDes port through software should be done on a temporary basis. Power is always required for the SerDes interface, even if the port is disabled through either mechanism. Table 61 describes the possible enabled/disabled scenarios for a SerDes port. The termination recommendations must be followed for each port.

**Table 61. SerDes Port Enabled/Disabled Configurations**

| | Disabled through POR input | Enabled through POR input |
|---|---|---|
| Enabled through DEVDISR | SerDes port is disabled (and cannot be enabled through DEVDISR)<br><br>Complete termination required (Reference clock not required | SerDes port is enabled<br><br>Partial termination may be required[1] (Reference clock is required) |
| Disabled through DEVDISR | SerDes port is disabled (through POR input)<br><br>Complete termination required (Reference clock not required) | SerDes port is disabled after software disables port<br><br>Same termination requirements as when the port is enabled through POR input[2] (Reference clock is required) |

1 Partial termination when a SerDes port is enabled through both POR input and DEVDISR is determined by the SerDes port mode. If port 1 is in x4 PCI Express mode, no termination is required because all pins are being used. If port 1 is in x1/x2 PCI Express mode, termination is required on the unused pins. If port 2 is in x8 PCI Express mode, no termination is required because all pins are being used. If port 1 is in x1/x2/x4 PCI Express mode, termination is required on the unused pins.

2 If a SerDes port is enabled through the POR input and then disabled through DEVDISR, no hardware changes are required. Termination of the SerDes port should follow what is required when the port is enabled through both POR input and DEVDISR. See Note 1 for more information.

If the high-speed SerDes port requires complete or partial termination, the unused pins should be terminated as described in this section.

The following pins must be left unconnected (floating):

- SD*n*_TX[7:0]
- $\overline{\text{SD}n\text{\_TX}}$[7:0]

The following pins must be connected to GND:

- SD*n*_RX[7:0]
- $\overline{\text{SD}n\text{\_RX}}$[7:0]
- SD*n*_REF_CLK
- $\overline{\text{SD}n\text{\_REF\_CLK}}$

For other directions on reserved or no-connects pins, see Section 1, “Pin Assignments and Reset States.”

## 3.11 Guidelines for PCI Interface Termination

PCI termination if PCI is not used at all.

Option 1

- If PCI arbiter is enabled during POR,
  - All AD pins will be driven to the stable states after POR. Therefore, all ADs pins can be floating. This includes PCI_AD[31:0], PCI_C/$\overline{BE}$[3:0], and PCI_PAR signals.
  - All PCI control pins can be grouped together and tied to $OV_{DD}$ through a single 10-kΩ resistor.
  - It is optional to disable PCI block through DEVDISR register after POR reset.

Option 2

- If PCI arbiter is disabled during POR,
  - All AD pins will be in the input state. Therefore, all ADs pins need to be grouped together and tied to $OV_{DD}$ through a single (or multiple) 10-kΩ resistor(s)
  - All PCI control pins can be grouped together and tied to $OV_{DD}$ through a single 10-kΩ resistor
  - It is optional to disable PCI block through DEVDISR register after POR reset.

## 3.12 Thermal

This section describes the thermal specifications of the MPC8610.

### 3.12.1 Thermal Characteristics

Table 62 provides the package thermal characteristics for the MPC8610.

**Table 62. Package Thermal Characteristics[1]**

| Characteristic | Symbol | Value | Unit | Notes |
|---|---|---|---|---|
| Junction-to-ambient thermal resistance, natural convection, single-layer (1s) board | $R_{\theta JA}$ | 24 | °C/W | 1 |
| Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board | $R_{\theta JA}$ | 18 | °C/W | 1 |
| Junction-to-ambient thermal resistance, 200 ft/min airflow, single-layer (1s) board | $R_{\theta JMA}$ | 18 | °C/W | 1 |
| Junction-to-ambient thermal resistance, 200 ft/min airflow, four-layer (2s2p) board | $R_{\theta JMA}$ | 15 | °C/W | 1 |
| Junction-to-board thermal resistance | $R_{\theta JB}$ | 10 | °C/W | 2 |
| Junction-to-case thermal resistance | $R_{\theta JC}$ | <0.1 | °C/W | 3 |

**Notes**:
1. Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
2. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-case resistance is less than 0.1°C/W because the silicon die is the top of the packaging case..

### 3.12.2 Thermal Management Information

This section provides thermal management information for the flip-chip, plastic ball-grid array (FC_PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The MPC8610 implements several features designed to assist with thermal management, including the temperature diode. The temperature diode allows an external device to monitor the die temperature in order to detect excessive temperature conditions and alert the system; see Section 3.12.2.5, “Temperature Diode,” for more information.

| | |
|---|---|
| Tyco Electronics<br>Chip Coolers™<br>P.O. Box 3668<br>Harrisburg, PA 17105-3668<br>Internet: www.chipcoolers.com | 800-522-6752 |
| Wakefield Engineering<br>33 Bridge St.<br>Pelham, NH 03076<br>Internet: www.wakefield.com | 603-635-5102 |

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

### 3.12.2.1 Internal Package Conduction Resistance

For the exposed-die packaging technology described in Table 62, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

Figure 55 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

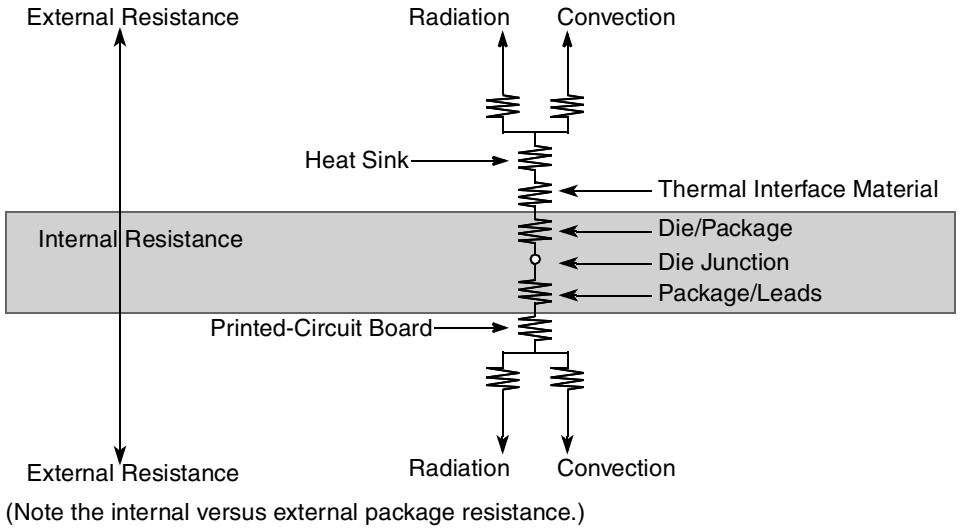



**Figure 55. C4 Package with Heat Sink Mounted to a Printed-Circuit Board**

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon, then through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

### 3.12.2.2 Thermal Interface Materials

A thermal interface material is recommended at the package-to-heat sink interface to minimize the thermal contact resistance. Figure 56 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, fluoroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. In contrast, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.