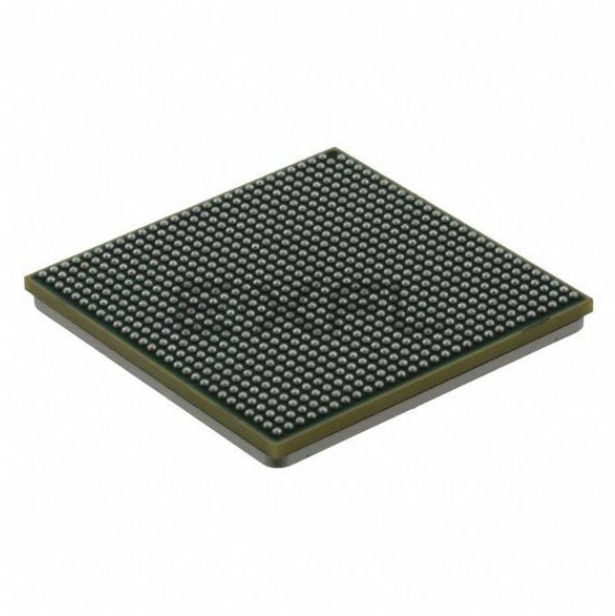

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e600
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	DIU, LCD
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8610px1333jb

Figure 1 shows the major functional units within the MPC8610.

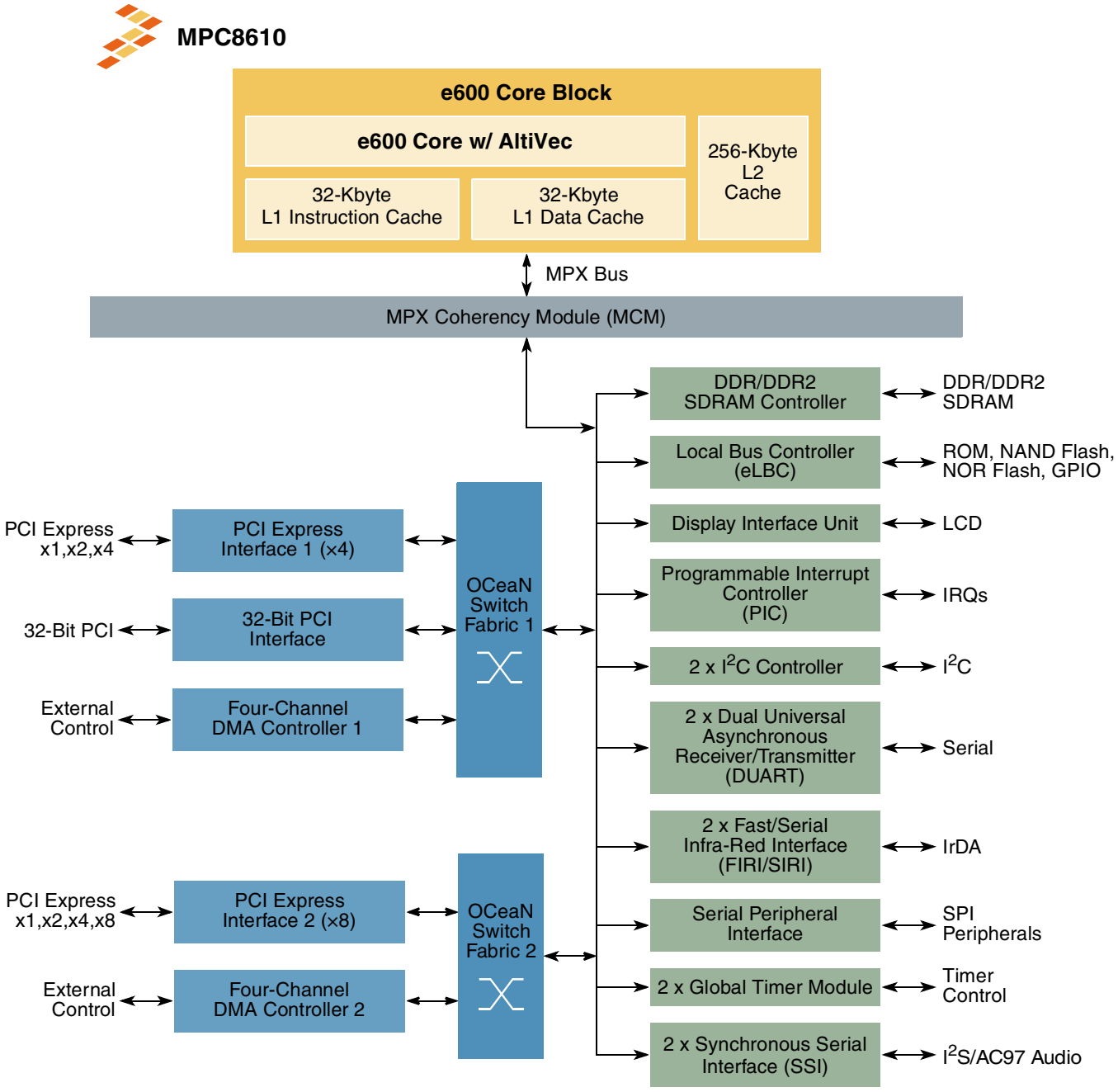


Figure 1. MPC8610 Block Diagram

Table 1. Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
LAD[0:31]	AA21, AA22, AA23, Y21, Y22, Y23, Y24, W23, W24, W25, V28, V27, V25, V23, V21, W22, U28, U26, U24, U22, U23, U20, U21, W20, V20, T24, T25, T27, T26, T21, T22, T23	I/O	BV_{DD}	20
LDP[0:3]/LA[6:9]	N28, M28, L28, P25	I/O	BV_{DD}	
LA10/SSI1_TXD	P19	O	BV_{DD}	20, 23
LA11/SSI1_TFS	M27	O	BV_{DD}	23
LA12/SSI1_TCK	U18	O	BV_{DD}	23
LA13/SSI1_RCK	P28	O	BV_{DD}	23
LA14/SSI1_RFS	R18	O	BV_{DD}	23
LA15/SSI1_RXD	R19	O	BV_{DD}	23
LA16/SSI2_TXD	R20	O	BV_{DD}	23
LA17/SSI2_TFS	M18	O	BV_{DD}	23
LA18/SSI2_TCK	N18	O	BV_{DD}	23
LA19/SSI2_RCK	N27	O	BV_{DD}	23
LA20/SSI2_RFS	P20	O	BV_{DD}	23
LA21/SSI2_RXD	P21	O	BV_{DD}	23
LA[22:31]	M19, M21, M22, M23, N23, N24, M26, N20, N21, N22	O	BV_{DD}	20
$\overline{\text{LCS}}$[0:4]	R24, R22, P23, P24, P27	O	BV_{DD}	21
$\overline{\text{LCS5}}$/$\overline{\text{DMA2\_DREQ0}}$	R23	O	BV_{DD}	21, 22, 23
$\overline{\text{LCS6}}$/$\overline{\text{DMA2\_DACK0}}$	N26	O	BV_{DD}	21, 23
$\overline{\text{LCS7}}$/$\overline{\text{DMA2\_DDONE0}}$	R26	O	BV_{DD}	21, 23
$\overline{\text{LWE0}}$/$\overline{\text{LFWE}}$/$\overline{\text{LBS0}}$	T19	O	BV_{DD}	20
$\overline{\text{LWE1}}$/$\overline{\text{LBS1}}$	T20	O	BV_{DD}	20
$\overline{\text{LWE2}}$/$\overline{\text{LBS2}}$	W19	O	BV_{DD}	20
$\overline{\text{LWE3}}$/$\overline{\text{LBS3}}$	T18	O	BV_{DD}	20
LBCTL	T28	O	BV_{DD}	20
LALE	R28	O	BV_{DD}	20
LGPL0/LFCLE	L19	O	BV_{DD}	20
LGPL1/LFALE	L20	O	BV_{DD}	20
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$	L21	O	BV_{DD}	20
LGPL3/$\overline{\text{LFWP}}$	L22	O	BV_{DD}	20
$\overline{\text{LGTA}}$/LFR$\overline{\text{B}}$/LGPL4/ LUPWAIT/LPBSE	L23	I/O	BV_{DD}	24

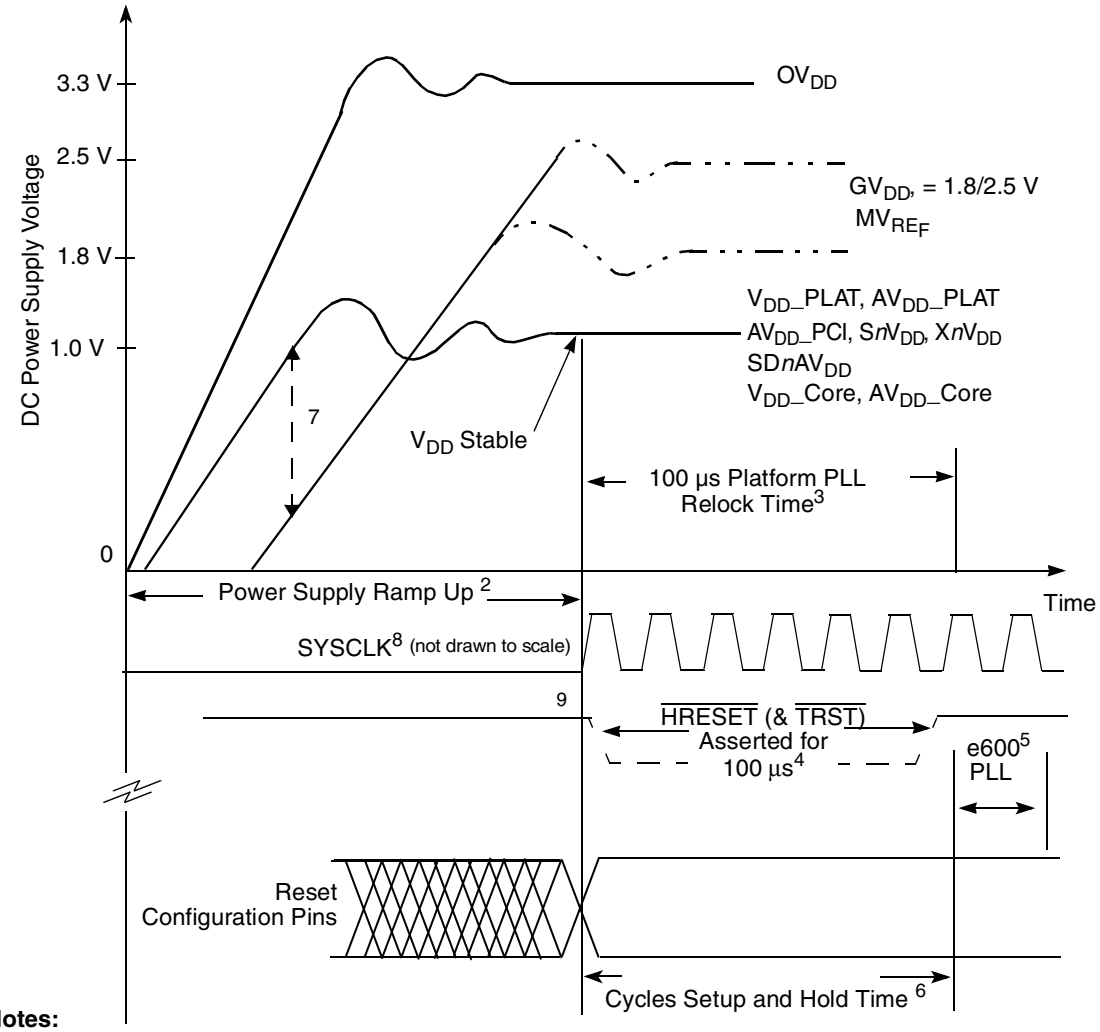
Table 3. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Notes
LCD, PCI, general timer, MPIC, IrDA, DUART, DMA, interrupts, system control and clocking, debug, test, JTAG, power management, I^2C, SPI, and miscellaneous I/O voltage		OV_{DD}	3.3 V ± 165 mV	V	6
Input voltage	DDR and DDR2 SDRAM signals	MV_{IN}	(GND – 0.3) to (GV_{DD} + 0.3)	V	7, 5
	DDR and DDR2 SDRAM reference	MV_{REF}	(GND – 0.3) to (GV_{DD}/2 + 0.3)	V	7
	Local Bus I/O voltage	BV_{IN}	(GND – 0.3) to (BV_{DD} + 0.3)		7
	LCD, PCI, general purpose timer, MPIC, IrDA, DUART, DMA, interrupts, system control and clocking, debug, test, JTAG, power management, I^2C, SPI, and miscellaneous I/O voltage	OV_{IN}	(GND – 0.3) to (OV_{DD} + 0.3)	V	7, 6
Junction temperature range		T_J	0 to 105	°C	
			–40 to 105		8

Notes:

1. Applies to devices marked with a core frequency of 1333 MHz. Refer to Table Part Numbering Nomenclature to determine if the device has been marked for a core frequency of 1333 MHz.
2. Applies to devices marked with a core frequency below 1333 MHz. Refer to Table Part Numbering Nomenclature to determine if the device has been marked for a core frequency below 1333 MHz.
3. AVDD measurements are made at the input of the R/C filter described in Section 3.2.1, “PLL Power Supply Filtering,” and not at the processor pin.
4. PCI Express interface of the device is expected to receive signals from 0.175 to 1.2 V. Refer to Section 2.18.4.3, “Differential Receiver (RX) Input Specifications,” for more information.
5. **Caution:** MV_{IN} must meet the overshoot/undershoot requirements for GV_{DD} as shown in Figure 2.
6. **Caution:** OV_{IN} must meet the overshoot/undershoot requirements for OV_{DD} as shown in Figure 2.
7. Timing limitations for (M, B, O) V_{IN} and MV_{REF} during regular run time is provided in Figure 2.
8. Applies to devices marked MC8610TxxyyyyMz for extended temperature range. Note that MC8610Txx1333Jz is not offered.

Figure 3 illustrates the power up sequence as described above.



Notes:

1. Dotted waveforms correspond to optional supply values for a specified power supply. See Table 3.
2. Ther recommended maximum ramp up time for power supplies is 20 milliseconds.
3. Refer to Section 2.5, "RESET Initialization" for additional information on PLL relock and reset signal assertion timing requirements.
4. Refer to Table 9 for additional information on reset configuration pin setup timing requirements. In addition see Figure 53 regarding $\overline{\text{HRESET}}$ and JTAG connection details including $\overline{\text{TRST}}$.
5. e600 PLL relock time is 100 microseconds maximum plus 255 MPX_clk cycles.
6. Stable PLL configuration signals are required as stable SYSCLK is applied. All other POR configuration inputs are required 4 SYSCLK cycles before $\overline{\text{HRESET}}$ negation and are valid at least 2 SYSCLK cycles after $\overline{\text{HRESET}}$ has negated (hold requirement). See Section 2.5, "RESET Initialization," for more information on setup and hold time of reset configuration signals.
7. The rail for V_{DD}_PLAT, AV_{DD}_PLAT, V_{DD}_Core, AV_{DD}_Core, AV_{DD}_PCI, SnV_{DD}, XnV_{DD}, and $SDnAV_{DD}$ must reach 90% of its value before the rail for GV_{DD} and MV_{REF} reaches 10% of its value.
8. SYSCLK must be driven only AFTER the power for the various power supplies is stable.
9. The reset configuration signals for DRAM types must be valid before $\overline{\text{HRESET}}$ is asserted.

Figure 3. MPC8610 Power Up Sequencing

Table 6. MPC8610 Individual Supply Maximum Power Dissipation[1] (continued)

Component Description	Supply Voltage (V)	Est. Power (Watts)	Notes
Platform PLL voltage supply	AV_{DD}_PLAT = 1.025 V @ 1333 MHz	0.0125	
	AV_{DD}_PLAT = 1.00 V @ 1066 MHz	0.0125	

Notes:

1. This is a maximum power supply number which is provided for power supply and board design information. The numbers are based on 100% utilization for each component. The components listed are not expected to have 100% usage simultaneously for all components. Actual numbers may vary based on activity. Note that the production parts should have a total maximum power value based on Table 5. The 'Est.' in the Est. Power column is to emphasize that these numbers are based on theoretical estimates. The device is tested to ensure that the sum of all four supplies does not exceed the power stated in Table 5. No specific supply should ever exceed its individual amount estimated in Table 6.

2.3.1 Frequency Derating

To reduce power consumption, these devices support frequency derating if the reduced maximum processor core frequency and reduced maximum platform frequency requirements are observed. The reduced maximum processor core frequency, resulting maximum platform frequency and power consumption are provided in Table 7. Only those parameters in Table 7 are affected; all other parameter specifications are unaffected.

Table 7. Core Frequency, Platform Frequency and Power Consumption Derating

Maximum Rated Core Frequency (Device Marking)	Maximum Derated Core/Platform Frequency (MHz)	V_{DD}_Core, V_{DD}_PLAT (V)	Typical Power (Watts)	Thermal Power (Watts)	Maximum Power (Watts)
1333J	N/A				
1066J	1000/400	1.00	8.0	9.4	12.5
800G	667/333	1.00	5.0	6.4	8.5

2.4 Input Clocks

Table 8 provides the system clock (SYSCLK) DC specifications for the MPC8610.

Table 8. SYSCLK DC Electrical Characteristics (OV_{DD} = 3.3 V ± 165 mV)

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN}[1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA

[1] Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2 and Table 3.

2.4.1 System Clock Timing

Table 9 provides the system clock (SYSCLK) AC timing specifications for the MPC8610.

Table 9. SYSCLK AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	33	—	133	MHz	1
SYSCLK cycle time	t_{SYSCLK}	7.5	—	—	ns	—
SYSCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	3
SYSCLK jitter	—	—	—	±150	ps	4, 5

Notes:
All specifications at recommended operating conditions (see Table 3) with OV_{DD} = 3.3 V ± 165 mV.
1. **Caution:** The platform to SYSCLK clock ratio and e600 core to platform clock ratio settings must be chosen such that the resulting SYSCLK, platform, and e600 (core) frequencies do not exceed their respective maximum or minimum operating frequencies. Refer to Section 3.1.2, “Platform/MPX to SYSCLK PLL Ratio” and Section 3.1.3, “e600 Core to MPX/Platform Clock PLL Ratio,” for ratio settings.
2. Rise and fall times for SYSCLK are measured at 0.4 and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the short term jitter only and is guaranteed by design.
5. The SYSCLK driver’s closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter. Note that the frequency modulation for SYSCLK reduces significantly for the spread spectrum source case. This is to guarantee what is supported based on design.

2.4.1.1 SYSCLK and Spread Spectrum Sources

Spread spectrum clock sources are a popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise over a wider spectrum and reducing the peak noise magnitude. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 9 considers short-term (cycle-to-cycle) jitter only and the clock generator’s cycle-to-cycle output jitter should meet the MPC8610 input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the MPC8610 is compatible with spread spectrum sources if the recommendations listed in Table 10 are observed.

Table 10. Spread Spectrum Clock Source Recommendations

Parameter	Min	Max	Unit	Notes
Frequency modulation	—	50	kHz	1
Frequency spread	—	1.0	%	1, 2

Notes:
All specifications at recommended operating conditions (see Table 3).
1. Guaranteed by design.
2. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 10.

It is imperative to note that the processor’s minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated e600 core frequency should avoid violating the stated limits by using down-spreading only.

Table 16. DDR SDRAM DC Electrical Characteristics for GV_{DD} (typ) = 2.5 V (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–16.2	—	mA	
Output low current (V_{OUT} = 0.35 V)	I_{OL}	16.2	—	mA	

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

Table 17 provides the DDR capacitance when GV_{DD} (typ)=2.5 V.

Table 17. DDR SDRAM Capacitance for GV_{DD} (typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

Table 18 provides the current draw characteristics for MV_{REF}.

Table 18. Current Draw Characteristics for MV_{REF}

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Current draw for MV_{REF}	I_{MVREF}	—	500	μA	1

Note:
1. The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.

2.6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR/DDR2 SDRAM interface.

2.6.2.1 DDR SDRAM Input AC Timing Specifications

Table 19 provides the input AC timing specifications for the DDR2 SDRAM when GV_{DD}(typ)=1.8 V.

Table 19. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.25	V
AC input high voltage	V_{IH}	MV_{REF} + 0.25	—	V

Table 30. I^2C DC Electrical Characteristics (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max)	I_I	–10	10	µA	3
Capacitance for each I/O pin	C_I	—	10	pF	

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. Refer to the *MPC8610 Integrated Host Processor Reference Manual*, for information on the digital filter used.
3. I/O pins will obstruct the SDA and SCL lines if OV_{DD} is switched off.

2.9.2 I^2C AC Electrical Specifications

Table 31 provides the AC timing parameters for the I^2C interfaces.

Table 31. I^2C AC Electrical Specifications

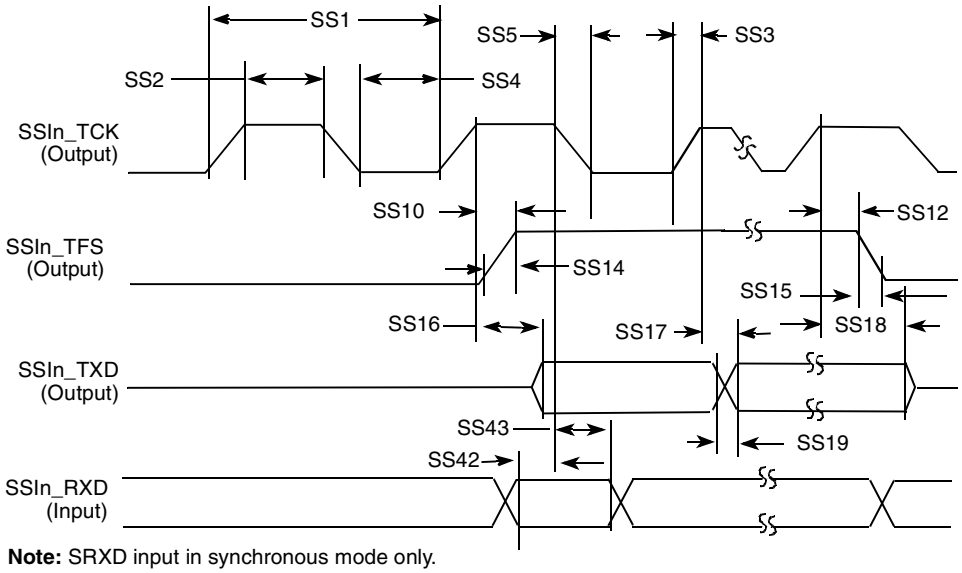
All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 30).

Parameter	Symbol[1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}[4]	1.3	—	µs
High period of the SCL clock	t_{I2CH}[4]	0.6	—	µs
Setup time for a repeated START condition	t_{I2SVKH}[4]	0.6	—	µs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}[4]	0.6	—	µs
Data setup time	t_{I2DVKH}[4]	100	—	ns
Data input hold time: CBUS compatible masters I^2C bus devices	t_{I2DXKL}	 — 0[2]	 — —	µs
Data ouput delay time	t_{I2OVKL}	—	0.9 [3]	µs
Setup time for STOP condition	t_{I2PVKH}	0.6	—	µs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V

Table 35. SSI Transmitter with Internal Clock Timing Parameters (continued)

Parameter	Symbol	Min	Max	Unit
SRXD hold after (Tx) CK falling	SS43	0	—	ns
Loading	SS52	—	25	pF

Figure 17 provides the SSI transmitter timing with internal clock.



Note: SRXD input in synchronous mode only.

Figure 17. SSI Transmitter with Internal Clock Timing Diagram

2.15 Serial Peripheral Interface (SPI)

This section describes the DC and AC electrical specifications for the SPI interface of the MPC8610.

2.15.1 SPI DC Electrical Characteristics

Table 43 provides the SPI DC electrical characteristics.

Table 43. SPI DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	– 0.3	0.8	V
Input current (V_{IN}[1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = mn, I_{OH} = –100 μA)	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 μA)	V_{OL}	—	0.2	V

Note:
1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2 and Table 3.

2.15.2 SPI AC Timing Specifications

Table 44 provides the SPI input and output AC timing specifications.

Table 44. SPI AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
SPI outputs valid—master mode (internal clock) delay	t_{NIKHOV}		1	ns
SPI outputs hold—master mode (internal clock) delay	t_{NIKHOX}	-0.2		ns
SPI outputs valid—slave mode (external clock) delay	t_{NEKHOV}		8	ns
SPI outputs hold—slave mode (external clock) delay	t_{NEKHOX}	2		ns
SPI inputs—master mode (internal clock input setup time	t_{NIIVKH}	4		ns
SPI inputs—master mode (internal clock input hold time	t_{NIIXKH}	0		ns
SPI inputs—slave mode (external clock) input setup time	t_{NEIVKH}	4		ns
SPI inputs—slave mode (external clock) input hold time	t_{NEIXKH}	2		ns

Notes:
1. Output specifications are measured from the 50 percent level of the rising edge of CLKIN to the 50 percent level of the signal. Timings are measured at the pin.
2. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).

Figure 28 shows the PCI output AC timing conditions.

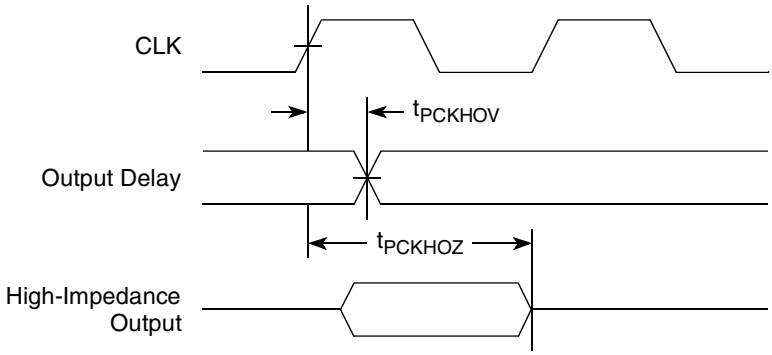


Figure 28. PCI Output AC Timing Measurement Condition

2.17 High-Speed Serial Interfaces (HSSI)

The MPC8610 features two Serializer/Deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. The SerDes1 interface is dedicated for PCI Express (x1/x2/x4) data transfers. The SerDes2 interface is dedicated for PCI Express (x1/x2/x4/x8) data transfers.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

2.17.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 29 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SD*n*_TX and $\overline{\text{SD}n\text{\_TX}}$) or a receiver input (SD*n*_RX and $\overline{\text{SD}n\text{\_RX}}$). Each signal swings between A volts and B volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. Single-ended swing

   The transmitter output signals and the receiver input signals SD*n*_TX, $\overline{\text{SD}n\text{\_TX}}$, SD*n*_RX, and $\overline{\text{SD}n\text{\_RX}}$ each have a peak-to-peak swing of A – B volts. This is also referred as each signal wire's single-ended swing.

2. Differential output voltage, V_{OD} (or differential output swing):

   The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SDn\_TX} - V_{\overline{SDn\_TX}}$. The V_{OD} value can be either positive or negative.

3. Differential input voltage, V_{ID} (or differential input swing):

   The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SDn\_RX} - V_{\overline{SDn\_RX}}$. The V_{ID} value can be either positive or negative.

4. Differential peak voltage, V_{DIFFp}

   The peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak voltage, $V_{DIFFp} = |A - B|$ volts.

5. Differential peak-to-peak, $V_{DIFFp-p}$

   Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to -(A – B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 * V_{DIFFp} = 2 * |(A - B)|$ volts, which is twice

2.17.2.3 Interfacing With Other Differential Signaling Levels

- With on-chip termination to SGND, the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC-coupled.
- Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

NOTE

Figure 34 to Figure 37 are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the MPC8610 SerDes reference clock receiver requirement provided in this document.

Figure 34 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with MPC8610 SerDes reference clock input's DC requirement.

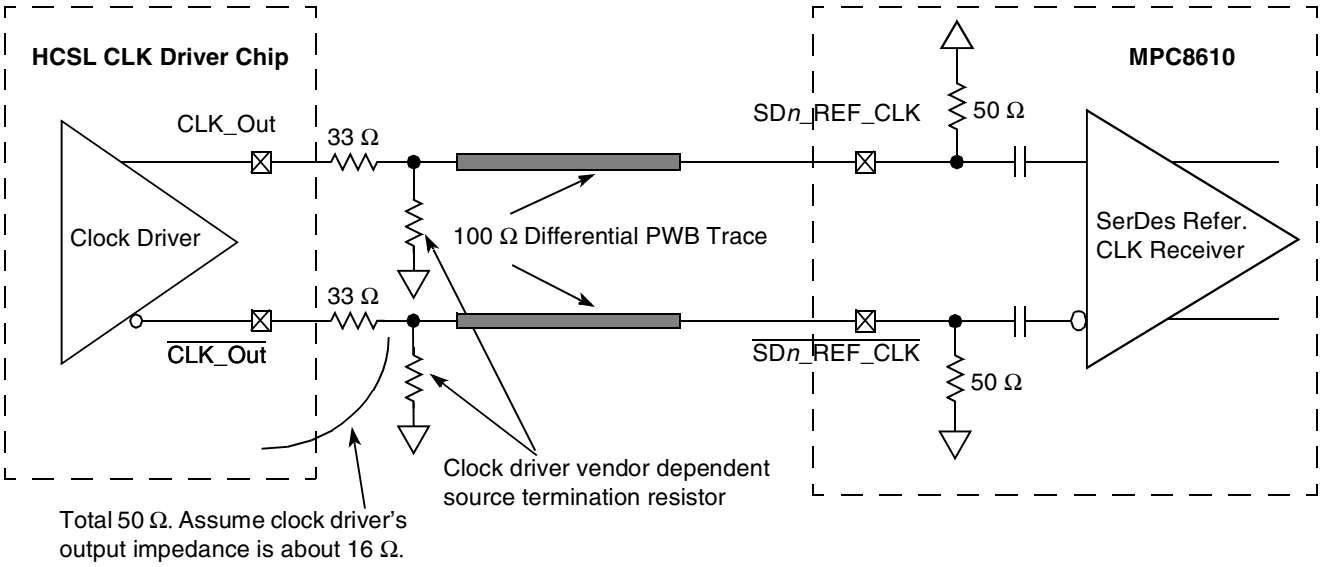


Figure 34. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

Figure 35 shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the MPC8610 SerDes reference clock input's allowed range (100 to 400 mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

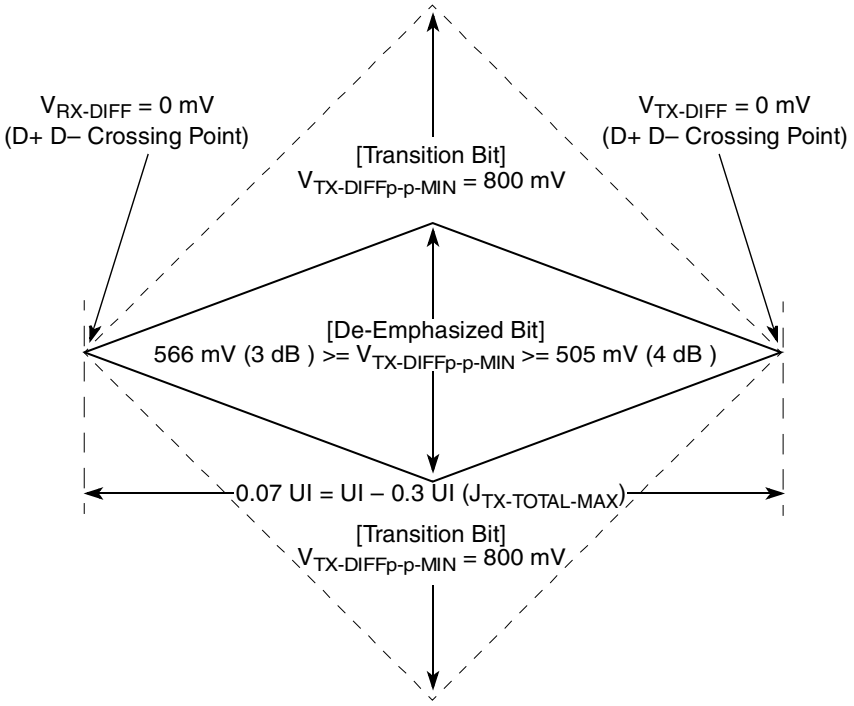


Figure 41. Minimum Transmitter Timing and Voltage Output Compliance Specifications

2.18.4.3 Differential Receiver (RX) Input Specifications

Table 50 defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 50. Differential Receiver (RX) Input Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$V_{RX-DIFFp-p}$	Differential peak-to-peak output voltage	0.175		1.200	V	$V_{RX-DIFFp-p}$ = 2*|V_{RX-D+} – $V_{RX-D–}$| See Note 2
T_{RX-EYE}	Minimum receiver eye width	0.4			UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER}$ = 1 – T_{RX-EYE}= 0.6 UI. See Notes 2 and 3
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.			0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3, and 7

Table 50. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$V_{RX-CM-ACp}$	AC peak common mode input voltage			150	mV	$V_{RX-CM-ACp} = \lvert V_{RXD+} - V_{RXD-}\rvert/2 - V_{RX-CM-DC}$ $V_{RX-CM-DC} = DC_{(avg)}$ of $\lvert V_{RX-D+} - V_{RX-D-}\rvert/2$ See Note 2
$RL_{RX-DIFF}$	Differential return loss	15			dB	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at +300 and –300 mV, respectively. See Note 4
RL_{RX-CM}	Common mode return loss	6			dB	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at 0 V. See Note 4
$Z_{RX-DIFF-DC}$	DC differential input impedance	80	100	120	Ω	RX DC differential mode impedance. See Note 5
Z_{RX-DC}	DC input impedance	40	50	60	Ω	Required RX D+ as well as D– DC impedance (50 ± 20% tolerance). See Notes 2 and 5
$Z_{RX-HIGH-IMP-DC}$	Powered down DC input impedance	200 k			Ω	Required RX D+ as well as D– DC Impedance when the receiver terminations do not have power. See Note 6
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65		175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2*\lvert V_{RX-D+} - V_{RX-D-}\rvert$ Measured at the package pins of the receiver
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected electrical idle enter detect threshold integration time			10	ms	An unexpected Electrical Idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition.

Table 51. JTAG DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN}[1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = mn, I_{OH} = –100 μA)	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 μA)	V_{OL}	—	0.2	V

Note:
1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2 and Table 3.

2.19.2 JTAG AC Electrical Specifications

Table 52 provides the JTAG AC timing specifications as defined in Figure 45 through Figure 47.

Table 52. JTAG AC Timing Specifications (Independent of SYSCLK)[1]

At recommended operating conditions (see Table 3).

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	
JTAG external clock cycle time	t_{JTG}	30	—	ns	
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	6
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 0	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 20 25	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 4 4	 20 25	ns	5
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 30 30	 — —	ns	5

3.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 53. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the Power Architecture technology. The device requires $\overline{\text{TRST}}$ to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP port connects primarily through the JTAG interface of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 52 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 52, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header shown in Figure 53; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 53 is common to all known emulators.

3.9.1 Termination of Unused Signals

If the JTAG interface and COP header will not be used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 53. If this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- Tie TCK to OV_{DD} through a 10-kΩ resistor. This will prevent TCK from changing state and reading incorrect data into the device.
- No connection is required for TDI, TMS, or TDO.

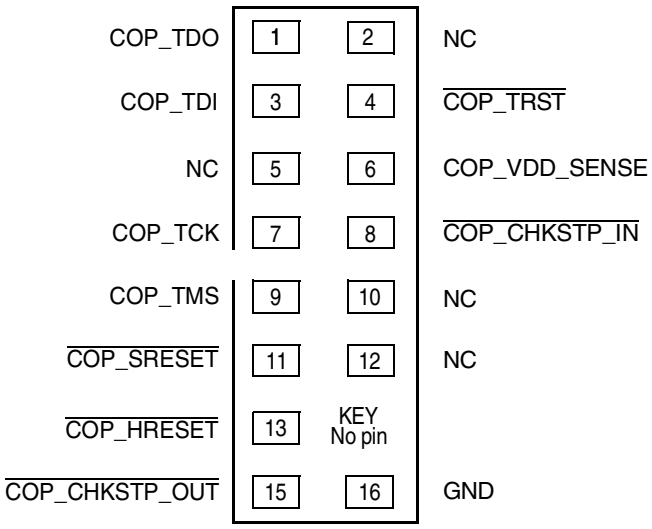


Figure 52. COP Connector Physical Pinout

3.10 Guidelines for High-Speed Interface Termination

3.10.1 SerDes Interface

The high-speed SerDes interface can be disabled through the POR input cfg_io_ports[0:2] and through the DEVDISR register in software. If a SerDes port is disabled through the POR input the user can not enable it through the DEVDISR register in software. However, if a SerDes port is enabled through the POR input the user can disable it through the DEVDISR register in software. Disabling a SerDes port through software should be done on a temporary basis. Power is always required for the SerDes interface, even if the port is disabled through either mechanism. Table 61 describes the possible enabled/disabled scenarios for a SerDes port. The termination recommendations must be followed for each port.

Table 61. SerDes Port Enabled/Disabled Configurations

	Disabled through POR input	Enabled through POR input
Enabled through DEVDISR	SerDes port is disabled (and cannot be enabled through DEVDISR) Complete termination required (Reference clock not required	SerDes port is enabled Partial termination may be required[1] (Reference clock is required)
Disabled through DEVDISR	SerDes port is disabled (through POR input) Complete termination required (Reference clock not required)	SerDes port is disabled after software disables port Same termination requirements as when the port is enabled through POR input[2] (Reference clock is required)

1 Partial termination when a SerDes port is enabled through both POR input and DEVDISR is determined by the SerDes port mode. If port 1 is in x4 PCI Express mode, no termination is required because all pins are being used. If port 1 is in x1/x2 PCI Express mode, termination is required on the unused pins. If port 2 is in x8 PCI Express mode, no termination is required because all pins are being used. If port 1 is in x1/x2/x4 PCI Express mode, termination is required on the unused pins.

2 If a SerDes port is enabled through the POR input and then disabled through DEVDISR, no hardware changes are required. Termination of the SerDes port should follow what is required when the port is enabled through both POR input and DEVDISR. See Note 1 for more information.

If the high-speed SerDes port requires complete or partial termination, the unused pins should be terminated as described in this section.

The following pins must be left unconnected (floating):

- SD*n*_TX[7:0]
- $\overline{\text{SD}n\text{\_TX}}$[7:0]

The following pins must be connected to GND:

- SD*n*_RX[7:0]
- $\overline{\text{SD}n\text{\_RX}}$[7:0]
- SD*n*_REF_CLK
- $\overline{\text{SD}n\text{\_REF\_CLK}}$

For other directions on reserved or no-connects pins, see Section 1, “Pin Assignments and Reset States.”

modeled as a collapsed thermal resistance with thermal conductivity of 12.1 W/(m • K) and an effective height of 0.1 mm. The thermal model uses median dimensions to reduce grid. Please refer to the case outline for actual dimensions.

The thermal model uses approximate dimensions to reduce grid. The approximations used do not impact thermal performance. Please refer to the case outline for exact dimensions.

Conductivity	Value	Unit
Die (8.5 x 9.7 x 0.86mm)		
Silicon	Temperature dependent	
Bump and Underfill (8.5 × 9.7 × 0.07 mm) Collapsed Resistance		
k_z	8.1	W/(m • K)
Substrate (29 × 29 × 1.18 mm)		
k_x	23.3	W/(m • K)
k_y	23.3	
k_z	0.95	
Solder and Air (29 × 29 × 0.4 mm)		
k_x	0.034	W/(m • K)
k_y	0.034	
k_z	12.1	

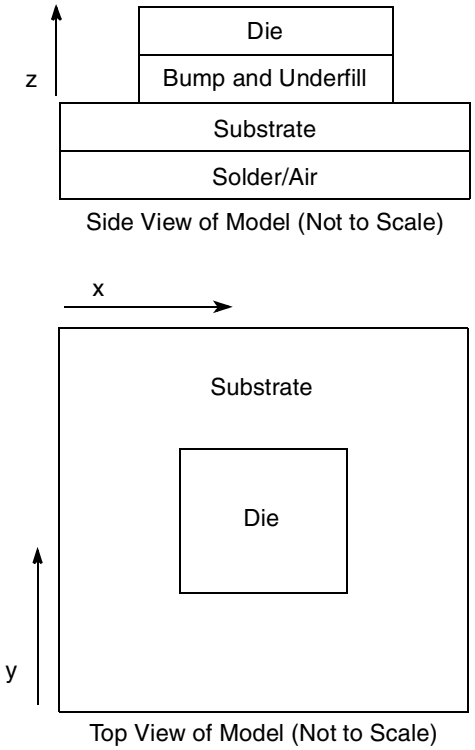


Figure 57. MPC8610 Thermal Model

3.12.2.5 Temperature Diode

The MPC8610 has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment. For proper operation, the monitoring device used should auto-calibrate the device by canceling out the V_{BE} variation of each MPC8610's internal diode.

The following are the specifications of the MPC8610 on-board temperature diode:

$V_f > 0.40$ V
$V_f < 0.90$ V
Operating range 2–300 µA
Diode leakage < 10 nA @ 125°C

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