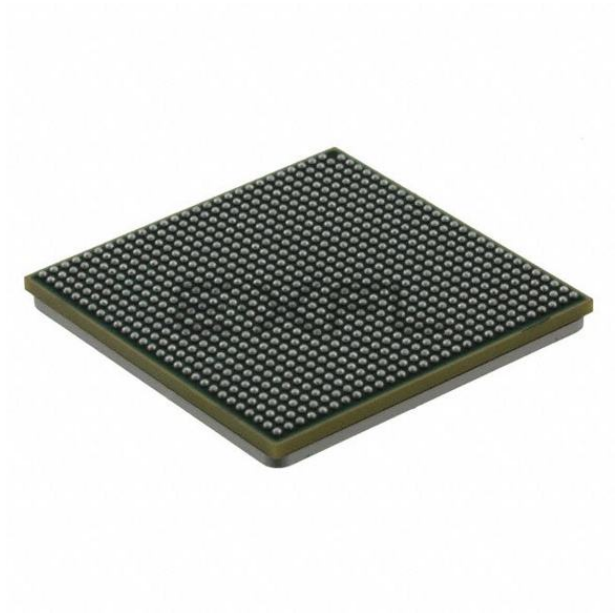

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Details	
Product Status	Obsolete
Core Processor	PowerPC e600
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.066GHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	DIU, LCD
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8610tpx1066jb

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Table 2. Absolute Maximum Ratings[1] (continued)

Characteristic	Symbol	Recommended Value	Unit	Notes
Storage temperature range	T_{STG}	–55 to 150	°C	

Notes:

1 Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2 During run time (M, B, O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Table 2.

2.1.2 Recommended Operating Conditions

Table 3 provides the recommended operating conditions for the MPC8610. Note that the values in Table 3 are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed. For details on order information and specific operating conditions for parts, see Section 4, "Ordering Information."

Table 3. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltages	V_{DD}_Core	1.025 ± 50 mV	V	1
		1.00 ± 50 mV		2
Core PLL supply	AV_{DD}_Core	1.025 ± 50 mV	V	1, 3
		1.00 ± 50 mV		2, 3
SerDes receiver and core power supply (ports 1 and 2)	$S1V_{DD}$ $S2V_{DD}$	1.025 ± 50 mV	V	1, 4
		1.00 ± 50 mV		2
SerDes transmitter power supply (ports 1 and 2)	$X1V_{DD}$ $X2V_{DD}$	1.025 ± 50 mV	V	1
		1.00 ± 50 mV		2
SerDes digital logic power supply (ports 1 and 2)	$L1V_{DD}$ $L2V_{DD}$	1.025 ± 50 mV	V	1
		1.00 ± 50 mV		2
Serdes PLL supply voltage (ports 1 and 2)	$SD1AV_{DD}$ $SD2AV_{DD}$	1.025 ± 50 mV	V	1, 3
		1.00 ± 50 mV		2, 3
Platform supply voltage	V_{DD}_PLAT	1.025 ± 50 mV	V	1
		1.00 ± 50 mV		2
PCI and platform PLL supply voltage	AV_{DD}_PCI AV_{DD}_PLAT	1.025 ± 50 mV	V	1, 3
		1.00 ± 50 mV		2, 3
DDR and DDR2 SDRAM I/O supply voltages	GV_{DD}	2.5 V ± 125 mV, 1.8 V ± 90 mV	V	5
Local bus and SSI I/O voltage	BV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV 1.8 V ± 90 mV	V	

Table 20 provides the input AC timing specifications for the DDR SDRAM when GV_{DD}(typ)=2.5 V.

Table 20. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V
AC input high voltage	V_{IH}	MV_{REF} + 0.31	—	V

Table 21 provides the input AC timing specifications for the DDR SDRAM interface.

Table 21. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC	t_{CISKEW}			ps	1, 2
533 MHz		–300	300		3
400 MHz		–365	365		
333 MHz		–390	390		

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[*n*] and any corresponding bit that will be captured with MDQS[*n*]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}.This can be determined by the following equation: $t_{DISKEW} = \pm(T/4 - abs(t_{CISKEW}))$, where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.
3. Maximum DDR1 frequency is 400 MHz.

Figure 4 shows the DDR SDRAM input timing for the MDQS to MDQ skew measurement (t_{DISKEW}).

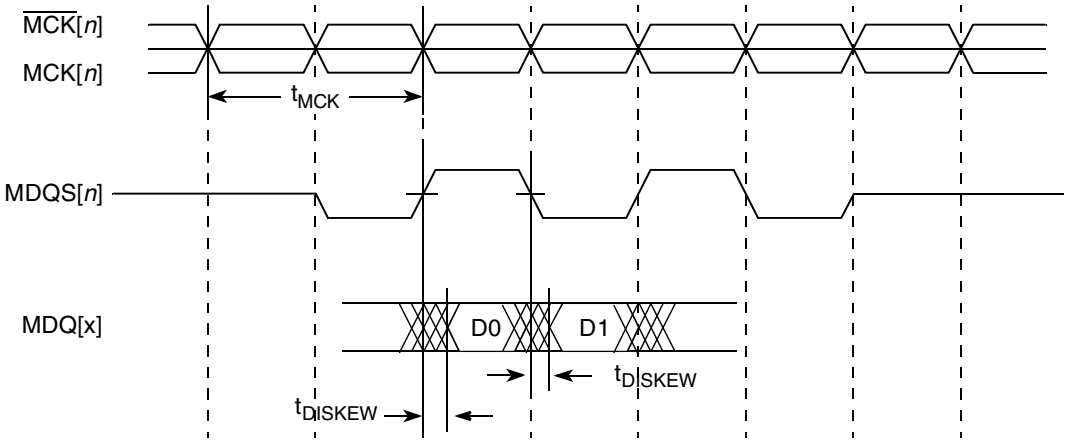

Figure 4. DDR Input Timing Diagram for tDISKEW

2.6.2.2 DDR SDRAM Output AC Timing Specifications

Table 22. DDR SDRAM Output AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MCK[n] cycle time, MCK[n]/$\overline{\text{MCK}}$[n] crossing	t_{MCK}	3	10	ns	2
MCK duty cycle	t_{MCKH}/t_{MCK}			%	
533 MHz		47	53		8
400 MHz		47	53		8
333 MHz		47	53		
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		
333 MHz		2.40	—		
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		
333 MHz		2.40	—		
$\overline{\text{MCS}}$[n] output setup with respect to MCK	t_{DDKHCS}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		
333 MHz		2.40	—		
$\overline{\text{MCS}}$[n] output hold with respect to MCK	t_{DDKHCX}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		
333 MHz		2.40	—		
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
533 MHz		590	—		7
400 MHz		700	—		
333 MHz		900	—		
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
533 MHz		590	—		7
400 MHz		700	—		
333 MHz		900	—		
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6

Table 22. DDR SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MDQS epilogue end	t_{DDKHME}	–0.6	0.6	ns	6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8610 Integrated Host Processor Reference Manual,* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[*n*] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
7. Maximum DDR1 frequency is 400 MHz.
8. Per the JEDEC spec the DDR2 duty cycle at 400 and 533 MHz is the low and high cycle time values.

NOTE

For the ADDR/CMD setup and hold specifications in Table 22, it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.

Figure 5 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

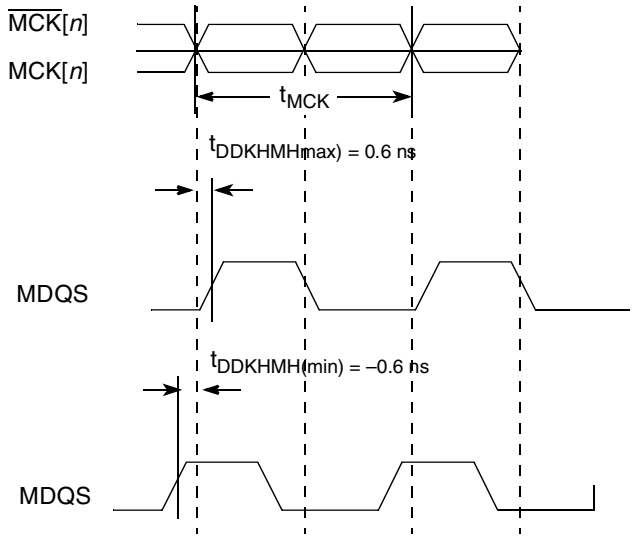

Figure 5. Timing Diagram for tDDKHMH

Figure 13 depicts the vertical timing (timing of one frame), including both the vertical sync pulse and the data. All parameters shown in the diagram are programmable.

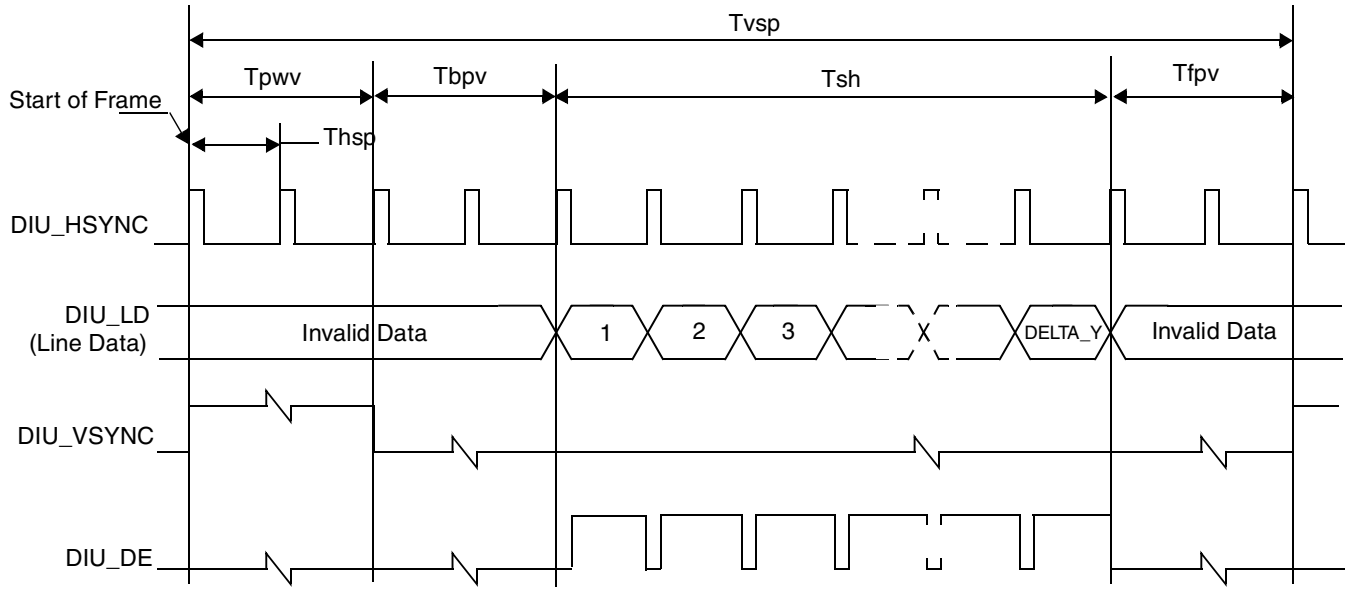

Figure 13. TFT DIU/LCD Interface Timing Diagram—Vertical Sync Pulse

Table 28 shows timing parameters of signals presented in Figure 12 and Figure 13.

Table 28. DIU Interface AC Timing Parameters—Pixel Level

Parameter	Symbol	Value	Unit	Notes
Display pixel clock period	t_{PCP}	7.5 (minimum)	ns	1, 2
HSYNC width	t_{PWH}	PW_H × t_{PCP}	ns	
HSYNC back porch width	t_{BPH}	BP_H × t_{PCP}	ns	
HSYNC front porch width	t_{FPH}	FP_H × t_{PCP}	ns	
Screen width	t_{SW}	DELTA_X × t_{PCP}	ns	
HSYNC (line) period	t_{HSP}	(PW_H + BP_H + DELTA_X + FP_H) × t_{PCP}	ns	
VSYNC width	t_{PWV}	PW_V × t_{HSP}	ns	
HSYNC back porch width	t_{BPV}	BP_V × t_{HSP}	ns	
HSYNC front porch width	t_{FPV}	FP_V × t_{HSP}	ns	
Screen height	t_{SH}	DELTA_Y × t_{HSP}	ns	
VSYNC (frame) period	t_{VSP}	(PW_V + BP_V + DELTA_Y + FP_H) × t_{HSP}	ns	

Notes:

1 Display interface pixel clock period immediate value (in nanoseconds).

2 Display pixel clock frequency must also be less than or equal to 1/3 the platform clock.

Table 31. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 30).

Parameter	Symbol[1]	Min	Max	Unit
Capacitive load for each bus line	Cb	—	400	pF

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. As a transmitter, the MPC8610 provides a delay time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of Start or Stop condition. When MPC8610 acts as the I²C bus master while transmitting, MPC8610 drives both SCL and SDA. As long as the load on SCL and SDA are balanced, MPC8610 would not cause unintended generation of Start or Stop condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for MPC8610 as transmitter, the following setting is recommended for the FDR bit field of the I2CFDR register to ensure both the desired I²C SCL clock frequency and SDA output delay time are achieved, assuming that the desired I²C SCL clock frequency is 400 kHz and the digital filter sampling rate register (I2CDFSRR) is programmed with its default setting of 0x10 (decimal 16):

I²C source clock frequency	533 MHz	400 MHz	333 MHz	266 MHz
FDR bit setting	0x0A	0x07	0x2A	0x05
Actual FDR divider selected	1536	1024	896	704
Actual I²C SCL frequency generated	347 kHz	391 kHz	371 kHz	378 kHz

   For the detail of I²C frequency calculation, refer to Freescale application note AN2919, *Determining the I²C Frequency Divider Ratio for SCL*. Note that the I²C source clock frequency is equal to the MPX clock frequency for MPC8610.
3. The maximum t_{I2DXKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. Guaranteed by design.

Figure 15 provides the AC test load for the I²C.

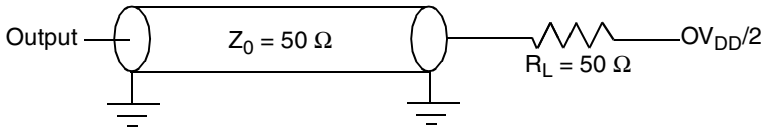

Figure 15. I²C AC Test Load

Figure 16 shows the AC timing diagram for the I²C bus.

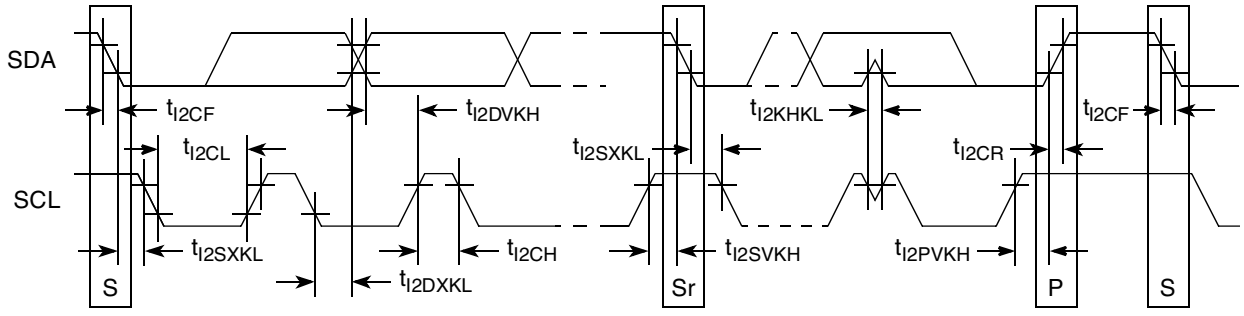

Figure 16. I²C Bus AC Timing Diagram

Table 34. SSI DC Electrical Characteristics (3.3 V DC)

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	BV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (BV_{IN}[1] = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±5	μA
High-level output voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	BV_{DD} – 0.2	—	V
Low-level output voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.2	V

Note:
1. The symbol BV_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 2 and Table 3.

2.12.2 SSI AC Timing Specifications

All timings for the SSI are given for a noninverted serial clock polarity (TSCKP/RSCKP = 0) and a noninverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the following tables and figures.

For internal frame sync operation using external clock, the FS timing will be same as that of Tx Data.

2.12.2.1 SSI Transmitter Timing with Internal Clock

Table 35 provides the transmitter timing parameters with internal clock.

Table 35. SSI Transmitter with Internal Clock Timing Parameters

Parameter	Symbol	Min	Max	Unit
Internal Clock Operation				
(Tx/Rx) CK clock period	SS1	81.4	—	ns
(Tx/Rx) CK clock high period	SS2	36.0	—	ns
(Tx/Rx) CK clock rise time	SS3	—	6	ns
(Tx/Rx) CK clock low period	SS4	36.0	—	ns
(Tx/Rx) CK clock fall time	SS5	—	6	ns
(Tx) CK high to FS high	SS10	—	15.0	ns
(Tx) CK high to FS low	SS12	—	15.0	ns
(Tx/Rx) internal FS rise time	SS14	—	6	ns
(Tx/Rx) internal FS fall time	SS15	—	6	ns
(Tx) CK high to STXD valid from high impedance	SS16	—	15.0	ns
(Tx) CK high to STXD high/low	SS17	—	15.0	ns
(Tx) CK high to STXD high impedance	SS18	—	15.0	ns
STXD rise/fall time	SS19	—	6	ns
Synchronous Internal Clock Operation				
SRXD setup before (Tx) CK falling	SS42	10.0	—	ns

Table 46. PCI AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	8, 11

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. All PCI signals are measured from $OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V PCI signaling levels.
4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Input timings are measured at the pin.
6. The timing parameter t_{SYS} indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see Section 3.1, "System Clocking."
7. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$.
8. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI 2.2 Local Bus Specifications*.
9. The reset assertion timing requirement for $\overline{\text{HRESET}}$ is 100 µs.
10. Guaranteed by characterization.
11. Guaranteed by design.
12. The timing parameter t_{PCKHOV} is a minimum of 1.5 ns and a maximum of 7.4 ns rather than the minimum of 2 ns and a maximum of 6 ns in the *PCI 2.2 Local Bus Specifications*.
13. The timing parameter t_{PCIVKH} is a minimum of 3.7 ns rather than the minimum of 3 ns in the *PCI 2.2 Local Bus Specifications*.
14. The timing parameter t_{PCIXKH} is a minimum of 0.8 ns rather than the minimum of 0 ns in the *PCI 2.2 Local Bus Specifications*.

Figure 15 provides the AC test load for PCI.

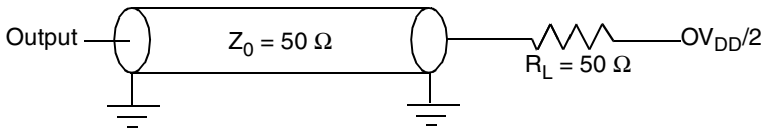

Figure 26. PCI AC Test Load

Figure 27 shows the PCI input AC timing conditions.

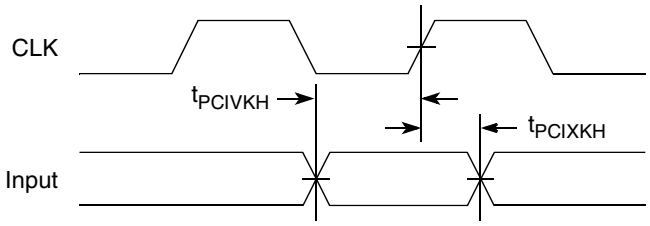

Figure 27. PCI Input AC Timing Measurement Conditions

Figure 28 shows the PCI output AC timing conditions.

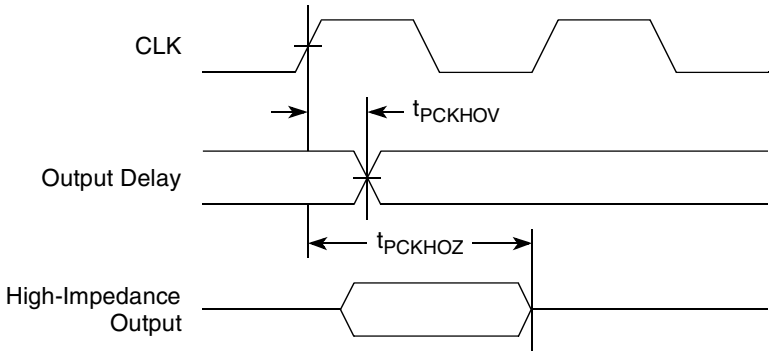

Figure 28. PCI Output AC Timing Measurement Condition

2.17 High-Speed Serial Interfaces (HSSI)

The MPC8610 features two Serializer/Deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. The SerDes1 interface is dedicated for PCI Express (x1/x2/x4) data transfers. The SerDes2 interface is dedicated for PCI Express (x1/x2/x4/x8) data transfers.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

2.17.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 29 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SD*n*_TX and $\overline{\text{SD}n\text{\_TX}}$) or a receiver input (SD*n*_RX and $\overline{\text{SD}n\text{\_RX}}$). Each signal swings between A volts and B volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. Single-ended swing

   The transmitter output signals and the receiver input signals SD*n*_TX, $\overline{\text{SD}n\text{\_TX}}$, SD*n*_RX, and $\overline{\text{SD}n\text{\_RX}}$ each have a peak-to-peak swing of A – B volts. This is also referred as each signal wire's single-ended swing.

2. Differential output voltage, V_{OD} (or differential output swing):

   The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SDn\_TX} - V_{\overline{SDn\_TX}}$. The V_{OD} value can be either positive or negative.

3. Differential input voltage, V_{ID} (or differential input swing):

   The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SDn\_RX} - V_{\overline{SDn\_RX}}$. The V_{ID} value can be either positive or negative.

4. Differential peak voltage, V_{DIFFp}

   The peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak voltage, $V_{DIFFp} = |A - B|$ volts.

5. Differential peak-to-peak, $V_{DIFFp-p}$

   Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to -(A – B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 * V_{DIFFp} = 2 * |(A - B)|$ volts, which is twice

2.17.2.3 Interfacing With Other Differential Signaling Levels

- With on-chip termination to SGND, the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC-coupled.
- Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

NOTE

Figure 34 to Figure 37 are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the MPC8610 SerDes reference clock receiver requirement provided in this document.

Figure 34 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with MPC8610 SerDes reference clock input's DC requirement.

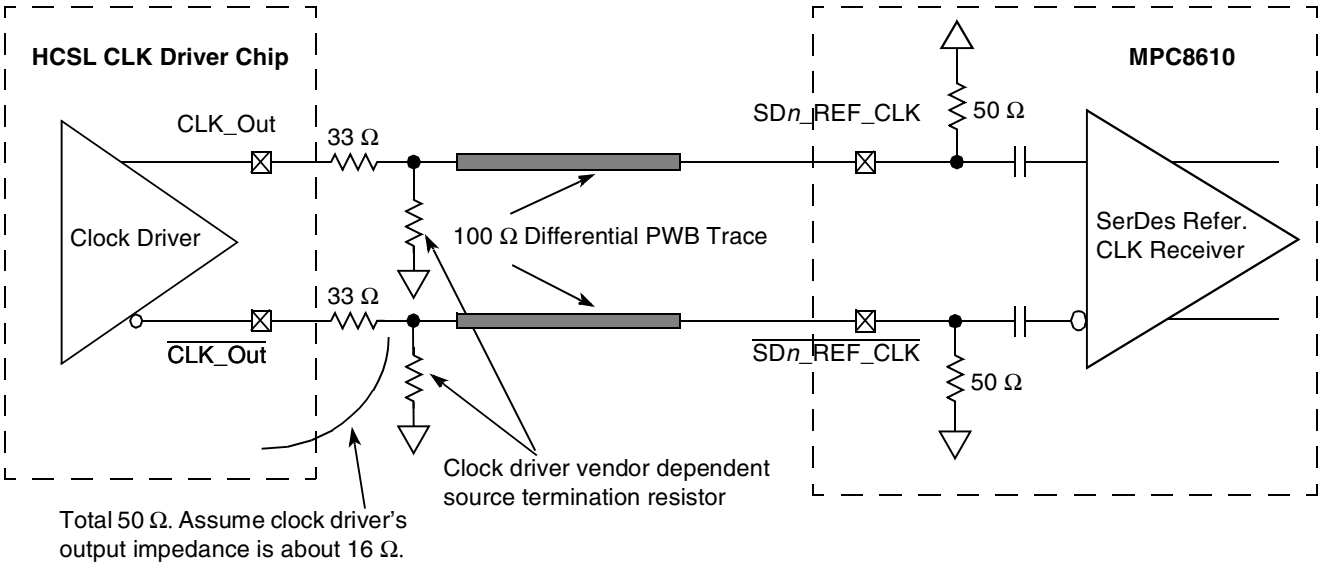

Figure 34. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

Figure 35 shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the MPC8610 SerDes reference clock input's allowed range (100 to 400 mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

Table 50. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$L_{TX-SKEW}$	Total skew			20	ns	Skew across all lanes on a link. This includes variation in the length of SKP ordered set (e.g., COM and one to five symbols) at the RX as well as any delay differences arising from the interconnect itself.

Notes:

1.)No test load is necessarily associated with this value.

2.)Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 43 should be used as the RX device when taking measurements (also refer to the receiver compliance eye diagram shown in Figure 42). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.

3.)A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.

4.)The receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D– line biased to –300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D– line (that is, as measured by a Vector Network Analyzer with 50-Ω probes—see Figure 43). Note that the series capacitors CTX is optional for the return loss measurement.

5.)Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.

6.)The RX DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit will not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.

7.)It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

2.18.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 42 is specified using the passive compliance/test measurement load (see Figure 43) in place of any real PCI Express RX component.

Note: In general, the minimum receiver eye diagram measured with the compliance/test measurement load (see Figure 43) will be larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum receiver eye diagram (shown in Figure 42) expected at the input receiver based on some adequate combination of system simulations and the return loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (i.e., as measured by a vector network analyzer with 50-Ω probes—see Figure 43). Note that the series capacitors, CTX, are optional for the return loss measurement.

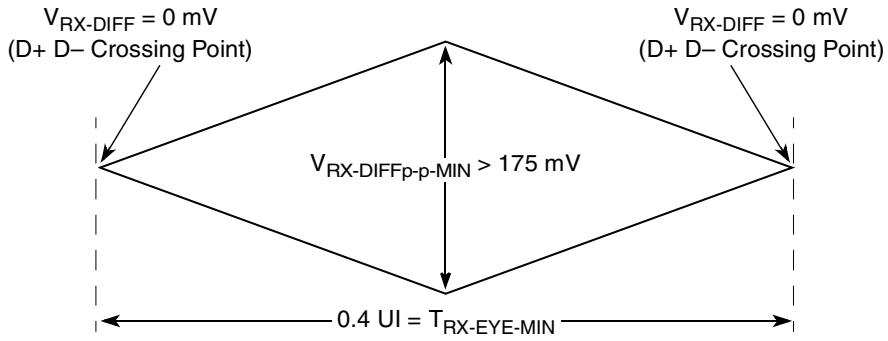

Figure 42. Minimum Receiver Eye Timing and Voltage Compliance Specification

2.18.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 43.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

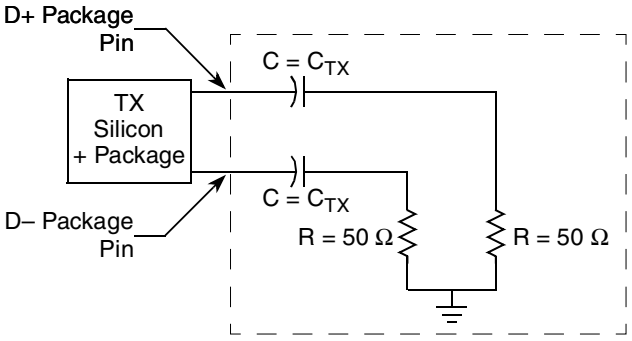

Figure 43. Compliance Test/Measurement Load

2.19 JTAG

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8610.

2.19.1 JTAG DC Electrical Characteristics

Table 51 provides the JTAG DC electrical characteristics for the JTAG interface.

Table 51. JTAG DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN}[1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = mn, I_{OH} = –100 μA)	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 μA)	V_{OL}	—	0.2	V

Note:
1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2 and Table 3.

2.19.2 JTAG AC Electrical Specifications

Table 52 provides the JTAG AC timing specifications as defined in Figure 45 through Figure 47.

Table 52. JTAG AC Timing Specifications (Independent of SYSCLK)[1]

At recommended operating conditions (see Table 3).

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	
JTAG external clock cycle time	t_{JTG}	30	—	ns	
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	6
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 0	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 20 25	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 4 4	 20 25	ns	5
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 30 30	 — —	ns	5

Figure 47 provides the boundary-scan timing diagram.

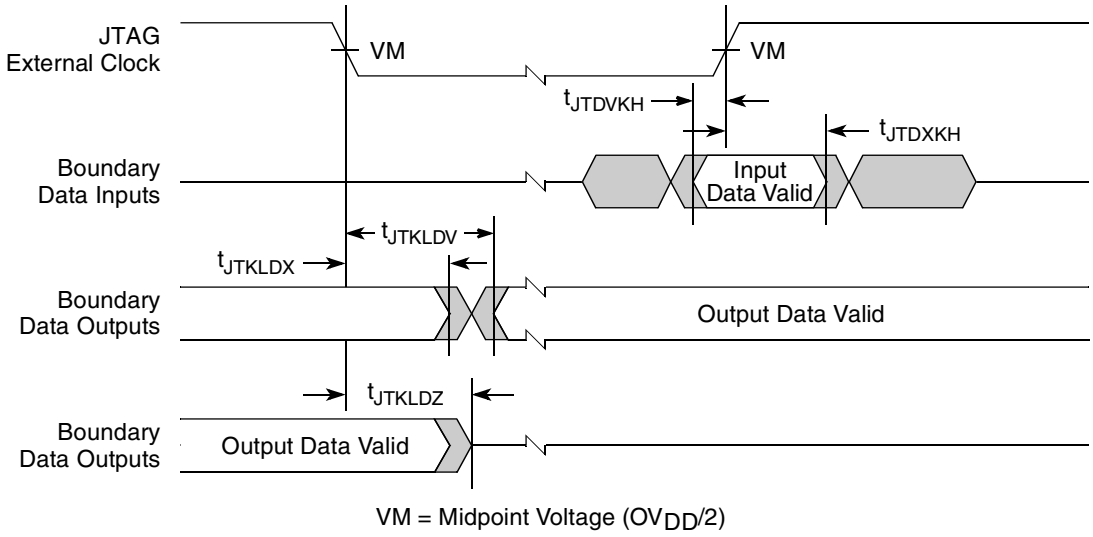

Figure 47. Boundary-Scan Timing Diagram

3 Hardware Design Considerations

This section provides electrical and thermal design recommendations for successful application of the MPC8610.

3.1 System Clocking

This section describes the PLL configuration of the MPC8610. Note that the platform clock is identical to the internal MPX bus clock.

This device includes six PLLs, as follows:

1. The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 3.1.2, “Platform/MPX to SYSCLK PLL Ratio.”
2. The e600 core PLL generates the core clock from the platform clock. The frequency ratio between the e600 core clock and the platform clock is selected using the e600 PLL ratio configuration bits as described in Section 3.1.3, “e600 Core to MPX/Platform Clock PLL Ratio.”
3. The PCI PLL generates the clocking for the PCI bus
4. Each of the two SerDes blocks has a PLL.

- SerDes—Receiver lanes configured for PCI Express are allowed to be disconnected (as would occur when a PCI Express slot is connected but not populated). Directions for terminating the SerDes signals is discussed in Section 3.10, "Guidelines for High-Speed Interface Termination."

3.6 Pull-Up and Pull-Down Resistor Requirements

The MPC8610 requires weak pull-up resistors (2–10 kΩ is recommended) on open drain type pins including I^2C pins and PIC interrupt pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 53. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Refer to the PCI 2.2 specification for all pull-ups required for PCI.

The following pins must not be pulled down during power-on reset: DIU_LD[5:6], MSRCID[1:2], $\overline{\text{HRESET\_REQ}}$, and TRIG_OUT/READY.

The following are factory test pins and require strong pull up resistors (100 Ω – 1 kΩ) to OV_{DD}: $\overline{\text{LSSD\_MODE}}$, TEST_MODE[0:3].

The following pins require weak pull-up resistors (2–10 kΩ) to their specific power supplies: $\overline{\text{LCS}}$[0:4], $\overline{\text{LCS}}$[5]/$\overline{\text{DMA_DREQ}}$2, $\overline{\text{LCS}}$[6]/$\overline{\text{DMA\_DACK}}$[2], $\overline{\text{LCS}}$[7]/$\overline{\text{DMA\_DDONE}}$[2], IRQ_OUT, IIC1_SDA, IIC1_SCL, IIC2_SDA, IIC2_SCL, and CKSTP_OUT.

The following pins should be pulled to ground with a 100-Ω resistor: SD1_IMP_CAL_TX, SD2_IMP_CAL_TX. The following pins should be pulled to ground with a 200-Ω resistor: SD1_IMP_CAL_RX, SD2_IMP_CAL_RX.

When the platform frequency is 400 MHz, cfg_platform_freq must be pulled down at reset. Also, cfg_dram_type[0 or 1] must be valid at power-up even before $\overline{\text{HRESET}}$ assertion.

For other pin pull-up or pull-down recommendations of signals, see Section 1, "Pin Assignments and Reset States."

3.7 Output Buffer DC Impedance

The MPC8610 drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 51). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and

3.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 53. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the Power Architecture technology. The device requires $\overline{\text{TRST}}$ to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP port connects primarily through the JTAG interface of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 52 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 52, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header shown in Figure 53; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 53 is common to all known emulators.

3.9.1 Termination of Unused Signals

If the JTAG interface and COP header will not be used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 53. If this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- Tie TCK to OV_{DD} through a 10-kΩ resistor. This will prevent TCK from changing state and reading incorrect data into the device.
- No connection is required for TDI, TMS, or TDO.

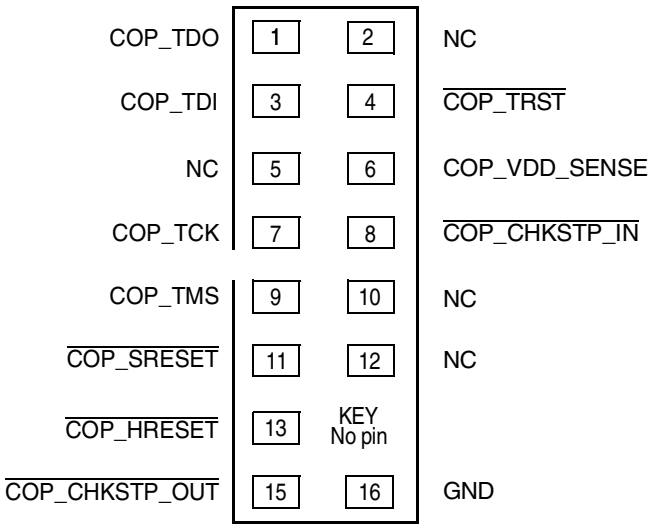

Figure 52. COP Connector Physical Pinout

Thermagon Inc. 888-246-9050
4707 Detroit Ave.
Cleveland, OH 44102
Internet: www.thermagon.com

3.12.2.3 Heat Sink Selection Example

This section provides a heat sink selection example using one of the commercially available heat sinks.

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_i + T_r + (R_{\theta JC} + R_{\theta int} + R_{\theta sa}) \times P_d$$

where:

T_j is the die-junction temperature
T_i is the inlet cabinet ambient temperature
T_r is the air temperature rise within the computer cabinet
$R_{\theta JC}$ is the junction-to-case thermal resistance
$R_{\theta int}$ is the adhesive or interface material thermal resistance
$R_{\theta sa}$ is the heat sink base-to-ambient thermal resistance
P_d is the power dissipated by the device

During operation, the die-junction temperatures (T_j) should be maintained less than the value specified in Table 3. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_i) may range from 30° to 40°C. The air temperature rise within a cabinet (T_r) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material ($R_{\theta int}$) is typically about 0.2°C/W. For example, assuming a T_i of 30°C, a T_r of 5°C, a package $R_{\theta JC}$ = 0.1, and a typical power consumption (P_d) of 10 W, the following expression for T_j is obtained:

Die-junction temperature: $T_j = 30°C + 5°C + (0.1°C/W + 0.2°C/W + \theta_{sa}) \times 10\ W$

For this example, a $R_{\theta sa}$value of 6.7°C/W or less is required to maintain the die junction temperature below the maximum value of Table 3.

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, and so on.

Due to the complexity and variety of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board as well as system-level designs.

3.12.2.4 Recommended Thermal Model

For system thermal modeling, the MPC8610 thermal model is shown in Figure 57. Four cuboids are used to represent this device. The die is modeled as 8.5 × 9.7 mm at a thickness of 0.86 mm. See Section 2.3, “Power Characteristics,” for power dissipation details. The substrate is modeled as a single block 29 × 29 × 1.18 mm with orthotropic conductivity of 23.3 W/(m • K) in the xy-plane and 0.95 W/(m • K) in the z-direction. The die is centered on the substrate. The bump/underfill layer is modeled as a collapsed thermal resistance between the die and substrate with a conductivity of 8.1 W/(m • K) in the thickness dimension of 0.07 mm. The C5 solder layer is modeled as a cuboid with dimensions 29 × 29 × 0.4 mm with orthotropic thermal conductivity of 0.034 W/(m • K) in the xy-plane and 12.1 W/(m • K) in the z-direction. An LGA solder layer would be

6 Product Documentation

The following documents are required for a complete description of the device and are needed to design properly with the part.

- *MPC8610 Integrated Host Processor Reference Manual* (document number: MPC8610RM)
- *e600 PowerPC Core Reference Manual* (document number: E600CORERM)

7 Revision History

Table 65 summarizes revisions to this document.

Table 65. Revision History

Rev. No.	Date	Substantive Change(s)
2	1/2009	• Updated Table of Contents • Removed subheading Section 1.1. pin assignments. • Promoted section 4.3, “Ordering Information,” and associated subsections to Section 4, “Ordering Information.” Renumbered subsequent sections and subsections accordingly.
1	01/2009	• Updated Table of Contents • Removed Serial Rapid IO from Section 2.4.4, “Platform Frequency Requirements for PCI-Express” because SRIO is not available on MPC8610. • Removed note in Table 21 and Table 22 that states “Minimum DDR2 frequency is 400 MHz.” • In Table 31, removed rows for t_{i2cr} and t_{i2CF}. Added row for Cb. • Replaced 1067 with 1066 in Table 63. • Replaced CBGA with PBGA in Section 5.1, “Package Parameters for the MPC8610.”
0	10/2008	Initial release.