# E·XFL



#### Welcome to E-XFL.COM

#### Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

#### Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	PowerPC e600
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	·
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	DIU, LCD
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8610tpx800gb

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

## **Table of Contents**

1	Pin A	ssignments and Reset States4
2	Elect	rical Characteristics
	2.1	Overall DC Electrical Characteristics15
	2.2	Power Sequencing
	2.3	Power Characteristics
	2.4	Input Clocks
	2.5	RESET Initialization
	2.6	DDR and DDR2 SDRAM25
	2.7	Local Bus
	2.8	Display Interface Unit
	2.9	l <sup>2</sup> C
	2.10	DUART
	2.11	Fast/Serial Infrared Interfaces (FIRI/SIRI)42
	2.12	Synchronous Serial Interface (SSI)42
	2.13	Global Timer Module
	2.14	GPIO
	2.15	Serial Peripheral Interface (SPI)
	2.16	PCI Interface
	2.17	High-Speed Serial Interfaces (HSSI)54
	2.18	PCI Express
	2.19	JTAG
3	Hard	ware Design Considerations

	3.1	System Clocking
	3.2	Power Supply Design and Sequencing
	3.3	Decoupling Recommendations
	3.4	SerDes Block Power Supply Decoupling
		Recommendations
	3.5	Connection Recommendations
	3.6	Pull-Up and Pull-Down Resistor Requirements 78
	3.7	Output Buffer DC Impedance
	3.8	Configuration Pin Muxing
	3.9	JTAG Configuration Signals
	3.10	Guidelines for High-Speed Interface Termination 83
	3.11	Guidelines for PCI Interface Termination
	3.12	Thermal
4	Orde	ring Information
	4.1	Part Numbers Fully Addressed by This Document 90
	4.2	Part Marking
5	Pack	age Information
	5.1	Package Parameters for the MPC8610 92
	5.2	Mechanical Dimensions of the MPC8610 FC-PBGA 93
6	Prod	uct Documentation
7	Revis	sion History

MPC8610 Integrated Host Processor Hardware Specifications, Rev. 2

NP



Figure 3 illustrates the power up sequence as described above.



#### Notes:

- 1. Dotted waveforms correspond to optional supply values for a specified power supply. See Table 3.
- 2. Ther recommended maximum ramp up time for power supplies is 20 milliseconds.
- 3. Refer to Section 2.5, "RESET Initialization" for additional information on PLL relock and reset signal assertion timing requirements.
- Refer to Table 9 for additional information on reset configuration pin setup timing requirements. In addition see Figure 53 regarding HRESET and JTAG connection details including TRST.
- 5. e600 PLL relock time is 100 microseconds maximum plus 255 MPX\_clk cycles.
- 6. Stable PLL configuration signals are required as stable SYSCLK is applied. All other POR configuration inputs are required 4 SYSCLK cycles before HRESET negation and are valid at least 2 SYSCLK cycles after HRESET has negated (hold requirement). See Section 2.5, "RESET Initialization," for more information on setup and hold time of reset configuration signals.
- 7. The rail for V<sub>DD</sub>\_PLAT, AV<sub>DD</sub>\_PLAT, V<sub>DD</sub>\_Core, AV<sub>DD</sub>\_Core, AV<sub>DD</sub>\_PCI, SnV<sub>DD</sub>, XnV<sub>DD</sub>, and SDnAV<sub>DD</sub> must reach 90% of its value before the rail for GV<sub>DD</sub> and MV<sub>REF</sub> reaches 10% of its value.
- 8. SYSCLK must be driven only AFTER the power for the various power supplies is stable.
- 9. The reset configuration signals for DRAM types must be valid before HRESET is asserted.

Figure 3. MPC8610 Power Up Sequencing





### 2.3 **Power Characteristics**

The power dissipation for the MPC8610 device is shown in Table 5.

Table 5.	MPC8610	Power	Dissipation
----------	---------	-------	-------------

Power Mode	Core/Platform Frequency (MHz)	V <sub>DD</sub> _Core, V <sub>DD</sub> _PLAT (V)	Junction Temperature (°C)	Power (Watts)	Notes
Typical			65	10.7	1, 2
Thermal	1333/533	1.025	105	12.1	1, 3
Maximum			105	16	1, 4
Typical			65	8.4	1, 2
Thermal	1066/533	1.00	105	9.8	1, 3
Maximum			105	13	1, 4
Typical			65	5.8	1, 2
Thermal	800/400	1.00	105	7.2	1, 3
Maximum			105	9.5	1, 4

#### Notes:

1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.

- Typical power is an average value measured at the nominal recommended core voltage (V<sub>DD</sub>\_Core) and 65°C junction temperature (see Table 3) while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz with the core at 100% efficiency. This parameter is not 100% tested but periodically sampled.
- 3. Thermal power is the average power measured at nominal core voltage (V<sub>DD</sub>\_Core) and maximum operating junction temperature (see Table 3) while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz on the core and a typical workload on platform interfaces. This parameter is not 100% tested but periodically sampled.
- 4. Maximum power is the maximum power measured at nominal core voltage (V<sub>DD</sub>\_Core) and maximum operating junction temperature (see Table 3) while running a test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep all the execution units maximally busy on the core.

The estimated maximum power dissipation for individual power supplies of the MPC8610 is shown in Table 6.

Table 6. MPC8610 Individual Supply Maximum Power Dissipation <sup>1</sup>
---

Component Description	Supply Voltage (V)	Est. Power (Watts)	Notes
Core voltage supply	V <sub>DD</sub> _Core = 1.025 V @ 1333 MHz	14.0	
	V <sub>DD</sub> _Core = 1.00 V @ 1066 MHz	12.0	
Core PLL voltage supply	AV <sub>DD</sub> _Core = 1.025 V @ 1333 MHz	0.0125	
	AV <sub>DD</sub> _Core = 1.00 V @ 1066 MHz	0.0125	
Platform source supply	V <sub>DD</sub> _PLAT = 1.025 V @ 1333 MHz	4.5	
	V <sub>DD</sub> _PLAT = 1.00 V @ 1066 MHz	4.3	



#### Table 22. DDR SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions.

Parameter	Symbol <sup>1</sup>	Min	Мах	Unit	Notes
MDQS epilogue end	t <sub>DDKHME</sub>	-0.6	0.6	ns	6

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t<sub>DDKHAS</sub> symbolizes DDR timing (DD) for the time t<sub>MCK</sub> memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t<sub>DDKLDX</sub> symbolizes DDR timing (DD) for the time t<sub>MCK</sub> memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
  </sub>
- 2. All MCK/MCK referenced measurements are made from the crossing of the two signals ±0.1 V.
- 3. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK, MCS, and MDQ/MECC/MDM/MDQS.
- 4. Note that t<sub>DDKHMH</sub> follows the symbol conventions described in note 1. For example, t<sub>DDKHMH</sub> describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t<sub>DDKHMH</sub> can be modified through control of the DQSS override bits in the TIMING\_CFG\_2 register. This will typically be set to the same delay as the clock adjust in the CLK\_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the MPC8610 Integrated Host Processor Reference Manual, for a description and understanding of the timing modifications enabled by use of these bits.
- 5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
- 6. All outputs are referenced to the rising edge of MCK[*n*] at the pins of the microprocessor. Note that t<sub>DDKHMP</sub> follows the symbol conventions described in note 1.
- 7. Maximum DDR1 frequency is 400 MHz.
- 8. Per the JEDEC spec the DDR2 duty cycle at 400 and 533 MHz is the low and high cycle time values.

#### NOTE

For the ADDR/CMD setup and hold specifications in Table 22, it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.

Figure 5 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t<sub>DDKHMH</sub>).



Figure 5. Timing Diagram for tDDKHMH



**Electrical Characteristics** 

Figure 6 shows the DDR SDRAM output timing diagram.



Figure 6. DDR SDRAM Output Timing Diagram

Figure 7 provides the AC test load for the DDR bus.



Figure 7. DDR AC Test Load

### 2.7 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8610.

### 2.7.1 Local Bus DC Electrical Characteristics

Table 23 provides the DC electrical characteristics for the local bus interface operating at  $BV_{DD} = 3.3$  V.

Table 23. Loca	I Bus DC Electrical	Characteristics	$(BV_{DD} = 3.3)$	V)
----------------	---------------------	-----------------	-------------------	----

Parameter	Symbol	Min	Мах	Unit
High-level input voltage	V <sub>IH</sub>	2	BV <sub>DD</sub> + 0.3	V
Low-level input voltage	V <sub>IL</sub>	-0.3	0.8	V
Input current $(V_{IN}^{1} = 0 V \text{ or } V_{IN} = BV_{DD})$	I <sub>IN</sub>	—	±5	μA
High-level output voltage ( $BV_{DD} = min, I_{OH} = -2 mA$ )	V <sub>OH</sub>	BV <sub>DD</sub> – 0.2	—	V



The DELTA\_X and DELTA\_Y parameters are programmed via the DISP\_SIZE register. The PW\_H, BP\_H, and FP\_H parameters are programmed via the HSYN\_PARA register; and the PW\_V, BP\_V, and FP\_V parameters are programmed via the VSYN\_PARA register.

Figure 14 depicts the synchronous display interface timing for access level, and Table 29 lists the timing parameters.



#### Figure 14. LCD Interface Timing Diagram—Access Level

#### NOTE

The DIU\_OUT\_CLK edge and phase delay is selectable via the Global Utilities CKDVDR register.

Table 29. LCD Interface Timing Parameters—Access Level

Parameter	Symbol	Min	Тур	Мах	Unit
LCD interface pixel clock high time	t <sub>CKH</sub>	$0.35  imes t_{PCP}$	$0.5  imes t_{PCP}$	$0.65  imes t_{PCP}$	ns
LCD interface pixel clock low time	t <sub>CKL</sub>	$0.35  imes t_{PCP}$	$0.5  imes t_{PCP}$	$0.65  imes t_{PCP}$	ns
LCD interface pixel clock to ouput valid	t <sub>DIUKHOV</sub>	—	_	2	ns
LCD interface output hold from pixel clock	t <sub>DIUKHOX</sub>	t <sub>PCP</sub> – 2	—	—	ns

### 2.9 I<sup>2</sup>C

This section describes the DC and AC electrical characteristics for the  $I^2C$  interfaces of the MPC8610.

### 2.9.1 I<sup>2</sup>C DC Electrical Characteristics

Table 30 provides the DC electrical characteristics for the I<sup>2</sup>C interfaces.

#### Table 30. I<sup>2</sup>C DC Electrical Characteristics

At recommended operating conditions with  $\text{OV}_{\text{DD}}$  of 3.3 V ± 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
Input high voltage level	V <sub>IH</sub>	$0.7  imes OV_{DD}$	OV <sub>DD</sub> + 0.3	V	
Input low voltage level	V <sub>IL</sub>	-0.3	$0.3  imes OV_{DD}$	V	
Low level output voltage	V <sub>OL</sub>	0	$0.2 \times \text{OV}_{\text{DD}}$	V	1
Pulse width of spikes which must be suppressed by the input filter	t <sub>I2KHKL</sub>	0	50	ns	2



#### Table 30. I<sup>2</sup>C DC Electrical Characteristics (continued)

At recommended operating conditions with  $\text{OV}_{\text{DD}}$  of 3.3 V  $\pm\,5\%.$ 

Parameter	Symbol	Min	Мах	Unit	Notes
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$ (max)	I	-10	10	μA	3
Capacitance for each I/O pin	CI	-	10	pF	

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.

2. Refer to the MPC8610 Integrated Host Processor Reference Manual, for information on the digital filter used.

3. I/O pins will obstruct the SDA and SCL lines if  $\mathrm{OV}_{\mathrm{DD}}$  is switched off.

### 2.9.2 I<sup>2</sup>C AC Electrical Specifications

Table 31 provides the AC timing parameters for the  $I^2C$  interfaces.

#### Table 31. I<sup>2</sup>C AC Electrical Specifications

All values refer to  $V_{IH}$  (min) and  $V_{IL}$  (max) levels (see Table 30).

Parameter	Symbol <sup>1</sup>	Min	Мах	Unit
SCL clock frequency	f <sub>I2C</sub>	0	400	kHz
Low period of the SCL clock	t <sub>I2CL</sub> 4	1.3	—	μs
High period of the SCL clock	t <sub>I2CH</sub> 4	0.6	—	μs
Setup time for a repeated START condition	t <sub>I2SVKH</sub> 4	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t <sub>I2SXKL</sub> 4	0.6	_	μs
Data setup time	t <sub>I2DVKH</sub> 4	100	—	ns
Data input hold time: CBUS compatible masters I <sup>2</sup> C bus devices	t <sub>I2DXKL</sub>	0 <sup>2</sup>		μs
Data ouput delay time	t <sub>I2OVKL</sub>	—	0.9 <sup>3</sup>	μs
Setup time for STOP condition	t <sub>I2PVKH</sub>	0.6	—	μs
Bus free time between a STOP and START condition	t <sub>I2KHDX</sub>	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V <sub>NL</sub>	$0.1 \times OV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V <sub>NH</sub>	$0.2 \times OV_{DD}$	_	V



Parameter	Symbol	Min	Мах	Unit
SRXD hold after (Tx) CK falling	SS43	0	—	ns
Loading	SS52	_	25	pF

Table 35. SSI Transmi	itter with Internal	Clock Timing	Parameters	(continued)
-----------------------	---------------------	--------------	------------	-------------

Figure 17 provides the SSI transmitter timing with internal clock.



Figure 17. SSI Transmitter with Internal Clock Timing Diagram



### 2.12.2.2 SSI Receiver Timing with Internal Clock

Table 36 provides the receiver timing parameters with internal clock.

Table 36. SSI Receiver with Internal Clock Timing Parameters

Parameter	Symbol	Min	Мах	Unit				
Internal Clock Operation								
(Tx/Rx) CK clock period	SS1	81.4	—	ns				
(Tx/Rx) CK clock high period	SS2	36.0	—	ns				
(Tx/Rx) CK clock rise time	SS3	—	6	ns				
(Tx/Rx) CK clock low period	SS4	36.0	—	ns				
(Tx/Rx) CK clock fall time	SS5	—	6	ns				
(Rx) CK high to FS high	SS11	—	15.0	ns				
(Rx) CK high to FS low	SS13	—	15.0	ns				
SRXD setup time before (Rx) CK low	SS20	10.0	—	ns				
SRXD hold time after (Rx) CK low	SS21	0	—	ns				

Figure 18 provides the SSI receiver timing with internal clock.



Figure 18. SSI Receiver with Internal Clock Timing Diagram

### 2.12.2.3 SSI Transmitter Timing with External Clock

Table 37 provides the transmitter timing parameters with external clock.

#### Table 37. SSI Transmitter with External Clock Timing Parameters

Parameter	Symbol	Min	Мах	Unit					
External Clock Operation									
(Tx/Rx) CK clock period	SS22	81.4	—	ns					
(Tx/Rx) CK clock high period	SS23	36.0	—	ns					
(Tx/Rx) CK clock rise time	SS24	—	6.0	ns					



### 2.14 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8610.

### 2.14.1 GPIO DC Electrical Characteristics

Table 41 provides the DC electrical characteristics for the GPIO.

#### Table 41. GPIO DC Electrical Characteristics

Parameter	Symbol	Min	Мах	Unit
High-level input voltage	V <sub>IH</sub>	2	OV <sub>DD</sub> + 0.3	V
Low-level input voltage	V <sub>IL</sub>	-0.3	0.8	V
Input current ( $V_{IN}^{1} = 0 V \text{ or } V_{IN} = V_{DD}$ )	I <sub>IN</sub>	—	±5	μA
High-level output voltage (OV <sub>DD</sub> = min, $I_{OH}$ = -100 $\mu$ A)	V <sub>OH</sub>	OV <sub>DD</sub> - 0.2	—	V
Low-level output voltage (OV <sub>DD</sub> = min, $I_{OL}$ = 100 $\mu$ A)	V <sub>OL</sub>	—	0.2	V

#### Note:

1. The symbol V<sub>IN</sub>, in this case, represents the OV<sub>IN</sub> symbol referenced in Table 2 and Table 3.

### 2.14.2 GPIO AC Timing Specifications

Table 42 provides the GPIO input and output AC timing specifications.

#### Table 42. GPIO Input and Output AC Timing Specifications<sup>1</sup>

Characteristic	Symbol <sup>2</sup>	Min	Unit	Notes
GPIO inputs—minimum pulse width	t <sub>GPIWID</sub>	7.5	ns	3
GPIO outputs—minimum pulse width	t <sub>GPOWID</sub>	12	ns	

#### Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

- GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any
  external synchronous logic. GPIO inputs are required to be valid for at least t<sub>PIWID</sub> ns to ensure proper operation.
- 3. The minimum pulse width is a function of the MPX/platform clock. The minimum pulse width must be greater than or equal to 4 times the MPX/platform clock period.

Figure 22 provides the AC test load for the GPIO.



Figure 22. GPIO AC Test Load



Figure 23 provides the AC test load for the SPI.



Figure 23. SPI AC Test Load

Figure 24 through Figure 25 represent the AC timings from Table 44. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 24 shows the SPI timings in slave mode (external clock).





Figure 25 shows the SPI timings in master mode (internal clock).



Figure 25. SPI AC Timing in Master Mode (Internal Clock) Diagram

# NP

#### **Electrical Characteristics**

Figure 37 shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with MPC8610 SerDes reference clock input's DC requirement.



Figure 37. Single-Ended Connection (Reference Only)

### 2.17.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 1–15 MHz range. The source impedance of the clock driver should be 50  $\Omega$  to match the transmission line and reduce reflections which are a source of noise to the system.

Table 47 describes some AC parameters common to PCI Express protocols.

#### Table 47. SerDes Reference Clock Common AC Parameters

At recommended operating conditions with X1V\_{DD} or X2V\_{DD} = 1.0 V  $\pm$  5% and 1.025 V  $\pm$  5%.

Parameter	Symbol	Min	Мах	Unit	Notes
Rising Edge Rate	Rise Edge Rate	1.0	4.0	V/ns	2, 3
Falling Edge Rate	Fall Edge Rate	1.0	4.0	V/ns	2, 3
Differential Input High Voltage	V <sub>IH</sub>	+200		mV	2
Differential Input Low Voltage	V <sub>IL</sub>	_	-200	mV	2



### 2.18.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the transport and data link layer, use the *PCI Express Base Specification*, Rev. 1.0a.

### 2.18.4.1 Differential Transmitter (TX) Output

Table 49 defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit interval	399.88	400	400.12	ps	Each UI is 400 ps $\pm$ 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1
V <sub>TX-DIFFp-p</sub>	Differential peak-to-peak output voltage	0.8		1.2	V	$V_{TX-DIFFp-p} = 2^*  V_{TX-D+} - V_{TX-D-} $ See Note 2
V <sub>TX-DE-RATIO</sub>	De- emphasized differential output voltage (ratio)	-3.0	-3.5	-4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 2
T <sub>TX-EYE</sub>	Minimum TX eye width	0.70			UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3$ UI. See Notes 2 and 3
T <sub>TX-EYE-MEDIAN-to-</sub> MAX-JITTER	Maximum time between the jitter median and maximum deviation from the median.			0.15	UI	Jitter is defined as the measurement variation of the crossing points ( $V_{TX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3
T <sub>TX-RISE</sub> , T <sub>TX-FALL</sub>	D+/D- TX output rise/fall time	0.125			UI	See Notes 2 and 5
V <sub>TX-CM-ACp</sub>	RMS AC peak common mode output voltage			20	mV	$\begin{split} & V_{TX\text{-}CM\text{-}ACp} = RMS(IV_{TXD\text{+}} - V_{TXD\text{-}}I/2 - V_{TX\text{-}CM\text{-}DC}) \\ & V_{TX\text{-}CM\text{-}DC} = DC_{(avg)} \text{ of } IV_{TX\text{-}D\text{+}} - V_{TX\text{-}D\text{-}}I/2 \\ & See Note 2 \end{split}$
V <sub>TX-CM-DC-ACTIVE-</sub> IDLE-DELTA	Absolute delta of DC common mode voltage during LO and electrical idle	0		100	mV	$eq:logical_lo$
V <sub>TX-CM</sub> -DC-LINE-DELTA	Absolute delta of DC common mode between D+ and D-	0		25	mV	$\begin{split} & V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-}  <= 25 \text{ mV} \\ &V_{TX-CM-DC-D+} = DC_{(avg)} \text{ of }  V_{TX-D+}  \\ &V_{TX-CM-DC-D-} = DC_{(avg)} \text{ of }  V_{TX-D-}  \\ &\text{See Note } 2 \end{split}$

Tahla 10	Differential	Tranemitter	(ΤΥ	) Out	nut S	nocific	atione
	Differential	manamiller	$(I \Lambda)$	, Out	pui J	pecilic	alions



#### Table 52. JTAG AC Timing Specifications (Independent of SYSCLK)<sup>1</sup> (continued)

At recommended operating conditions (see Table 3).

Parameter	Symbol <sup>2</sup>	Min	Мах	Unit	Notes
JTAG external clock to output high impedance: Boundary-scan data TDO	t <sub>jtkldz</sub> t <sub>jtkloz</sub>	3 3	19 9	ns	5, 6

#### Notes:

- All outputs are measured from the midpoint voltage of the falling/rising edge of t<sub>TCLK</sub> to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 15). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
- 2. The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>JTDVKH</sub> symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t<sub>JTG</sub> clock reference (K) going to the high (H) state or setup time. Also, t<sub>JTDXKH</sub> symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t<sub>JTG</sub> clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).</sub>
- 3. TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.
- 4. Non-JTAG signal input timing with respect to t<sub>TCLK</sub>.
- 5. Non-JTAG signal output timing with respect to t<sub>TCLK</sub>.
- 6. Guaranteed by design.

Figure 15 provides the AC test load for TDO and the boundary-scan outputs.



Figure 44. AC Test Load for the JTAG Interface

Figure 45 provides the JTAG clock input timing diagram.



VM = Midpoint Voltage (OVDD/2)

#### Figure 45. JTAG Clock Input Timing Diagram

Figure 46 provides the  $\overline{\text{TRST}}$  timing diagram.





Figure 47 provides the boundary-scan timing diagram.



VM = Midpoint Voltage (OV<sub>DD</sub>/2)

Figure 47. Boundary-Scan Timing Diagram

## **3 Hardware Design Considerations**

This section provides electrical and thermal design recommendations for successful application of the MPC8610.

### 3.1 System Clocking

This section describes the PLL configuration of the MPC8610. Note that the platform clock is identical to the internal MPX bus clock.

This device includes six PLLs, as follows:

- 1. The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 3.1.2, "Platform/MPX to SYSCLK PLL Ratio."
- The e600 core PLL generates the core clock from the platform clock. The frequency ratio between the e600 core clock and the platform clock is selected using the e600 PLL ratio configuration bits as described in Section 3.1.3, "e600 Core to MPX/Platform Clock PLL Ratio."
- 3. The PCI PLL generates the clocking for the PCI bus
- 4. Each of the two SerDes blocks has a PLL.



### 3.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 53. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The TRST signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the Power Architecture technology. The device requires TRST to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the TRST signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying TRST to HRESET is not practical.

The COP function of these processors allows a remote computer system (typically a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP port connects primarily through the JTAG interface of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert HRESET or TRST in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 52 allows the COP port to independently assert  $\overline{\text{HRESET}}$  or  $\overline{\text{TRST}}$ , while ensuring that the target can drive  $\overline{\text{HRESET}}$  as well.

The COP interface has a standard header, shown in Figure 52, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header shown in Figure 53; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 53 is common to all known emulators.

### 3.9.1 Termination of Unused Signals

If the JTAG interface and COP header will not be used, Freescale recommends the following connections:

- TRST should be tied to HRESET through a 0-k $\Omega$  isolation resistor so that it is asserted when the system reset signal (HRESET) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 53. If this is not possible, the isolation resistor will allow future access to TRST in case a JTAG interface may need to be wired onto the system in future debug situations.
- Tie TCK to  $OV_{DD}$  through a 10-k $\Omega$  resistor. This will prevent TCK from changing state and reading incorrect data into the device.
- No connection is required for TDI, TMS, or TDO.



### 3.11 Guidelines for PCI Interface Termination

PCI termination if PCI is not used at all.

Option 1

- If PCI arbiter is enabled during POR,
  - All AD pins will be driven to the stable states after POR. Therefore, all ADs pins can be floating. This includes PCI\_AD[31:0], PCI\_C/BE[3:0], and PCI\_PAR signals.
  - All PCI control pins can be grouped together and tied to  $OV_{DD}$  through a single 10-k $\Omega$  resistor.
  - It is optional to disable PCI block through DEVDISR register after POR reset.

Option 2

- If PCI arbiter is disabled during POR,
  - All AD pins will be in the input state. Therefore, all ADs pins need to be grouped together and tied to  $OV_{DD}$  through a single (or multiple) 10-k $\Omega$  resistor(s)
  - All PCI control pins can be grouped together and tied to  $OV_{DD}$  through a single 10-k $\Omega$  resistor
  - It is optional to disable PCI block through DEVDISR register after POR reset.

### 3.12 Thermal

This section describes the thermal specifications of the MPC8610.

### 3.12.1 Thermal Characteristics

Table 62 provides the package thermal characteristics for the MPC8610.

Table dell'i dellago internal enalacionettee
--

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient thermal resistance, natural convection, single-layer (1s) board	R <sub>θJA</sub>	24	°C/W	1
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	$R_{ extsf{ heta}JA}$	18	°C/W	1
Junction-to-ambient thermal resistance, 200 ft/min airflow, single-layer (1s) board	R <sub>θJMA</sub>	18	°C/W	1
Junction-to-ambient thermal resistance, 200 ft/min airflow, four-layer (2s2p) board	R <sub>θJMA</sub>	15	°C/W	1
Junction-to-board thermal resistance	$R_{ heta JB}$	10	°C/W	2
Junction-to-case thermal resistance	R <sub>θJC</sub>	<0.1	°C/W	3

Notes:

- 1. Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
- 2. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
- 3. Junction-to-case resistance is less than 0.1°C/W because the silicon die is the top of the packaging case..

### 3.12.2 Thermal Management Information

This section provides thermal management information for the flip-chip, plastic ball-grid array (FC\_PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The MPC8610 implements several features designed to assist with thermal management, including the temperature diode. The temperature diode allows an external device to monitor the die temperature in order to detect excessive temperature conditions and alert the system; see Section 3.12.2.5, "Temperature Diode," for more information.



Often, heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 54). Therefore, synthetic grease offers the best thermal performance, considering the low interface pressure, and is recommended. Of course, the selection of any thermal interface material depends on many factors—thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, and so on.



Figure 56. Thermal Performance of Select Thermal Interface Material

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based on high conductivity and mechanical strength to meet equipment shock/vibration requirements. There are several commercially available thermal interfaces and adhesive materials provided by the following vendors:

The Bergquist Company 18930 West 78 <sup>th</sup> St.	800-347-4572
Chanhassen, MN 55317	
Internet: www.bergquistcompany.com	
Chomerics, Inc.	781-935-4850
77 Dragon Ct.	
Woburn, MA 01801	
Internet: www.chomerics.com	
Dow-Corning Corporation	800-248-2481
Corporate Center	
PO Box 994	
Midland, MI 48686-0994	
Internet: www.dowcorning.com	
Shin-Etsu MicroSi, Inc.	888-642-7674
10028 S. 51st St.	
Phoenix, AZ 85044	
Internet: www.microsi.com	



Product Documentation

# 6 **Product Documentation**

The following documents are required for a complete description of the device and are needed to design properly with the part.

- MPC8610 Integrated Host Processor Reference Manual (document number: MPC8610RM)
- e600 PowerPC Core Reference Manual (document number: E600CORERM)

# 7 Revision History

Table 65 summarizes revisions to this document.

#### Table 65. Revision History

Rev. No.	Date	Substantive Change(s)
2	1/2009	<ul> <li>Updated Table of Contents</li> <li>Removed subheading Section 1.1. pin assignments.</li> <li>Promoted section 4.3, "Ordering Information," and associated subsections to Section 4, "Ordering Information." Renumbered subsequent sections and subsections accordingly.</li> </ul>
1	01/2009	<ul> <li>Updated Table of Contents</li> <li>Removed Serial Rapid IO from Section 2.4.4, "Platform Frequency Requirements for PCI-Express" because SRIO is not available on MPC8610.</li> <li>Removed note in Table 21 and Table 22 that states "Minimum DDR2 frequency is 400 MHz."</li> <li>In Table 31, removed rows for t<sub>i2cr</sub> and t<sub>i2CF</sub> Added row for Cb.</li> <li>Replaced 1067 with 1066 in Table 63.</li> <li>Replaced CBGA with PBGA in Section 5.1, "Package Parameters for the MPC8610."</li> </ul>
0	10/2008	Initial release.



THIS PAGE INTENTIONALLY BLANK