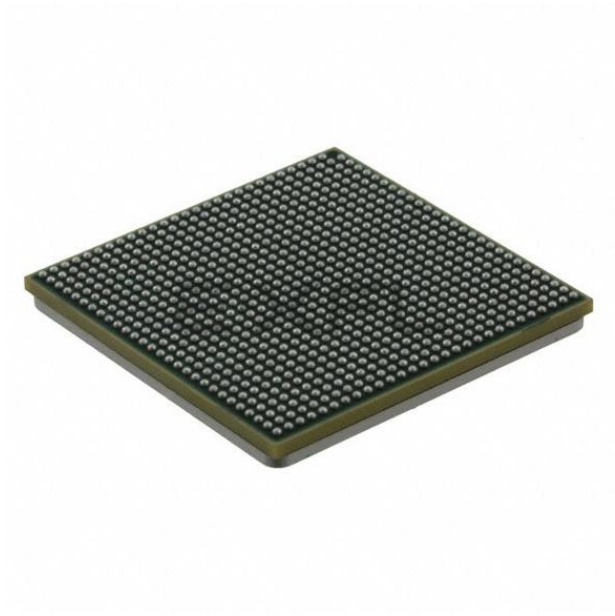

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e600
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.066GHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	DIU, LCD
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8610tvt1066jb

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Table 4. Output Drive Capability (continued)

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus	25 35	BV_{DD} = 3.3 V BV_{DD} = 2.5 V	2
	45 (default) 45 (default) 125	BV_{DD} = 3.3 V BV_{DD} = 2.5 V BV_{DD} = 1.8 V	
PCI, DUART, DMA, interrupts, system control and clocking, debug, test, JTAG, power management, and miscellaneous I/O voltage	45	OV_{DD} = 3.3 V	
I^2C	150	OV_{DD} = 3.3 V	
PCI Express	100	XV_{DD} = 1.0 V	3

Notes:
1. See the DDR control driver registers in the *MPC8610 Integrated Host Processor Reference Manual,* for more information.
2. See the POR impedance control register in the *MPC8610 Integrated Host Processor Reference Manual,* for more information about local bus signals and their drive strength programmability.
3. See Section 1, "Pin Assignments and Reset States," for details on resistor requirements for the calibration of SD*n*_IMP_CAL_TX and SD*n*_IMP_CAL_RX transmit and receive signals.
4. Stub series terminated logic (SSTL-25) type pins.
5. Stub series terminated logic (SSTL-18) type pins.
6. The drive strength of the DDR interface in half strength mode is at T_j = 105°C and at GV_{DD} (min).

2.2 Power Sequencing

The MPC8610 requires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows:

The chronological order of power up is:

1. OV_{DD}, BV_{DD}
2. V_{DD}_PLAT, AV_{DD}_PLAT, V_{DD}_Core, AV_{DD}_Core, AV_{DD}_PCI, S*n*V_{DD}, X*n*V_{DD}, SD*n*AV_{DD} (this rail must reach 90% of its value before the rail for GV_{DD} and MV_{REF} reaches 10% of its value)
3. GV_{DD}, MV_{REF}
4. SYSCLK

The order of power down is as follows:

1. SYSCLK
2. GV_{DD}, MV_{REF}
3. V_{DD}_PLAT, AV_{DD}_PLAT, V_{DD}_Core, AV_{DD}_Core, AV_{DD}_PCI, S*n*V_{DD}, X*n*V_{DD}, SD*n*AV_{DD}
4. O_{DD}, BV_{DD}

NOTE

AV_{DD} type supplies should be delayed with respect to their source supplies by the RC time constant of the PLL filter circuit described in Section 3.2, "Power Supply Design and Sequencing."

2.6.1 DDR SDRAM DC Electrical Characteristics

Table 14 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8610 when GV_{DD}(typ) = 1.8 V.

Table 14. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.71	1.89	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.125	GV_{DD} + 0.3	V	
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.125	V	
Output leakage current	I_{OZ}	–50	50	µA	4
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA	
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

Table 15 provides the DDR capacitance when GV_{DD}(typ) = 1.8 V.

Table 15. DDR2 SDRAM Capacitance for GV_{DD}(typ)=1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

Table 16 provides the recommended operating conditions for the DDR SDRAM component(s) when GV_{DD}(typ) = 2.5 V.

Table 16. DDR SDRAM DC Electrical Characteristics for GV_{DD} (typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.15	GV_{DD} + 0.3	V	
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.15	V	
Output leakage current	I_{OZ}	–50	50	µA	4

2.6.2.2 DDR SDRAM Output AC Timing Specifications

Table 22. DDR SDRAM Output AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MCK[n] cycle time, MCK[n]/$\overline{\text{MCK}}$[n] crossing	t_{MCK}	3	10	ns	2
MCK duty cycle	t_{MCKH}/t_{MCK}			%	
533 MHz		47	53		8
400 MHz		47	53		8
333 MHz		47	53		
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		
333 MHz		2.40	—		
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		
333 MHz		2.40	—		
$\overline{\text{MCS}}$[n] output setup with respect to MCK	t_{DDKHCS}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		
333 MHz		2.40	—		
$\overline{\text{MCS}}$[n] output hold with respect to MCK	t_{DDKHCX}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		
333 MHz		2.40	—		
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
533 MHz		590	—		7
400 MHz		700	—		
333 MHz		900	—		
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
533 MHz		590	—		7
400 MHz		700	—		
333 MHz		900	—		
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6

2.10 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8610.

2.10.1 DUART DC Electrical Characteristics

Table 32 provides the DC electrical characteristics for the DUART interface.

Table 32. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	– 0.3	0.8	V
Input current (V_{IN}[1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = mn, I_{OH} = –100 μA)	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 μA)	V_{OL}	—	0.2	V

Note:
1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2 and Table 3.

2.10.2 DUART AC Electrical Specifications

Table 33 provides the AC timing parameters for the DUART interface.

Table 33. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	Platform clock/1,048,576	baud	1
Maximum baud rate	Platform clock/16	baud	1, 2
Oversample rate	16	—	1, 3

Notes:
1. Guaranteed by design.
2. Actual attainable baud rate will be limited by the latency of interrupt processing.
3. The middle of a start bit is detected as the 8^{th} sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

2.11 Fast/Serial Infrared Interfaces (FIRI/SIRI)

The fast/serial infrared interfaces (FIRI/SIRI) implements asynchronous infrared protocols (FIR, MIR, SIR) that are defined by IrDA (Infrared Data Association). Refer to http://www.IrDA.org for details on FIR and SIR protocols.

2.12 Synchronous Serial Interface (SSI)

This section describes the DC and AC electrical specifications for the SSI interface of the MPC8610.

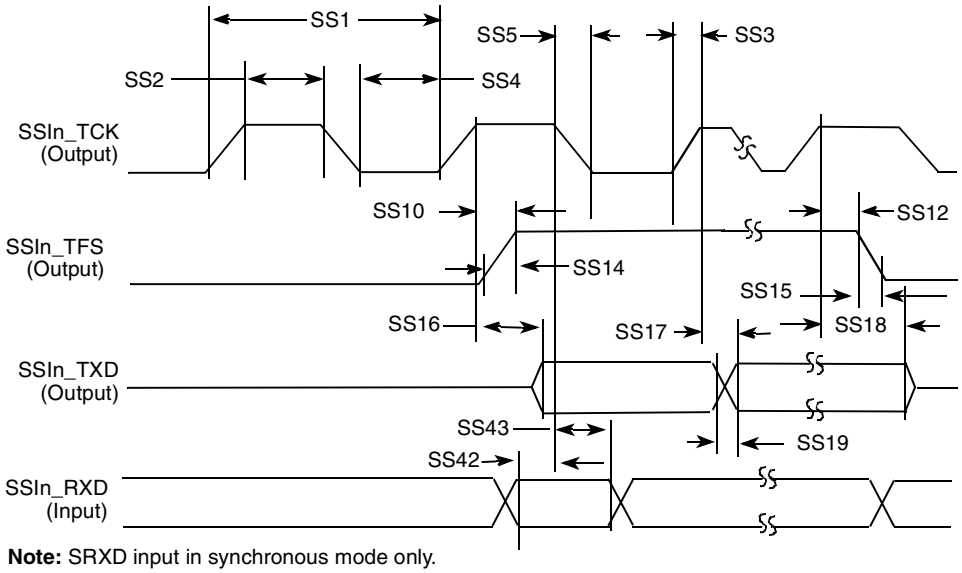
2.12.1 SSI DC Electrical Characteristics

Table 34 provides SSI DC electrical characteristics.

Table 35. SSI Transmitter with Internal Clock Timing Parameters (continued)

Parameter	Symbol	Min	Max	Unit
SRXD hold after (Tx) CK falling	SS43	0	—	ns
Loading	SS52	—	25	pF

Figure 17 provides the SSI transmitter timing with internal clock.



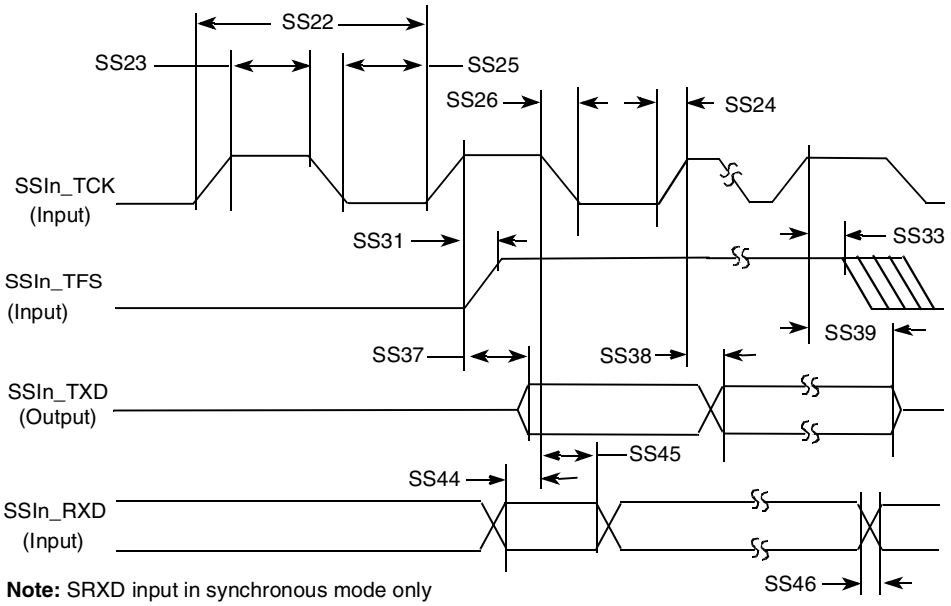
Note: SRXD input in synchronous mode only.

Figure 17. SSI Transmitter with Internal Clock Timing Diagram

Table 37. SSI Transmitter with External Clock Timing Parameters (continued)

Parameter	Symbol	Min	Max	Unit
(Tx/Rx) CK clock low period	SS25	36.0	—	ns
(Tx/Rx) CK clock fall time	SS26	—	6.0	ns
(Tx) CK high to FS high	SS31	–10.0	15.0	ns
(Tx) CK high to FS low	SS33	10.0	—	ns
(Tx) CK high to STXD valid from high impedance	SS37	—	15.0	ns
(Tx) CK high to STXD high/low	SS38	—	15.0	ns
(Tx) CK high to STXD high impedance	SS39	—	15.0	ns
Synchronous External Clock Operation				
SRXD setup before (Tx) CK falling	SS44	10.0	—	ns
SRXD hold after (Tx) CK falling	SS45	2.0	—	ns
SRXD rise/fall time	SS46	—	6.0	ns

Figure 19 provides the SSI transmitter timing with external clock.



Note: SRXD input in synchronous mode only

Figure 19. SSI Transmitter with External Clock Timing Diagram

2.12.2.4 SSI Receiver Timing with External Clock

Table 38 provides the receiver timing parameters with external clock.

Table 38. SSI Receiver with External Clock Timing Parameters

Parameter	Symbol	Min	Max	Unit
External Clock Operation				
(Tx/Rx) CK clock period	SS22	81.4	—	ns
(Tx/Rx) CK clock high period	SS23	36.0	—	ns
(Tx/Rx) CK clock rise time	SS24	—	6.0	ns
(Tx/Rx) CK clock low period	SS25	36.0	—	ns
(Tx/Rx) CK clock fall time	SS26	—	6.0	ns
(Rx) CK high to FS high	SS32	–10.0	15.0	ns
(Rx) CK high to FS low	SS34	10.0	—	ns
(Tx/Rx) external FS rise time	SS35	—	6.0	ns
(Tx/Rx) external FS fall time	SS36	—	6.0	ns
SRXD setup time before (Rx) CK low	SS40	10.0	—	ns
SRXD hold time after (Rx) CK low	SS41	2.0	—	ns

Figure 20 provides the SSI receiver timing with external clock.

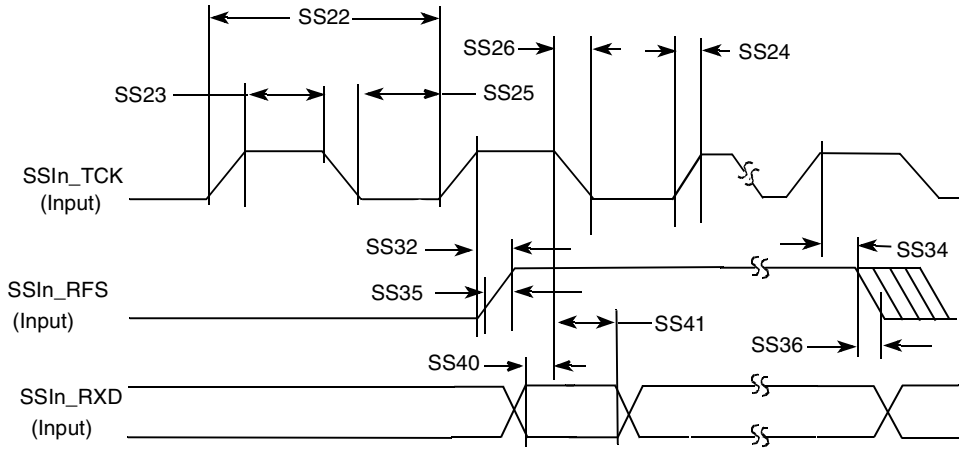


Figure 20. SSI Receiver with External Clock Timing Diagram

2.13 Global Timer Module

This section describes the DC and AC electrical specifications for the global timer module (GTM) of the MPC8610.

2.13.1 GTM DC Electrical Characteristics

Table 39 provides the DC electrical characteristics for the MPC8610 global timer module pins, including GTM*n*_TIN*n*, GTM*n*_$\overline{\text{TOUT}}$*n*, GTM*n*_$\overline{\text{TGATE}}$*n*, and RTC.

Table 39. GTM DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN}[1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –100 μA)	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 μA)	V_{OL}	—	0.2	V

Note:
1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2 and Table 3.

2.13.2 GTM AC Timing Specifications

Table 40 provides the GTM input and output AC timing specifications.

Table 40. GTM Input and Output AC Timing Specification[1]

Characteristic	Symbol[2]	Min	Unit	Notes
GTM inputs—minimum pulse width	t_{GTIWID}	7.5	ns	3
GTM outputs—minimum pulse width	t_{GTOWID}	12	ns	

Notes:
1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by external synchronous logic. Timer inputs are required to be valid for at least t_{GTIWID} ns to ensure proper operation.
3. The minimum pulse width is a function of the MPX/platform clock. The minimum pulse width must be greater than or equal to 4 times the MPX/platform clock period.

Figure 21 provides the AC test load for the GTM.

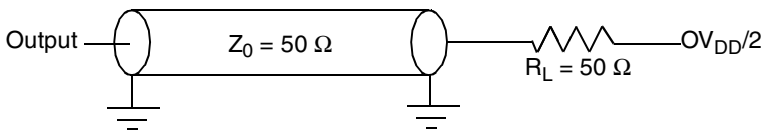


Figure 21. GTM AC Test Load

2.15 Serial Peripheral Interface (SPI)

This section describes the DC and AC electrical specifications for the SPI interface of the MPC8610.

2.15.1 SPI DC Electrical Characteristics

Table 43 provides the SPI DC electrical characteristics.

Table 43. SPI DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	– 0.3	0.8	V
Input current (V_{IN}[1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = mn, I_{OH} = –100 μA)	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 μA)	V_{OL}	—	0.2	V

Note:
1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2 and Table 3.

2.15.2 SPI AC Timing Specifications

Table 44 provides the SPI input and output AC timing specifications.

Table 44. SPI AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
SPI outputs valid—master mode (internal clock) delay	t_{NIKHOV}		1	ns
SPI outputs hold—master mode (internal clock) delay	t_{NIKHOX}	-0.2		ns
SPI outputs valid—slave mode (external clock) delay	t_{NEKHOV}		8	ns
SPI outputs hold—slave mode (external clock) delay	t_{NEKHOX}	2		ns
SPI inputs—master mode (internal clock input setup time	t_{NIIVKH}	4		ns
SPI inputs—master mode (internal clock input hold time	t_{NIIXKH}	0		ns
SPI inputs—slave mode (external clock) input setup time	t_{NEIVKH}	4		ns
SPI inputs—slave mode (external clock) input hold time	t_{NEIXKH}	2		ns

Notes:
1. Output specifications are measured from the 50 percent level of the rising edge of CLKIN to the 50 percent level of the signal. Timings are measured at the pin.
2. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).

of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX\text{-}DIFFp\text{-}p} = 2 * |V_{OD}|$.

6. Differential waveform

   The differential waveform is constructed by subtracting the inverting signal ($\overline{SDn\_TX}$, for example) from the noninverting signal (SD*n*_TX, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 38 as an example for differential waveform.

7. Common mode voltage, V_{cm}

   The common mode voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = (V_{SDn\_TX} + V_{\overline{SDn\_TX}})/2 = (A + B)/2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It's also referred as the DC offset in some occasion.

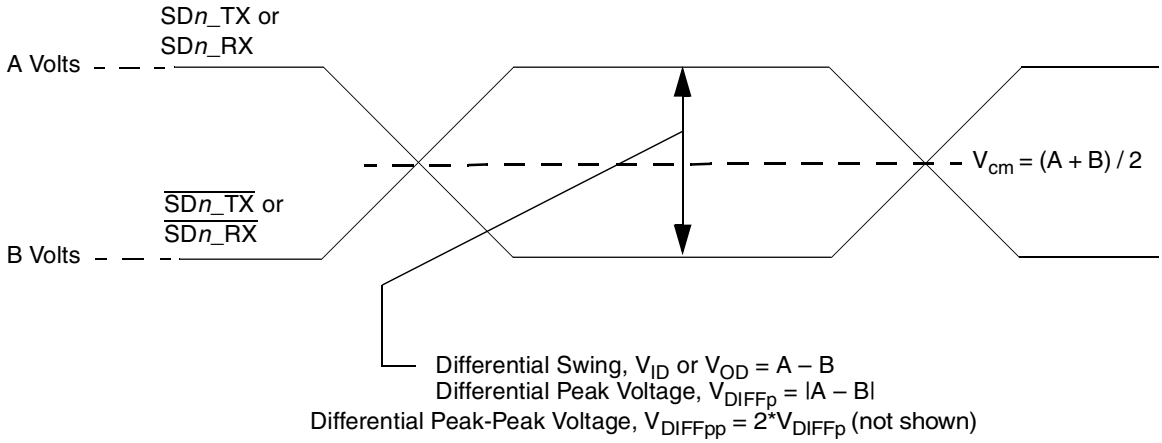


Figure 29. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{TD}$, has a swing that goes between 2.5 and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{TD}$) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV, in other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp\text{-}p}$) is 1000 mV p-p.

2.17.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD*n*_REF_CLK and $\overline{SDn\_REF\_CLK}$ for PCI Express.

The following sections describe the SerDes reference clock requirements and some application information.

2.17.2.1 SerDes Reference Clock Receiver Characteristics

Figure 30 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for XnV_{DD} are specified in Table 2 and Table 3.

2.17.2.3 Interfacing With Other Differential Signaling Levels

- With on-chip termination to SGND, the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC-coupled.
- Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

NOTE

Figure 34 to Figure 37 are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the MPC8610 SerDes reference clock receiver requirement provided in this document.

Figure 34 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with MPC8610 SerDes reference clock input's DC requirement.

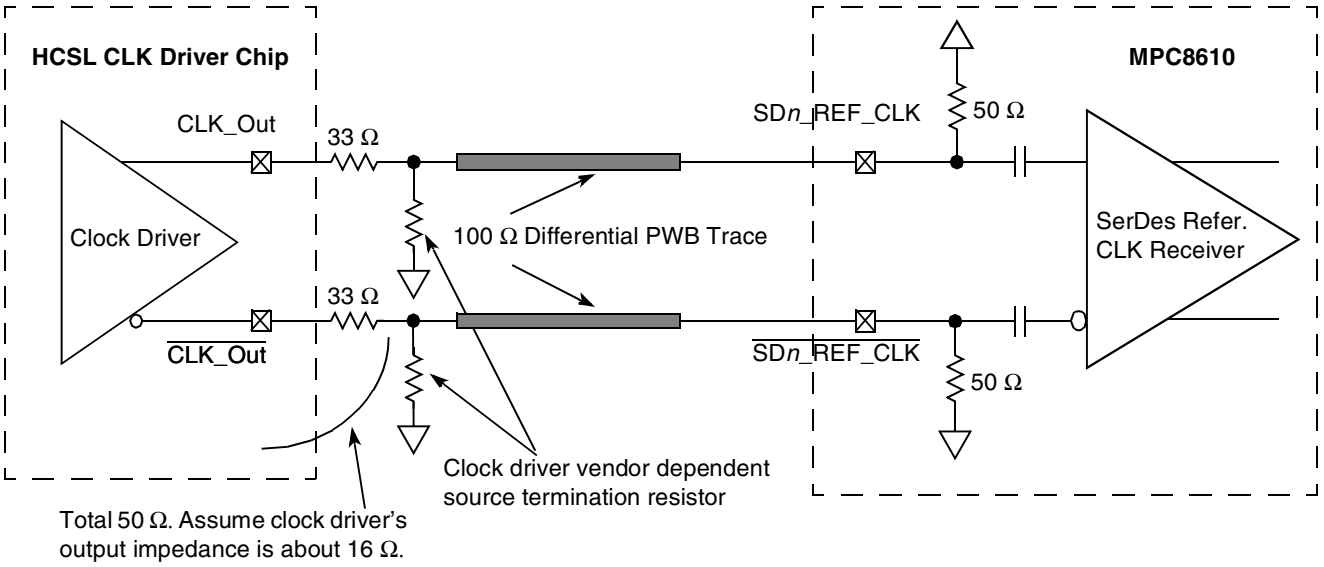


Figure 34. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

Figure 35 shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the MPC8610 SerDes reference clock input's allowed range (100 to 400 mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

2.17.3 SerDes Transmitter and Receiver Reference Circuits

Figure 40 shows the reference circuits for SerDes data lane's transmitter and receiver.

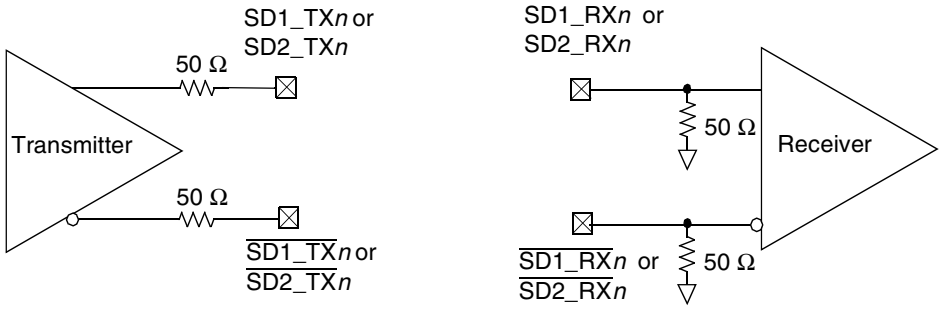


Figure 40. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express) in this document based on the application usage:"

- Section 2.18, "PCI Express"

Note that external AC Coupling capacitor is required for the above serial transmission protocols with the capacitor value defined in specification of each protocol section.

2.18 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the MPC8610.

2.18.1 DC Requirements for PCI Express SD*n*_REF_CLK and SD*n*_REF_CLK

For more information, see Section 2.17.2, "SerDes Reference Clocks."

2.18.2 AC Requirements for PCI Express SerDes Clocks

Table 48 lists AC requirements.

Table 48. SD*n*_REF_CLK and SD*n*_REF_CLK AC Requirements

Symbol	Parameter Description	Min	Typ	Max	Units
t_{REF}	REFCLK cycle time	—	10	—	ns
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–50	—	50	ps

2.18.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

Table 50. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$L_{TX-SKEW}$	Total skew			20	ns	Skew across all lanes on a link. This includes variation in the length of SKP ordered set (e.g., COM and one to five symbols) at the RX as well as any delay differences arising from the interconnect itself.

Notes:

1.)No test load is necessarily associated with this value.

2.)Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 43 should be used as the RX device when taking measurements (also refer to the receiver compliance eye diagram shown in Figure 42). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.

3.)A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.

4.)The receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D– line biased to –300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D– line (that is, as measured by a Vector Network Analyzer with 50-Ω probes—see Figure 43). Note that the series capacitors CTX is optional for the return loss measurement.

5.)Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.

6.)The RX DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit will not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.

7.)It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

2.18.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 42 is specified using the passive compliance/test measurement load (see Figure 43) in place of any real PCI Express RX component.

Note: In general, the minimum receiver eye diagram measured with the compliance/test measurement load (see Figure 43) will be larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum receiver eye diagram (shown in Figure 42) expected at the input receiver based on some adequate combination of system simulations and the return loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (i.e., as measured by a vector network analyzer with 50-Ω probes—see Figure 43). Note that the series capacitors, CTX, are optional for the return loss measurement.

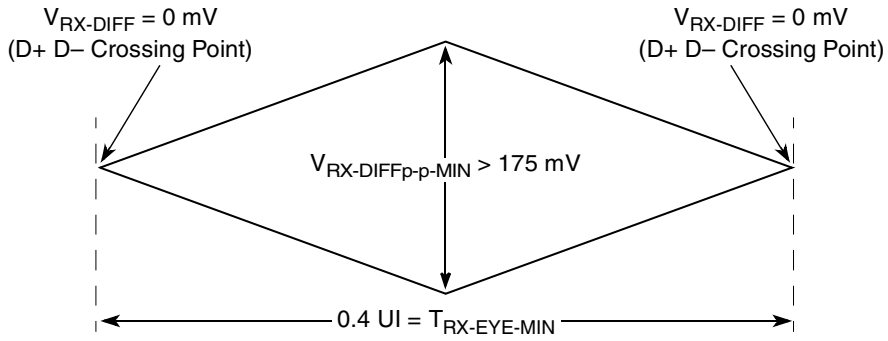


Figure 42. Minimum Receiver Eye Timing and Voltage Compliance Specification

2.18.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 43.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

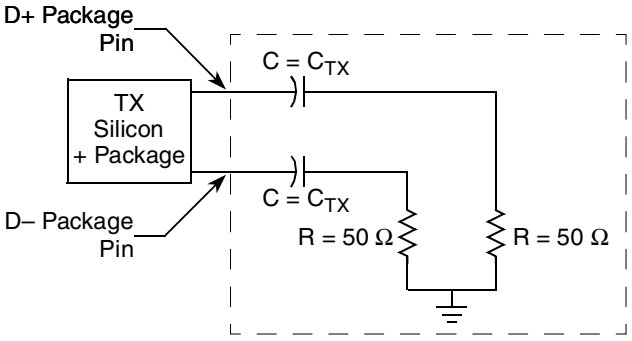


Figure 43. Compliance Test/Measurement Load

2.19 JTAG

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8610.

2.19.1 JTAG DC Electrical Characteristics

Table 51 provides the JTAG DC electrical characteristics for the JTAG interface.

3.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 53. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the Power Architecture technology. The device requires $\overline{\text{TRST}}$ to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP port connects primarily through the JTAG interface of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 52 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 52, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header shown in Figure 53; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 53 is common to all known emulators.

3.9.1 Termination of Unused Signals

If the JTAG interface and COP header will not be used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 53. If this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- Tie TCK to OV_{DD} through a 10-kΩ resistor. This will prevent TCK from changing state and reading incorrect data into the device.
- No connection is required for TDI, TMS, or TDO.

An approximate value of the ideality may be obtained by calibrating the device near the expected operating temperature.

Ideality factor is defined as the deviation from the ideal diode equation:

$$I_{fw} = I_s \left[e^{\frac{qV_f}{nKT}} - 1 \right]$$

Another useful equation is:

$$V_H - V_L = n\frac{KT}{q}\left[ln\frac{I_H}{I_L} \right]$$

Where:

I_{fw} = Forward current
I_s = Saturation current
V_d = Voltage at diode
V_f = Voltage forward biased
V_H = Diode voltage while I_H is flowing
V_L = Diode voltage while I_L is flowing
I_H = Larger diode bias current
I_L = Smaller diode bias current
q = Charge of electron (1.6×10^{-19} C)
n = Ideality factor (normally 1.0)
K = Boltzman's constant (1.38×10^{-23} Joules/K)
T = Temperature (Kelvins)

The ratio of I_H to I_L is usually selected to be 10:1. The above simplifies to the following:

$$V_H - V_L = 1.986 \times 10^{-4} \times nT$$

Solving for T, the equation becomes:

$$nT = \frac{V_H - V_L}{1.986 \times 10^{-4}}$$

4 Ordering Information

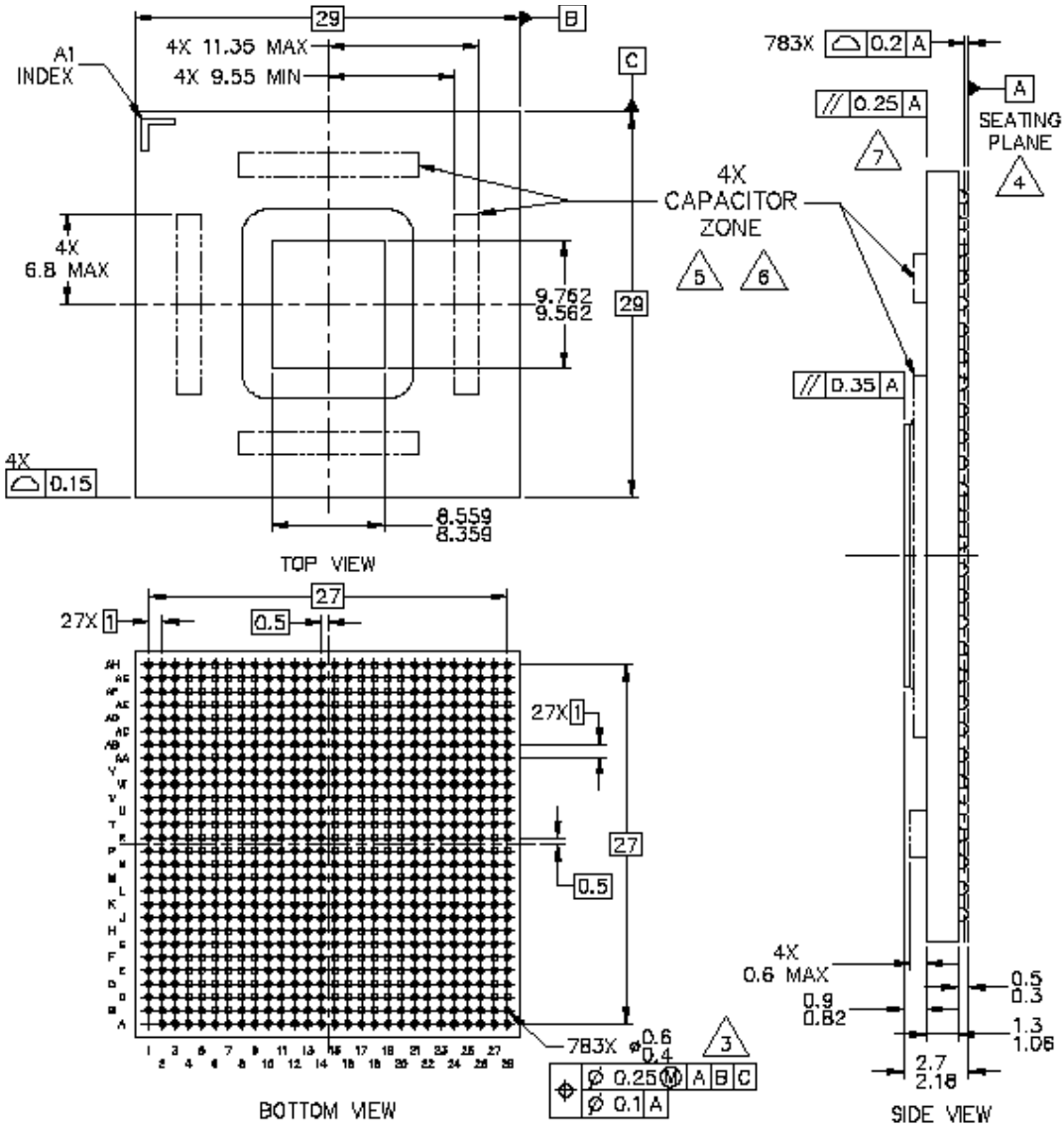
Ordering information for the parts fully covered by this specification document is provided in Section 4.1, "Part Numbers Fully Addressed by This Document."

4.1 Part Numbers Fully Addressed by This Document

Table 63 provides the Freescale part numbering nomenclature for the MPC8610. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

5.2 Mechanical Dimensions of the MPC8610 FC-PBGA

Figure 59 shows the mechanical dimensions and bottom surface nomenclature of the MPC8610 lead-free FC-PBGA.



Notes:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.
5. Capacitors may not be present on all devices.
6. Caution must be taken not to short capacitors or expose metal capacitor pads on package top.
7. All dimensions symmetrical about centerlines unless otherwise specified.

Figure 59. MPC8610 FC-PBGA Dimensions

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