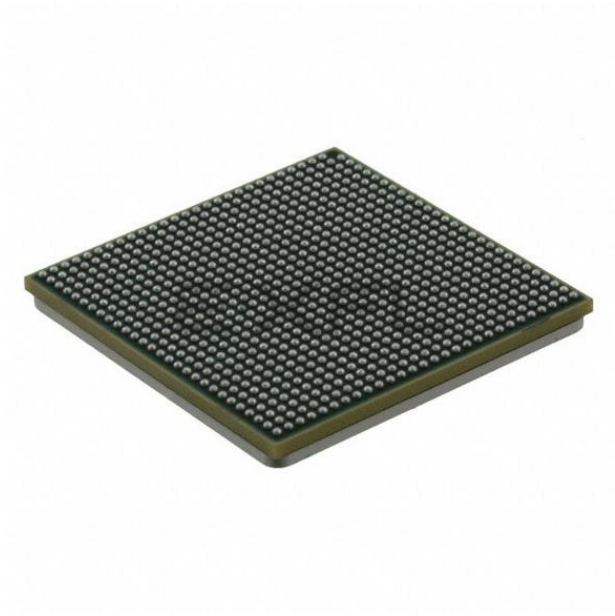

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e600
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.066GHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	DIU, LCD
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8610vt1066jb

Table 1. Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
LAD[0:31]	AA21, AA22, AA23, Y21, Y22, Y23, Y24, W23, W24, W25, V28, V27, V25, V23, V21, W22, U28, U26, U24, U22, U23, U20, U21, W20, V20, T24, T25, T27, T26, T21, T22, T23	I/O	BV_{DD}	20
LDP[0:3]/LA[6:9]	N28, M28, L28, P25	I/O	BV_{DD}	
LA10/SSI1_TXD	P19	O	BV_{DD}	20, 23
LA11/SSI1_TFS	M27	O	BV_{DD}	23
LA12/SSI1_TCK	U18	O	BV_{DD}	23
LA13/SSI1_RCK	P28	O	BV_{DD}	23
LA14/SSI1_RFS	R18	O	BV_{DD}	23
LA15/SSI1_RXD	R19	O	BV_{DD}	23
LA16/SSI2_TXD	R20	O	BV_{DD}	23
LA17/SSI2_TFS	M18	O	BV_{DD}	23
LA18/SSI2_TCK	N18	O	BV_{DD}	23
LA19/SSI2_RCK	N27	O	BV_{DD}	23
LA20/SSI2_RFS	P20	O	BV_{DD}	23
LA21/SSI2_RXD	P21	O	BV_{DD}	23
LA[22:31]	M19, M21, M22, M23, N23, N24, M26, N20, N21, N22	O	BV_{DD}	20
$\overline{\text{LCS}}$[0:4]	R24, R22, P23, P24, P27	O	BV_{DD}	21
$\overline{\text{LCS5}}$/$\overline{\text{DMA2\_DREQ0}}$	R23	O	BV_{DD}	21, 22, 23
$\overline{\text{LCS6}}$/$\overline{\text{DMA2\_DACK0}}$	N26	O	BV_{DD}	21, 23
$\overline{\text{LCS7}}$/$\overline{\text{DMA2\_DDONE0}}$	R26	O	BV_{DD}	21, 23
$\overline{\text{LWE0}}$/$\overline{\text{LFWE}}$/$\overline{\text{LBS0}}$	T19	O	BV_{DD}	20
$\overline{\text{LWE1}}$/$\overline{\text{LBS1}}$	T20	O	BV_{DD}	20
$\overline{\text{LWE2}}$/$\overline{\text{LBS2}}$	W19	O	BV_{DD}	20
$\overline{\text{LWE3}}$/$\overline{\text{LBS3}}$	T18	O	BV_{DD}	20
LBCTL	T28	O	BV_{DD}	20
LALE	R28	O	BV_{DD}	20
LGPL0/LFCLE	L19	O	BV_{DD}	20
LGPL1/LFALE	L20	O	BV_{DD}	20
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$	L21	O	BV_{DD}	20
LGPL3/$\overline{\text{LFWP}}$	L22	O	BV_{DD}	20
$\overline{\text{LGTA}}$/LFR$\overline{\text{B}}$/LGPL4/ LUPWAIT/LPBSE	L23	I/O	BV_{DD}	24

Table 1. Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{SD2\_REF\_CLK}}$	B18	I	$S2V_{DD}$	
SD2_PLL_TPD	D17	O	$X2V_{DD}$	9, 10
SD2_PLL_TPA	C17	Analog	$S2V_{DD}$	9, 11
SD2_IMP_CAL_TX	E21	Analog	$X2V_{DD}$	7
SD2_IMP_CAL_RX	B11	Analog	$S2V_{DD}$	8
System Control Signals[4]				
$\overline{\text{HRESET}}$	B23	I	OV_{DD}	
$\overline{\text{HRESET\_REQ}}$	J22	O	OV_{DD}	
$\overline{\text{SRESET}}$	A26	I	OV_{DD}	
$\overline{\text{CKSTP\_IN}}$	C27	I	OV_{DD}	
$\overline{\text{CKSTP\_OUT}}$	F24	O	OV_{DD}	21, 25
Power Management Signals[4]				
ASLEEP	B26	O	OV_{DD}	20
Debug Signals[4]				
TRIG_IN	K20	I	OV_{DD}	
TRIG_OUT/READY/ $\overline{\text{QUIESCE}}$	C28	O	OV_{DD}	14
MSRCID[0:4]	Y20, AB23, AB20, AB21, AC23	O	BV_{DD}	14, 20
MDVAL	AC20	O	BV_{DD}	20
CLK_OUT	G28	O	OV_{DD}	18
Test Signals[4]				
$\overline{\text{LSSD\_MODE}}$	G23	I	OV_{DD}	26
TEST_MODE[0:1]	K12, K10	I	OV_{DD}	26
JTAG Signals[4]				
TCK	D26	I	OV_{DD}	
TDI	B25	I	OV_{DD}	27
TDO	D27	O	OV_{DD}	18
TMS	C25	I	OV_{DD}	27
$\overline{\text{TRST}}$	A28	I	OV_{DD}	27
Additional Analog Signals				
TEMP_ANODE	C11	Thermal	—	
TEMP_CATHODE	C10	Thermal	—	
Special Connection Requirement Pins				

Table 4. Output Drive Capability (continued)

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus	25 35	BV_{DD} = 3.3 V BV_{DD} = 2.5 V	2
	45 (default) 45 (default) 125	BV_{DD} = 3.3 V BV_{DD} = 2.5 V BV_{DD} = 1.8 V	
PCI, DUART, DMA, interrupts, system control and clocking, debug, test, JTAG, power management, and miscellaneous I/O voltage	45	OV_{DD} = 3.3 V	
I^2C	150	OV_{DD} = 3.3 V	
PCI Express	100	XV_{DD} = 1.0 V	3

Notes:
1. See the DDR control driver registers in the *MPC8610 Integrated Host Processor Reference Manual,* for more information.
2. See the POR impedance control register in the *MPC8610 Integrated Host Processor Reference Manual,* for more information about local bus signals and their drive strength programmability.
3. See Section 1, "Pin Assignments and Reset States," for details on resistor requirements for the calibration of SD*n*_IMP_CAL_TX and SD*n*_IMP_CAL_RX transmit and receive signals.
4. Stub series terminated logic (SSTL-25) type pins.
5. Stub series terminated logic (SSTL-18) type pins.
6. The drive strength of the DDR interface in half strength mode is at T_j = 105°C and at GV_{DD} (min).

2.2 Power Sequencing

The MPC8610 requires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows:

The chronological order of power up is:

1. OV_{DD}, BV_{DD}
2. V_{DD}_PLAT, AV_{DD}_PLAT, V_{DD}_Core, AV_{DD}_Core, AV_{DD}_PCI, S*n*V_{DD}, X*n*V_{DD}, SD*n*AV_{DD} (this rail must reach 90% of its value before the rail for GV_{DD} and MV_{REF} reaches 10% of its value)
3. GV_{DD}, MV_{REF}
4. SYSCLK

The order of power down is as follows:

1. SYSCLK
2. GV_{DD}, MV_{REF}
3. V_{DD}_PLAT, AV_{DD}_PLAT, V_{DD}_Core, AV_{DD}_Core, AV_{DD}_PCI, S*n*V_{DD}, X*n*V_{DD}, SD*n*AV_{DD}
4. O_{DD}, BV_{DD}

NOTE

AV_{DD} type supplies should be delayed with respect to their source supplies by the RC time constant of the PLL filter circuit described in Section 3.2, "Power Supply Design and Sequencing."

2.3 Power Characteristics

The power dissipation for the MPC8610 device is shown in Table 5.

Table 5. MPC8610 Power Dissipation

Power Mode	Core/Platform Frequency (MHz)	V_{DD}_Core, V_{DD}_PLAT (V)	Junction Temperature (°C)	Power (Watts)	Notes
Typical	1333/533	1.025	65	10.7	1, 2
Thermal			105	12.1	1, 3
Maximum				16	1, 4
Typical	1066/533	1.00	65	8.4	1, 2
Thermal			105	9.8	1, 3
Maximum				13	1, 4
Typical	800/400	1.00	65	5.8	1, 2
Thermal			105	7.2	1, 3
Maximum				9.5	1, 4

Notes:

1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.
2. Typical power is an average value measured at the nominal recommended core voltage (V_{DD}_Core) and 65°C junction temperature (see Table 3) while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz with the core at 100% efficiency. This parameter is not 100% tested but periodically sampled.
3. Thermal power is the average power measured at nominal core voltage (V_{DD}_Core) and maximum operating junction temperature (see Table 3) while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz on the core and a typical workload on platform interfaces. This parameter is not 100% tested but periodically sampled.
4. Maximum power is the maximum power measured at nominal core voltage (V_{DD}_Core) and maximum operating junction temperature (see Table 3) while running a test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep all the execution units maximally busy on the core.

The estimated maximum power dissipation for individual power supplies of the MPC8610 is shown in Table 6.

Table 6. MPC8610 Individual Supply Maximum Power Dissipation[1]

Component Description	Supply Voltage (V)	Est. Power (Watts)	Notes
Core voltage supply	V_{DD}_Core = 1.025 V @ 1333 MHz	14.0	
	V_{DD}_Core = 1.00 V @ 1066 MHz	12.0	
Core PLL voltage supply	AV_{DD}_Core = 1.025 V @ 1333 MHz	0.0125	
	AV_{DD}_Core = 1.00 V @ 1066 MHz	0.0125	
Platform source supply	V_{DD}_PLAT = 1.025 V @ 1333 MHz	4.5	
	V_{DD}_PLAT = 1.00 V @ 1066 MHz	4.3	

SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ was designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock. For better results use a source without significant unintended modulation.

2.4.2 Real Time Clock Timing

The RTC input is sampled by the platform clock. The output of the sampling latch is then used as an input to the counters of the PIC. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than 2× the period of the platform clock. That is, minimum clock high time is $2 \times t_{MPX}$, and minimum clock low time is $2 \times t_{MPX}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

2.4.3 PCI/PCI-X Reference Clock Timing

When the PCI/PCI-X controller is configured for asynchronous operation, the reference clock for the PCI/PCI-X controller is not the SYSCLK input, but instead the PCI*n*_CLK. Table 11provides the PCI/PCI-X reference clock AC timing specifications for the MPC8610.

Table 11. PCI*n*_CLK AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
PCI*n*_CLK frequency	f_{PCICLK}	16	—	133	MHz	—
PCI*n*_CLK cycle time	t_{PCICLK}	7.5	—	60	ns	—
PCI*n*_CLK rise and fall time	t_{PCIKH}, t_{PCIKL}	0.6	1.0	2.1	ns	1, 2
PCI*n*_CLK duty cycle	$t_{PCIKHKL}/t_{PCICLK}$	40	—	60	%	2

Notes:
1. Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.
2. Timing is guaranteed by design and characterization.

2.4.4 Platform Frequency Requirements for PCI-Express

The MPX platform clock frequency must be considered for proper operation of the high-speed PCI Express interface as described below.

For proper PCI Express operation, the MPX clock frequency must be greater than or equal to:

$$\frac{\text{527 MHz x (PCI-Express link width)}}{\text{16 / (1 + cfg\_net2\_div)}}$$

Note that at MPX = 333 - 400 MHz, cfg_net2_div = 0 and at MPX > 400 MHz, cfg_net2_div = 1. Therefore, when operating PCI Express in x8 link width, the MPX platform frequency must be 333-400 MHz with cfg_net2_div = 0 or greater than or equal to 527 MHz with cfg_net2_div = 1.

Table 16. DDR SDRAM DC Electrical Characteristics for GV_{DD} (typ) = 2.5 V (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–16.2	—	mA	
Output low current (V_{OUT} = 0.35 V)	I_{OL}	16.2	—	mA	

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

Table 17 provides the DDR capacitance when GV_{DD} (typ)=2.5 V.

Table 17. DDR SDRAM Capacitance for GV_{DD} (typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

Table 18 provides the current draw characteristics for MV_{REF}.

Table 18. Current Draw Characteristics for MV_{REF}

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Current draw for MV_{REF}	I_{MVREF}	—	500	μA	1

Note:
1. The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.

2.6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR/DDR2 SDRAM interface.

2.6.2.1 DDR SDRAM Input AC Timing Specifications

Table 19 provides the input AC timing specifications for the DDR2 SDRAM when GV_{DD}(typ)=1.8 V.

Table 19. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.25	V
AC input high voltage	V_{IH}	MV_{REF} + 0.25	—	V

Table 27. DIU DC Electrical Characteristics (continued)

Parameter	Symbol	Min	Max	Unit
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 µA)	V_{OL}	—	0.2	V

Note:
1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2 and Table 3.

2.8.2 DIU AC Timing Specifications

Figure 12 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and the data. All parameters shown in the diagram are programmable. This timing diagram corresponds to positive polarity of the DIU_CLK_OUT signal and active-high polarity of the DIU_HSYNC, DIU_VSYNC, and DIU_DE signals. By default, all control signals and the display data are generated at the rising edge of the internal pixel clock, and the DIU_CLK_OUT output to drive the panel has the same polarity with the internal pixel clock. User can select the polarity of the DIU_HSYNC and DIU_VSYNC signal (via the SYN_POL register), whether active-high or active-low, the default is active-high. The DIU_DE signal is always active-high.

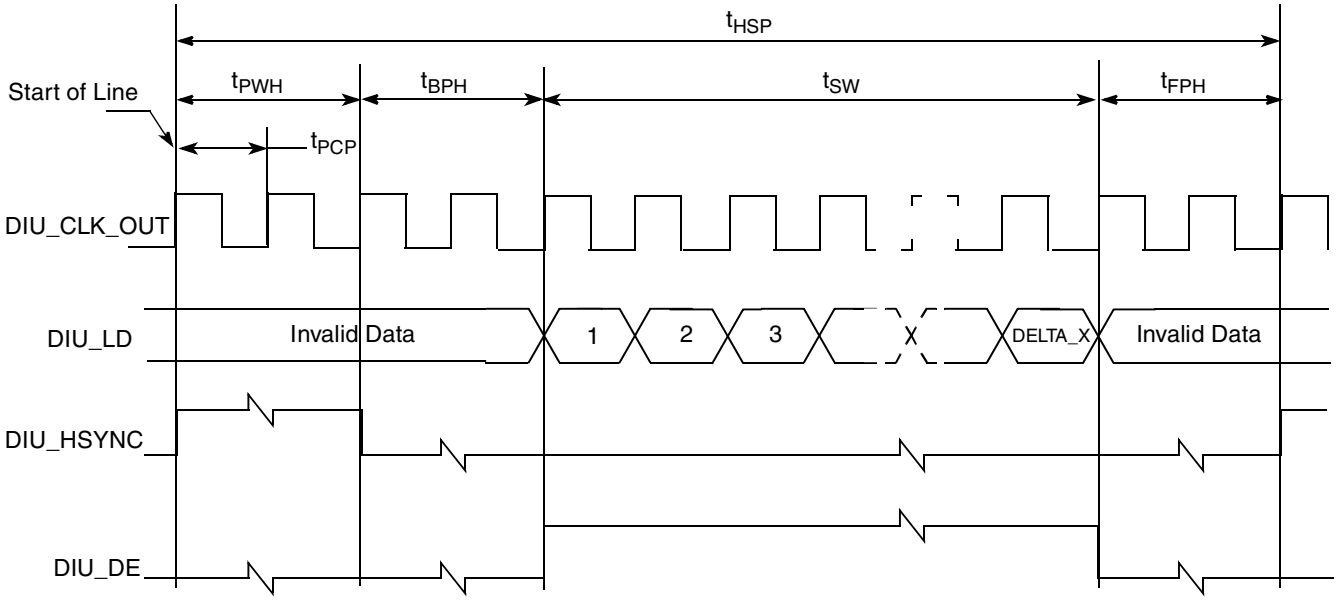


Figure 12. TFT DIU/LCD Interface Timing Diagram—Horizontal Sync Pulse

The DELTA_X and DELTA_Y parameters are programmed via the DISP_SIZE register. The PW_H, BP_H, and FP_H parameters are programmed via the HSYN_PARA register; and the PW_V, BP_V, and FP_V parameters are programmed via the VSYN_PARA register.

Figure 14 depicts the synchronous display interface timing for access level, and Table 29 lists the timing parameters.

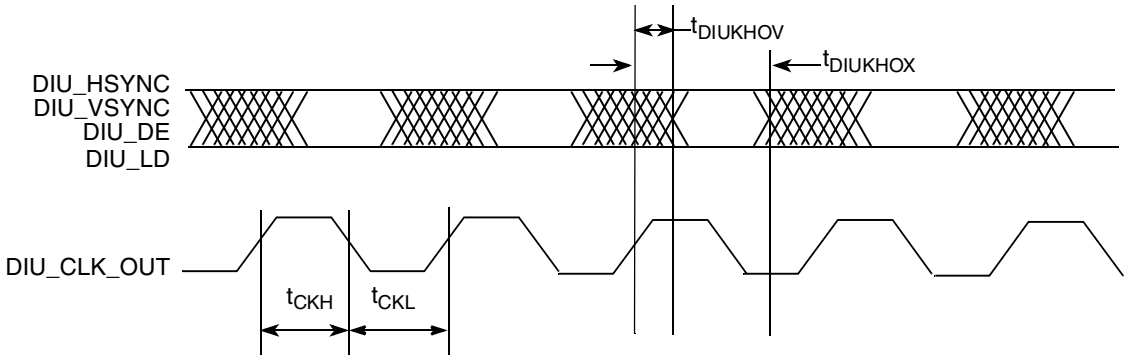


Figure 14. LCD Interface Timing Diagram—Access Level

NOTE

The DIU_OUT_CLK edge and phase delay is selectable via the Global Utilities CKDVDR register.

Table 29. LCD Interface Timing Parameters—Access Level

Parameter	Symbol	Min	Typ	Max	Unit
LCD interface pixel clock high time	t_{CKH}	$0.35 \times t_{PCP}$	$0.5 \times t_{PCP}$	$0.65 \times t_{PCP}$	ns
LCD interface pixel clock low time	t_{CKL}	$0.35 \times t_{PCP}$	$0.5 \times t_{PCP}$	$0.65 \times t_{PCP}$	ns
LCD interface pixel clock to ouput valid	$t_{DIUKHOV}$	—	—	2	ns
LCD interface output hold from pixel clock	$t_{DIUKHOX}$	$t_{PCP} - 2$	—	—	ns

2.9 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the MPC8610.

2.9.1 I²C DC Electrical Characteristics

Table 30 provides the DC electrical characteristics for the I²C interfaces.

Table 30. I²C DC Electrical Characteristics

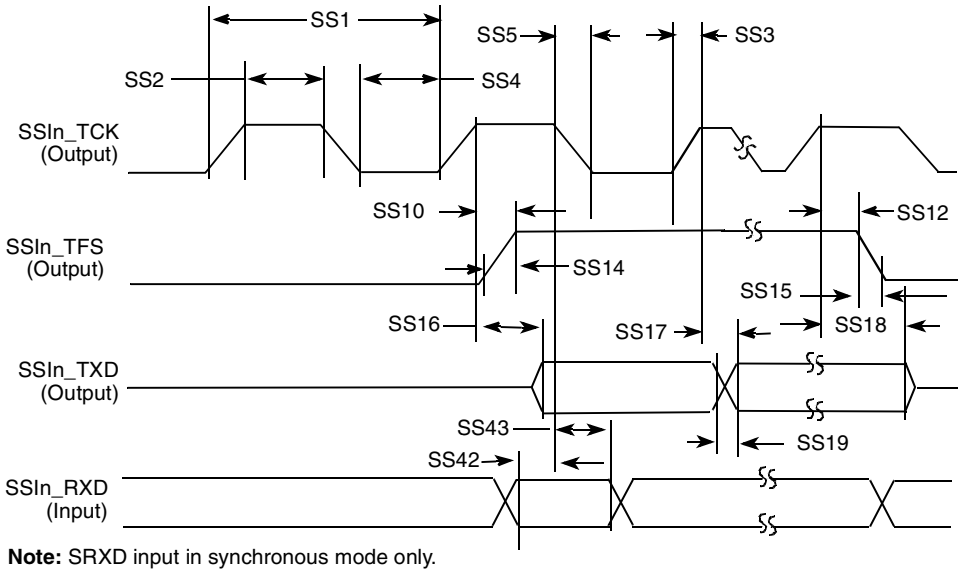
At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	2

Table 35. SSI Transmitter with Internal Clock Timing Parameters (continued)

Parameter	Symbol	Min	Max	Unit
SRXD hold after (Tx) CK falling	SS43	0	—	ns
Loading	SS52	—	25	pF

Figure 17 provides the SSI transmitter timing with internal clock.



Note: SRXD input in synchronous mode only.

Figure 17. SSI Transmitter with Internal Clock Timing Diagram

2.12.2.2 SSI Receiver Timing with Internal Clock

Table 36 provides the receiver timing parameters with internal clock.

Table 36. SSI Receiver with Internal Clock Timing Parameters

Parameter	Symbol	Min	Max	Unit
Internal Clock Operation				
(Tx/Rx) CK clock period	SS1	81.4	—	ns
(Tx/Rx) CK clock high period	SS2	36.0	—	ns
(Tx/Rx) CK clock rise time	SS3	—	6	ns
(Tx/Rx) CK clock low period	SS4	36.0	—	ns
(Tx/Rx) CK clock fall time	SS5	—	6	ns
(Rx) CK high to FS high	SS11	—	15.0	ns
(Rx) CK high to FS low	SS13	—	15.0	ns
SRXD setup time before (Rx) CK low	SS20	10.0	—	ns
SRXD hold time after (Rx) CK low	SS21	0	—	ns

Figure 18 provides the SSI receiver timing with internal clock.

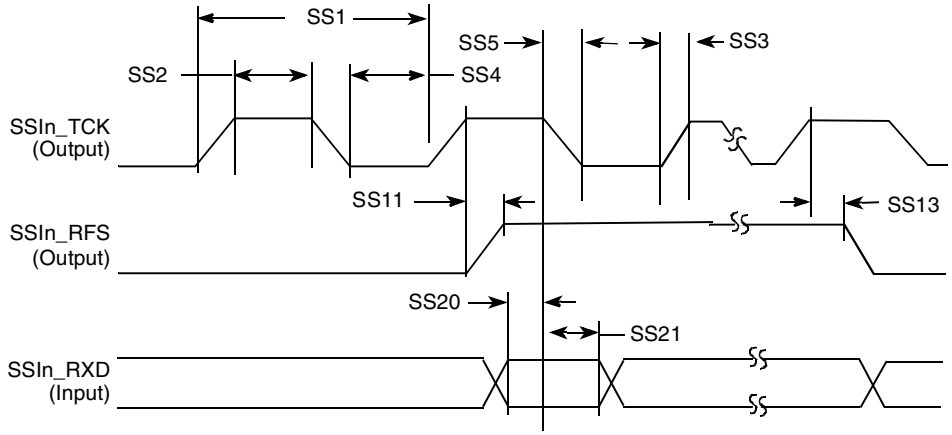


Figure 18. SSI Receiver with Internal Clock Timing Diagram

2.12.2.3 SSI Transmitter Timing with External Clock

Table 37 provides the transmitter timing parameters with external clock.

Table 37. SSI Transmitter with External Clock Timing Parameters

Parameter	Symbol	Min	Max	Unit
External Clock Operation				
(Tx/Rx) CK clock period	SS22	81.4	—	ns
(Tx/Rx) CK clock high period	SS23	36.0	—	ns
(Tx/Rx) CK clock rise time	SS24	—	6.0	ns

2.16 PCI Interface

This section describes the DC and AC electrical specifications for the PCI bus interface.

2.16.1 PCI DC Electrical Characteristics

Table 45 provides the DC electrical characteristics for the PCI interface.

Table 45. PCI DC Electrical Characteristics[1]

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN} [2] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –100 μA)	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 μA)	V_{OL}	—	0.2	V

Notes:
1. Ranges listed do not meet the full range of the DC specifications of the *PCI 2.2 Local Bus Specifications*.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2 and Table 3.

2.16.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus. Note that the SYSCLK signal is used as the PCI input clock. Table 46 provides the PCI AC timing specifications at 66 MHz.

Table 46. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol[1]	Min	Max	Unit	Notes
SYSCLK to output valid	t_{PCKHOV}	1.5	7.4	ns	2, 3, 12
SYSCLK to output high impedance	t_{PCKHOZ}	—	14	ns	2, 4, 11
Input setup to SYSCLK	t_{PCIVKH}	3.7	—	ns	2, 5, 10, 13
Input hold from SYSCLK	t_{PCIXKH}	0.8	—	ns	2, 5, 10, 14
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ [9] setup time	t_{PCRVRH}	$10 \times t_{SYS}$	—	clocks	6, 7, 11
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	7, 11

Figure 28 shows the PCI output AC timing conditions.

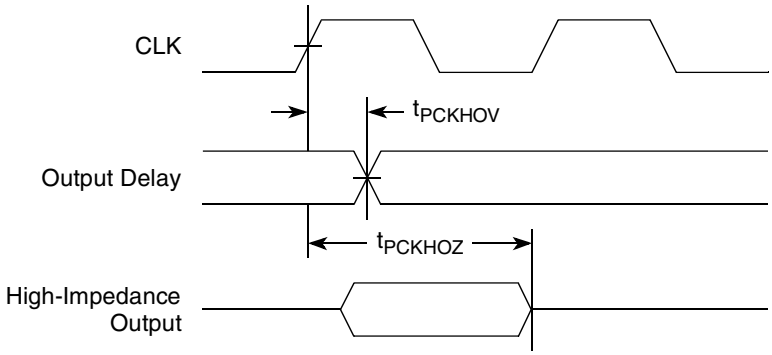


Figure 28. PCI Output AC Timing Measurement Condition

2.17 High-Speed Serial Interfaces (HSSI)

The MPC8610 features two Serializer/Deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. The SerDes1 interface is dedicated for PCI Express (x1/x2/x4) data transfers. The SerDes2 interface is dedicated for PCI Express (x1/x2/x4/x8) data transfers.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

2.17.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 29 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SD*n*_TX and $\overline{\text{SD}n\text{\_TX}}$) or a receiver input (SD*n*_RX and $\overline{\text{SD}n\text{\_RX}}$). Each signal swings between A volts and B volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. Single-ended swing

   The transmitter output signals and the receiver input signals SD*n*_TX, $\overline{\text{SD}n\text{\_TX}}$, SD*n*_RX, and $\overline{\text{SD}n\text{\_RX}}$ each have a peak-to-peak swing of A – B volts. This is also referred as each signal wire's single-ended swing.

2. Differential output voltage, V_{OD} (or differential output swing):

   The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SDn\_TX} - V_{\overline{SDn\_TX}}$. The V_{OD} value can be either positive or negative.

3. Differential input voltage, V_{ID} (or differential input swing):

   The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SDn\_RX} - V_{\overline{SDn\_RX}}$. The V_{ID} value can be either positive or negative.

4. Differential peak voltage, V_{DIFFp}

   The peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak voltage, $V_{DIFFp} = |A - B|$ volts.

5. Differential peak-to-peak, $V_{DIFFp-p}$

   Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to -(A – B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 * V_{DIFFp} = 2 * |(A - B)|$ volts, which is twice

2.17.2.3 Interfacing With Other Differential Signaling Levels

- With on-chip termination to SGND, the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC-coupled.
- Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

NOTE

Figure 34 to Figure 37 are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the MPC8610 SerDes reference clock receiver requirement provided in this document.

Figure 34 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with MPC8610 SerDes reference clock input's DC requirement.

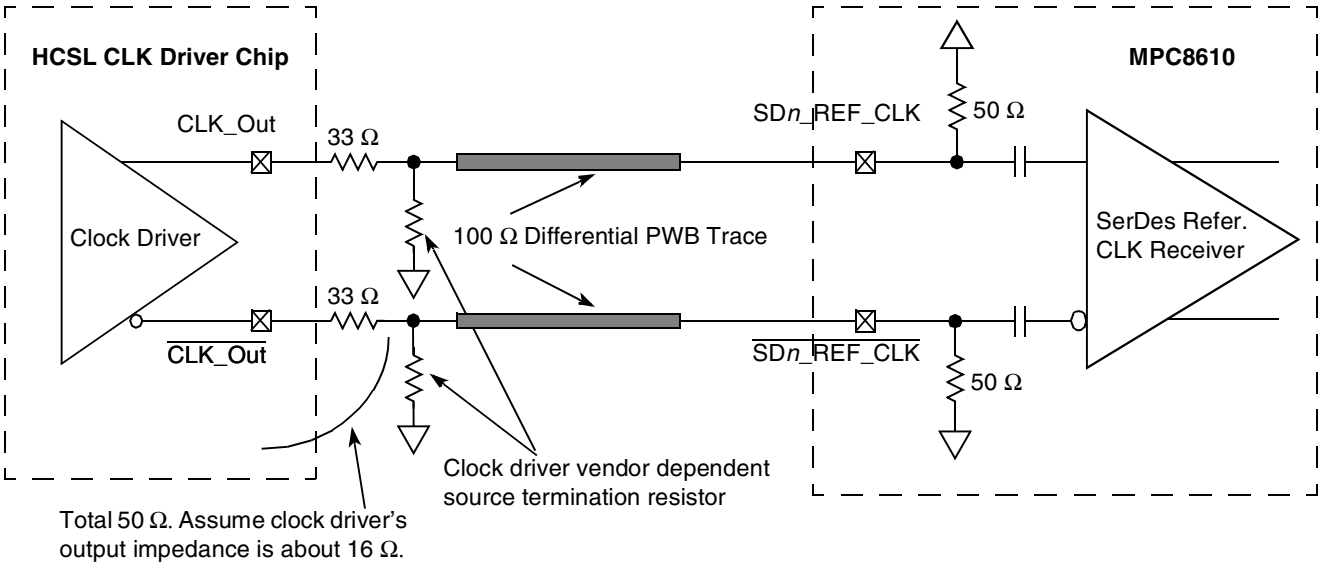


Figure 34. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

Figure 35 shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the MPC8610 SerDes reference clock input's allowed range (100 to 400 mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

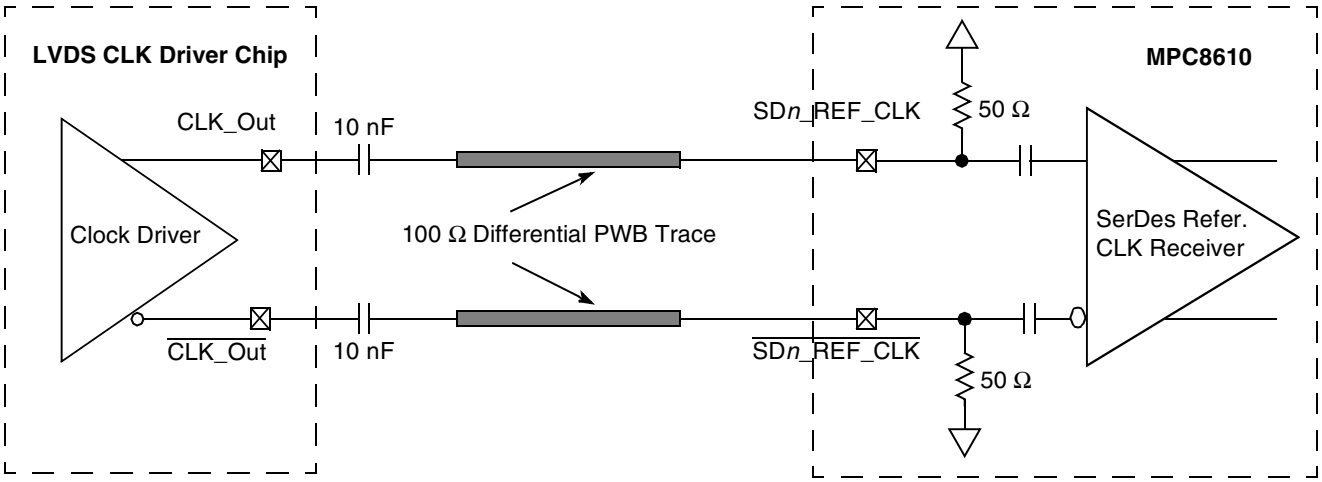


Figure 35. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

Figure 36 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with MPC8610 SerDes reference clock input's DC requirement, AC-coupling has to be used. Figure 36 assumes that the LVPECL clock driver's output impedance is 50 Ω. R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from 140 to 240 Ω depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50-Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8610 SerDes reference clock's differential input amplitude requirement (between 200 and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600 mV, the attenuation factor is 0.67, which requires R2 = 25 Ω. Please consult clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

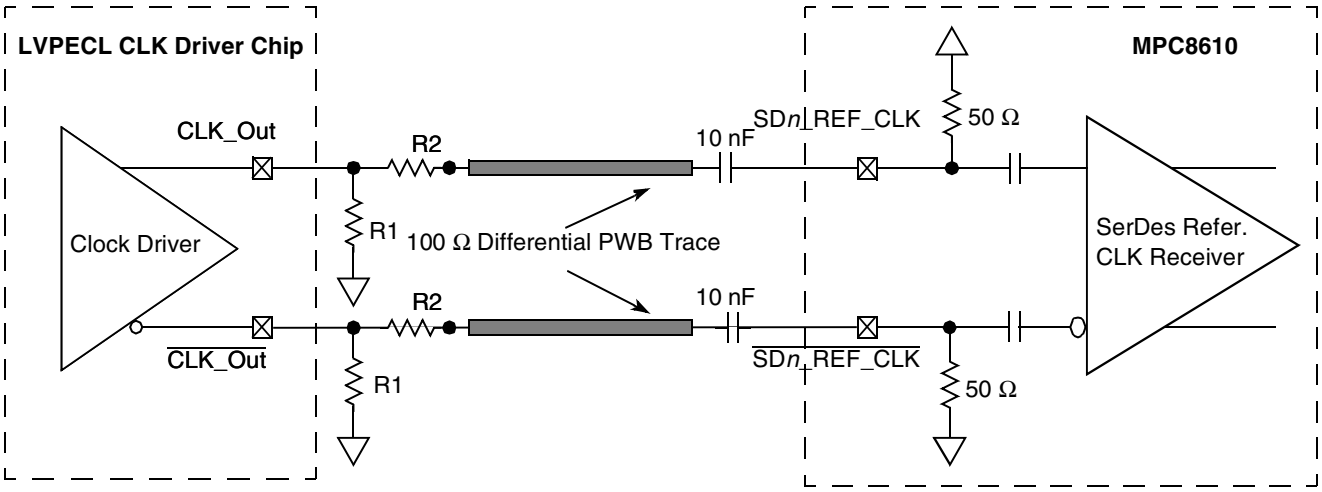


Figure 36. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

2.17.3 SerDes Transmitter and Receiver Reference Circuits

Figure 40 shows the reference circuits for SerDes data lane's transmitter and receiver.

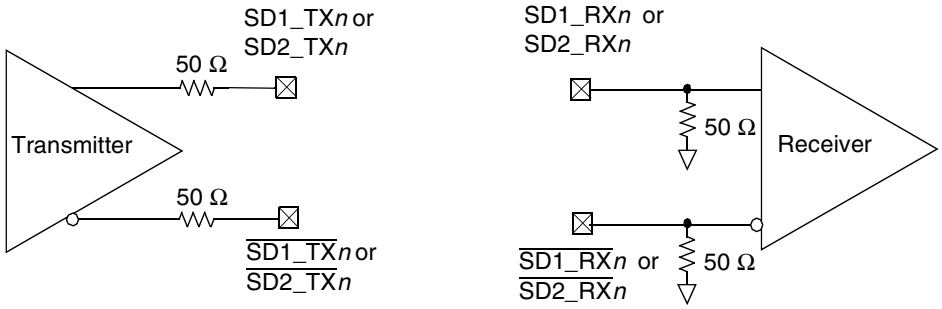


Figure 40. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express) in this document based on the application usage:"

- Section 2.18, "PCI Express"

Note that external AC Coupling capacitor is required for the above serial transmission protocols with the capacitor value defined in specification of each protocol section.

2.18 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the MPC8610.

2.18.1 DC Requirements for PCI Express SD*n*_REF_CLK and SD*n*_REF_CLK

For more information, see Section 2.17.2, "SerDes Reference Clocks."

2.18.2 AC Requirements for PCI Express SerDes Clocks

Table 48 lists AC requirements.

Table 48. SD*n*_REF_CLK and SD*n*_REF_CLK AC Requirements

Symbol	Parameter Description	Min	Typ	Max	Units
t_{REF}	REFCLK cycle time	—	10	—	ns
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–50	—	50	ps

2.18.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

Table 50. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$L_{TX-SKEW}$	Total skew			20	ns	Skew across all lanes on a link. This includes variation in the length of SKP ordered set (e.g., COM and one to five symbols) at the RX as well as any delay differences arising from the interconnect itself.

Notes:

1.)No test load is necessarily associated with this value.

2.)Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 43 should be used as the RX device when taking measurements (also refer to the receiver compliance eye diagram shown in Figure 42). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.

3.)A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.

4.)The receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D– line biased to –300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D– line (that is, as measured by a Vector Network Analyzer with 50-Ω probes—see Figure 43). Note that the series capacitors CTX is optional for the return loss measurement.

5.)Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.

6.)The RX DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit will not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.

7.)It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

2.18.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 42 is specified using the passive compliance/test measurement load (see Figure 43) in place of any real PCI Express RX component.

Note: In general, the minimum receiver eye diagram measured with the compliance/test measurement load (see Figure 43) will be larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum receiver eye diagram (shown in Figure 42) expected at the input receiver based on some adequate combination of system simulations and the return loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

Table 56 provides the clocking specifications for the Platform/MPX bus.

Table 56. Platform/MPX Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	800, 1066, 1333 MHz			
	Min	Max		
Platform/MPX bus clock speed	333	533	MHz	1, 2

Note:
1. **Caution:** The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 3.1.2, "Platform/MPX to SYSCLK PLL Ratio."
2. For MPX clock frequencies at 400 MHz and below, cfg_net2_div must be pulled low.

3.1.2 Platform/MPX to SYSCLK PLL Ratio

The the clock that drives the internal MPX bus is called the platform clock. The frequency of the platform clock is set using the following reset signals, as shown in Table 57:

- SYSCLK input signal
- Binary value on DIU_LD[10], LA[28:31] (cfg_sys_pll[0:4] - reset config) at power up

These signals must be pulled to the desired values. Also note that the DDR data rate is the determining factor in selecting the platform frequency, since the platform frequency must equal the DDR data rate.

For specifications on the PCI_CLK, refer to the PCI 2.2 Specification.

Table 57. Platform/SYSCLK Clock Ratios

Binary Value of DIU_LD[10], LA[28:31] Signals	Platform:SYSCLK Ratio	Binary Value of DIU_LD[10], LA[28:31] Signals	Platform:SYSCLK Ratio
00010	2:1	01010	10:1
00011	3:1	01100	12:1
00100	4:1	01110	14:1
00101	5:1	01111	15:1
00110	6:1	10000	16:1
00111	7:1	10001	17:1
01000	8:1	10010	18:1
01001	9:1	All others	Reserved

Often, heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 54). Therefore, synthetic grease offers the best thermal performance, considering the low interface pressure, and is recommended. Of course, the selection of any thermal interface material depends on many factors—thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, and so on.

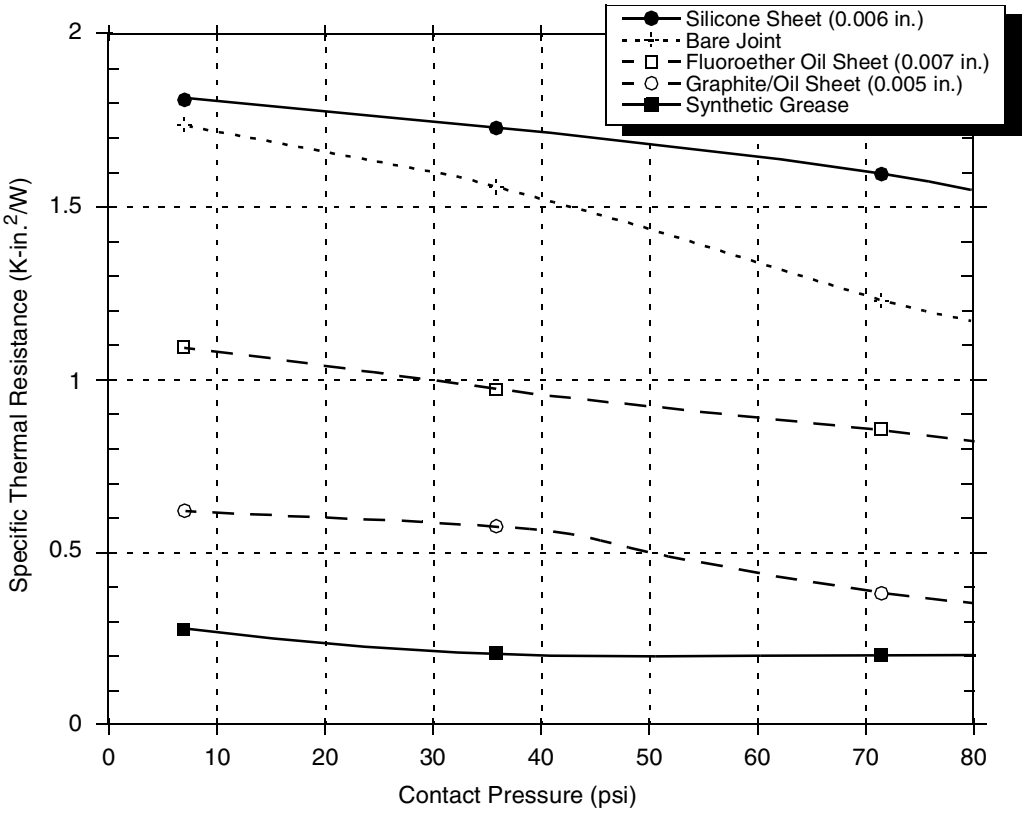


Figure 56. Thermal Performance of Select Thermal Interface Material

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based on high conductivity and mechanical strength to meet equipment shock/vibration requirements. There are several commercially available thermal interfaces and adhesive materials provided by the following vendors:

The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572
Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01801 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Corporate Center PO Box 994 Midland, MI 48686-0994 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674

Thermagon Inc. 888-246-9050
4707 Detroit Ave.
Cleveland, OH 44102
Internet: www.thermagon.com

3.12.2.3 Heat Sink Selection Example

This section provides a heat sink selection example using one of the commercially available heat sinks.

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_i + T_r + (R_{\theta JC} + R_{\theta int} + R_{\theta sa}) \times P_d$$

where:

T_j is the die-junction temperature
T_i is the inlet cabinet ambient temperature
T_r is the air temperature rise within the computer cabinet
$R_{\theta JC}$ is the junction-to-case thermal resistance
$R_{\theta int}$ is the adhesive or interface material thermal resistance
$R_{\theta sa}$ is the heat sink base-to-ambient thermal resistance
P_d is the power dissipated by the device

During operation, the die-junction temperatures (T_j) should be maintained less than the value specified in Table 3. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_i) may range from 30° to 40°C. The air temperature rise within a cabinet (T_r) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material ($R_{\theta int}$) is typically about 0.2°C/W. For example, assuming a T_i of 30°C, a T_r of 5°C, a package $R_{\theta JC}$ = 0.1, and a typical power consumption (P_d) of 10 W, the following expression for T_j is obtained:

Die-junction temperature: $T_j = 30°C + 5°C + (0.1°C/W + 0.2°C/W + \theta_{sa}) \times 10\ W$

For this example, a $R_{\theta sa}$value of 6.7°C/W or less is required to maintain the die junction temperature below the maximum value of Table 3.

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, and so on.

Due to the complexity and variety of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board as well as system-level designs.

3.12.2.4 Recommended Thermal Model

For system thermal modeling, the MPC8610 thermal model is shown in Figure 57. Four cuboids are used to represent this device. The die is modeled as 8.5 × 9.7 mm at a thickness of 0.86 mm. See Section 2.3, “Power Characteristics,” for power dissipation details. The substrate is modeled as a single block 29 × 29 × 1.18 mm with orthotropic conductivity of 23.3 W/(m • K) in the xy-plane and 0.95 W/(m • K) in the z-direction. The die is centered on the substrate. The bump/underfill layer is modeled as a collapsed thermal resistance between the die and substrate with a conductivity of 8.1 W/(m • K) in the thickness dimension of 0.07 mm. The C5 solder layer is modeled as a cuboid with dimensions 29 × 29 × 0.4 mm with orthotropic thermal conductivity of 0.034 W/(m • K) in the xy-plane and 12.1 W/(m • K) in the z-direction. An LGA solder layer would be

An approximate value of the ideality may be obtained by calibrating the device near the expected operating temperature.

Ideality factor is defined as the deviation from the ideal diode equation:

$$I_{fw} = I_s \left[e^{\frac{qV_f}{nKT}} - 1 \right]$$

Another useful equation is:

$$V_H - V_L = n\frac{KT}{q}\left[ln\frac{I_H}{I_L} \right]$$

Where:

I_{fw} = Forward current
I_s = Saturation current
V_d = Voltage at diode
V_f = Voltage forward biased
V_H = Diode voltage while I_H is flowing
V_L = Diode voltage while I_L is flowing
I_H = Larger diode bias current
I_L = Smaller diode bias current
q = Charge of electron (1.6×10^{-19} C)
n = Ideality factor (normally 1.0)
K = Boltzman's constant (1.38×10^{-23} Joules/K)
T = Temperature (Kelvins)

The ratio of I_H to I_L is usually selected to be 10:1. The above simplifies to the following:

$$V_H - V_L = 1.986 \times 10^{-4} \times nT$$

Solving for T, the equation becomes:

$$nT = \frac{V_H - V_L}{1.986 \times 10^{-4}}$$

4 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 4.1, "Part Numbers Fully Addressed by This Document."

4.1 Part Numbers Fully Addressed by This Document

Table 63 provides the Freescale part numbering nomenclature for the MPC8610. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.