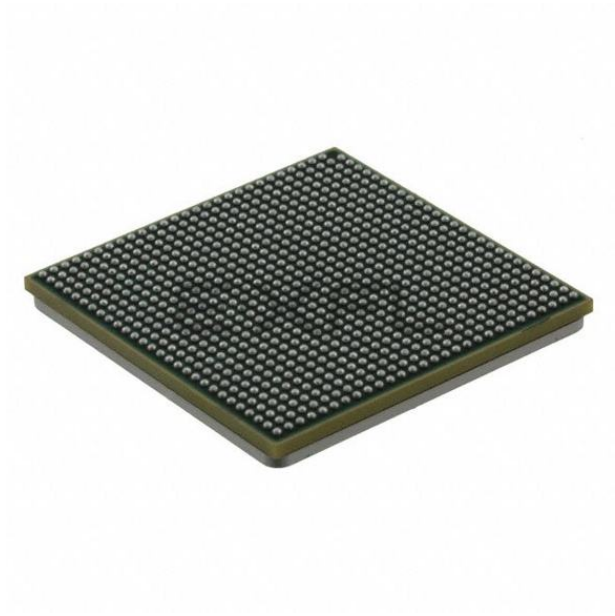

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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e600
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	DIU, LCD
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8610vt800gb

1 Pin Assignments and Reset States

Table 1 provides the pin assignments for the signals.

Table 1. Signal Reference by Functional Block

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
Clocking Signals[4]				
SYSCLK	D28	I	OV_{DD}	
RTC	A25	I	OV_{DD}	17
DDR Memory Interface Signals[2]				
MA[15:0]	AH28, AH25, AH6, AH24, AH22, AG13, AG22, AG19, AH21, AH19, AH18, AG16, AH16, AG15, AH15, AH14	O	GV_{DD}	
MBA[2:0]	AG25, AH13, AH12	O	GV_{DD}	
$\overline{\text{MCS}}$[0:3]	AH10, AG7, AH9, AG4	O	GV_{DD}	
MDQ[0:63]	W26, Y26, AB24, AC28, W27, Y28, AB27, AB26 AD27, AE27, AD25, AF25, AC26, AD28, AC25, AD24, AG24, AF23, AE21, AG21, AE24, AE23, AF22, AD21, AH20, AC19, AG18, AF17, AE20, AF20, AE18, AC17, AC13, AD12, AG9, AE9, AD13, AE12, AD10, AC10, AF8, AE8, AD6, AH5, AD9, AH8, AG6, AE6, AF4, AD4, AC3, AC1, AF5, AE5, AD2, AC4, AB1, AB2, Y1, Y6, AB6, AA6, Y3, Y4	I/O	GV_{DD}	
MECC[0:7]	AD16, AF16, AC15, AF15, AH17, AE17, AA15, AB15	I/O	GV_{DD}	
MDM[0:8]	Y25, AE26, AH23, AD19, AF11, AF7, AE3, AB4, AC16	O	GV_{DD}	
MDQS[0:8]	AA25, AF26, AD22, AD18, AF10, AC7, AD3, AA5, Y15	I/O	GV_{DD}	
$\overline{\text{MDQS}}$[0:8]	AA27, AF28, AC22, AF19, AE11, AD7, AE2, AB5, AB16	I/O	GV_{DD}	
$\overline{\text{M}}$CAS	AG10	O	GV_{DD}	
$\overline{\text{M}}$WE	AH11	O	GV_{DD}	
$\overline{\text{M}}$RAS	AG12	O	GV_{DD}	
MCK[0:5]	AF14, AG28, AH3, AD15, AH27, AG2	O	GV_{DD}	
$\overline{\text{MCK}}$[0:5]	AF13, AG27, AH2, AD14, AH26, AG1	O	GV_{DD}	
MCKE[0:3]	AB28, AA28, AE28, W28	O	GV_{DD}	18
MDIC[0:1]	AD1, AE1	I/O	GV_{DD}	19
MODT[0:3]	AH7, AH4, AG3, AF1	O	GV_{DD}	
Enhanced Local Bus Signals[4]				

Table 1. Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
DMA1_DREQ3/IRQ9/ GPIO2[26]	H26	I	OV_{DD}	23
DMA1_DACK0/IRQ7/ GPIO2[25]	J25	O	OV_{DD}	23
DMA1_DACK3/IRQ10/ GPIO2[27]	J26	O	OV_{DD}	23
DMA1_DDONE0/IRQ8	J27	O	OV_{DD}	23
DMA1_DDONE3/IRQ11/ GPIO2[28]	K27	O	OV_{DD}	23
DMA2_DREQ0/LCS5	R23	I	OV_{DD}	23
DMA2_DREQ3/ GPIO2[29]	H27	I	OV_{DD}	23
DMA2_DACK0/LCS6	N26	O	OV_{DD}	23
DMA2_DACK3/ GPIO2[30]	H28	O	OV_{DD}	23
DMA2_DDONE0/LCS7	R26	O	OV_{DD}	23
DMA2_DDONE3/ GPIO2[31]	J28	O	OV_{DD}	23
General-Purpose Timer Signals[4]				
GTM1_TIN1/GPIO2[15]	U3	I	OV_{DD}	23
GTM1_TIN3/GPIO2[21]	W2	I	OV_{DD}	23
GTM1_TGATE1/ GPIO2[16]	V2	I	OV_{DD}	23
GTM1_TGATE3/ GPIO2[22]	U1	I	OV_{DD}	23
GTM1_TOUT1/GPIO2[17]	W3	O	OV_{DD}	23
GTM1_TOUT3/GPIO2[23]	U2	O	OV_{DD}	23
GTM2_TIN1/GPIO2[18]	V1	I	OV_{DD}	23
GTM2_TGATE1/ GPIO2[19]	W1	I	OV_{DD}	23
GTM2_TOUT1/GPIO2[20]	V3	O	OV_{DD}	23
PCI Signals[4]				
PCI_AD[31:0]	M1, M2, M3, M4, M5,M7, L1, L6, J1, K2, K3, K4, K5, K6, K7, H1, H7, G1, G2, G3, G4, G5, G6, F1, F4, F6, F7, F8, D2, D3, E1, E2	I/O	OV_{DD}	
PCI_C/BE[3:0]	L2, J2, H6, F2	I/O	OV_{DD}	
PCI_PAR	H5	I/O	OV_{DD}	
PCI_FRAME	J3	I/O	OV_{DD}	
PCI_TRDY	J6	I/O	OV_{DD}	

Table 1. Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
V_{DD}_Core	L8, L10, M9, M11, M13, M15, N8, N10, N12, N14, N16, P9, P11, P13, P15, R12, R14, R16, T11, T13, T15, U10, U12, U14, U16, V9, V11, V13, V15, W8, W10, W12, W14, W16, Y9, Y11, Y13, Y7, AA8, AA10, AA12, AB9, AB11, AC8	Core voltage supply	V_{DD}_Core	
V_{DD}_PLAT	L12, L14, L16, L18, M17, P17, T17, V17, V19, W18, Y17, Y19, AA18	Platform supply voltage	V_{DD}_PLAT	
AV_{DD}_Core	A27	Core PLL supply	AV_{DD}_Core	
AV_{DD}_PLAT	B28	Platform PLL supply	AV_{DD}_PLAT	
AV_{DD}_PCI	A2		AV_{DD}_PCI	
$SD1AV_{DD}$	A6		$SD1AV_{DD}$	
$SD2AV_{DD}$	A16		$SD2AV_{DD}$	
$SENSEV_{DD}$	AC11	V_{DD}_Core sensing pin		28
$SENSEV_{SS}$	AB12	Core GND sensing pin		28
GND	B2, B27, D25, E3, F26, F5, G8, H23, J4, K25, L11, L13, L15, L17, L3, L9, M10, M12, M14, M16, M6, M8, N11, N13, N15, N17, N19, N25, N9, P12, P14, P16, P8, R11, R13, R15, R17, R21, R27, R5, T12, T14, T16, U11, U13, U15, U17, U25, U6, U8, U9, V10, V12, V14, V16, V18, V22, V26, W11, W13, W15, W17, W7, W9, Y10, Y12, Y14, Y18, Y27, Y5, Y8, AA11AA13, AA14, AA16, AA17, AA19, AA9, AB10, AB13, AB18, AB19, AB22, AB25, AB3, AB7, AB8, AC14, AD11, AD17, AD20, AD23, AD26, AD5, AD8, AE15, AF12, AF18, AF21, AF24, AF27, AF3, AF6, AF9	GND		
SD1AGND	C6	SerDes port 1 ground pin for $SD1AV_{DD}$		
SD2AGND	B16	SerDes port 2 ground pin for $SD2AV_{DD}$		
SGND	A5, A8, A13, A17, A21, B15, B19, C4, C9, C12, C16, C20, C22, D6, D9, D10, D11, D14, D18, D22, E5, E6, E7, E8, E9, E10, E13, E14, E15, E16, E17, E18, E19, E20	Ground pins for SV_{DD}		
XGND	E12, F9, F15, F19, F23, G13, G17, G21, H10, H16, H20, J8, J12, J14, J18, K8, K9, K11, K15, K17, K19, K21	Ground pins for XV_{DD}		

2 Electrical Characteristics

This section provides the AC and DC electrical specifications for the MPC8610. The MPC8610 is currently targeted to these specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

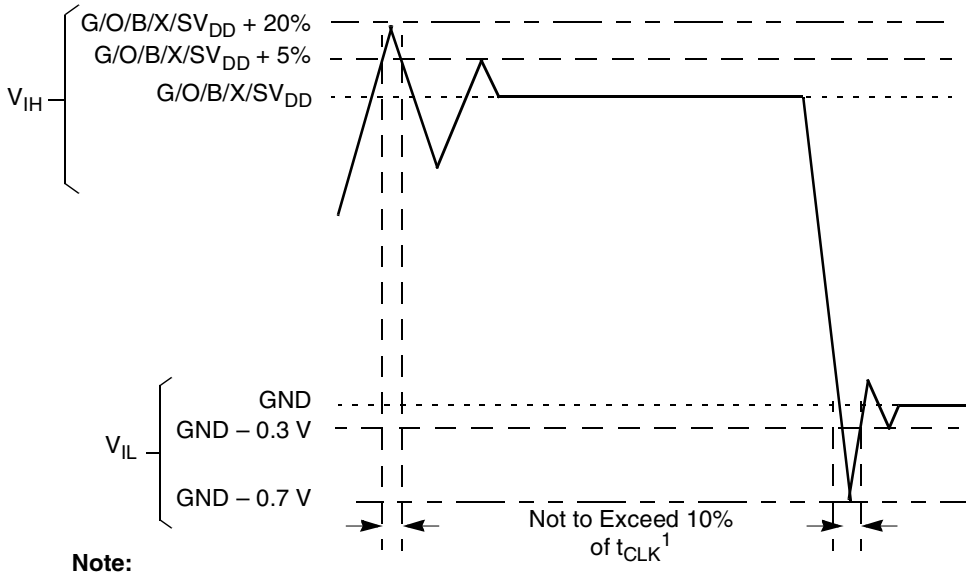
2.1.1 Absolute Maximum Ratings

Table 2 provides the absolute maximum ratings.

Table 2. Absolute Maximum Ratings[1]

Characteristic		Symbol	Recommended Value	Unit	Notes
Core supply voltages		V_{DD}_Core	–0.3 to 1.21	V	
Core PLL supply		AV_{DD}_Core	–0.3 to 1.21	V	
SerDes receiver and core power supply (ports 1 and 2)		$S1V_{DD}$ $S2V_{DD}$	–0.3 to 1.21	V	
SerDes transmitter power supply (ports 1 and 2)		$X1V_{DD}$ $X2V_{DD}$	–0.3 to 1.21	V	
SerDes digital logic power supply (ports 1 and 2)		$L1V_{DD}$ $L2V_{DD}$	–0.3 to 1.21	V	
Serdes PLL supply voltage (ports 1 and 2)		$SD1AV_{DD}$ $SD2AV_{DD}$	–0.3 to 1.21	V	
Platform supply voltage		V_{DD}_PLAT	–0.3 to 1.21	V	
PCI and platform PLL supply voltage		AV_{DD}_PCI AV_{DD}_PLAT	–0.3 to 1.21	V	
DDR/DDR2 SDRAM I/O supply voltages		GV_{DD}	–0.3 to 2.75	V	
Local bus and SSI I/O voltage		BV_{DD}	–0.3 to 3.63	V	
LCD, PCI, general purpose timer, MPIC, IrDA, DUART, DMA, interrupts, system control and clocking, debug, test, JTAG, power management, I^2C, SPI, and miscellaneous I/O voltage		OV_{DD}	–0.3 to 3.63	V	
Input voltage	DDR/DDR2 SDRAM signals	MV_{IN}	(GND – 0.3) to (GV_{DD} + 0.3)	V	2
	DDR/DDR2 SDRAM reference	MV_{REF}	(GND – 0.3) to (GV_{DD}/2 + 0.3)	V	2
	Local bus I/O voltage	BV_{IN}	(GND – 0.3) to (BV_{DD} + 0.3)	V	2
	LCD, PCI, general purpose, MPIC, IrDA, DUART, DMA, interrupts, system control and clocking, debug, test, JTAG, power management, I^2C, SPI and miscellaneous I/O voltage	OV_{IN}	(GND – 0.3) to (OV_{DD} + 0.3)	V	2

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8610.



Note:
1. t_{CLK} references clocks for various functional blocks as follows:
For DDR, t_{CLK} references MCK.
For LBIU, t_{CLK} references LCLK.
For PCI, t_{CLK} references PCI_CLK or SYSCLK.
For I^2C and JTAG, t_{CLK} references SYSCLK.

Figure 2. Overshoot/Undershoot Voltage for M/B/OV_{IN}

The MPC8610 core voltage must always be provided at nominal V_{DD}_Core (see Table 3 for actual recommended core voltage). Voltage to the external interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD}-based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced to each externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$) as is appropriate for the (SSTL-18 and SSTL-2) electrical signaling standards.

2.1.3 Output Driver Characteristics

Table 4 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 4. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
DDR signals	18 36 (half strength mode)	GV_{DD} = 2.5 V	1, 4, 6
DDR2 signals	18 36 (half strength mode)	GV_{DD} = 1.8 V	1, 5, 6

Table 4. Output Drive Capability (continued)

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus	25 35	BV_{DD} = 3.3 V BV_{DD} = 2.5 V	2
	45 (default) 45 (default) 125	BV_{DD} = 3.3 V BV_{DD} = 2.5 V BV_{DD} = 1.8 V	
PCI, DUART, DMA, interrupts, system control and clocking, debug, test, JTAG, power management, and miscellaneous I/O voltage	45	OV_{DD} = 3.3 V	
I^2C	150	OV_{DD} = 3.3 V	
PCI Express	100	XV_{DD} = 1.0 V	3

Notes:
1. See the DDR control driver registers in the *MPC8610 Integrated Host Processor Reference Manual,* for more information.
2. See the POR impedance control register in the *MPC8610 Integrated Host Processor Reference Manual,* for more information about local bus signals and their drive strength programmability.
3. See Section 1, "Pin Assignments and Reset States," for details on resistor requirements for the calibration of SD*n*_IMP_CAL_TX and SD*n*_IMP_CAL_RX transmit and receive signals.
4. Stub series terminated logic (SSTL-25) type pins.
5. Stub series terminated logic (SSTL-18) type pins.
6. The drive strength of the DDR interface in half strength mode is at T_j = 105°C and at GV_{DD} (min).

2.2 Power Sequencing

The MPC8610 requires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows:

The chronological order of power up is:

1. OV_{DD}, BV_{DD}
2. V_{DD}_PLAT, AV_{DD}_PLAT, V_{DD}_Core, AV_{DD}_Core, AV_{DD}_PCI, S*n*V_{DD}, X*n*V_{DD}, SD*n*AV_{DD} (this rail must reach 90% of its value before the rail for GV_{DD} and MV_{REF} reaches 10% of its value)
3. GV_{DD}, MV_{REF}
4. SYSCLK

The order of power down is as follows:

1. SYSCLK
2. GV_{DD}, MV_{REF}
3. V_{DD}_PLAT, AV_{DD}_PLAT, V_{DD}_Core, AV_{DD}_Core, AV_{DD}_PCI, S*n*V_{DD}, X*n*V_{DD}, SD*n*AV_{DD}
4. O_{DD}, BV_{DD}

NOTE

AV_{DD} type supplies should be delayed with respect to their source supplies by the RC time constant of the PLL filter circuit described in Section 3.2, "Power Supply Design and Sequencing."

2.3 Power Characteristics

The power dissipation for the MPC8610 device is shown in Table 5.

Table 5. MPC8610 Power Dissipation

Power Mode	Core/Platform Frequency (MHz)	V_{DD}_Core, V_{DD}_PLAT (V)	Junction Temperature (°C)	Power (Watts)	Notes
Typical	1333/533	1.025	65	10.7	1, 2
Thermal			105	12.1	1, 3
Maximum				16	1, 4
Typical	1066/533	1.00	65	8.4	1, 2
Thermal			105	9.8	1, 3
Maximum				13	1, 4
Typical	800/400	1.00	65	5.8	1, 2
Thermal			105	7.2	1, 3
Maximum				9.5	1, 4

Notes:

1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.
2. Typical power is an average value measured at the nominal recommended core voltage (V_{DD}_Core) and 65°C junction temperature (see Table 3) while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz with the core at 100% efficiency. This parameter is not 100% tested but periodically sampled.
3. Thermal power is the average power measured at nominal core voltage (V_{DD}_Core) and maximum operating junction temperature (see Table 3) while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz on the core and a typical workload on platform interfaces. This parameter is not 100% tested but periodically sampled.
4. Maximum power is the maximum power measured at nominal core voltage (V_{DD}_Core) and maximum operating junction temperature (see Table 3) while running a test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep all the execution units maximally busy on the core.

The estimated maximum power dissipation for individual power supplies of the MPC8610 is shown in Table 6.

Table 6. MPC8610 Individual Supply Maximum Power Dissipation[1]

Component Description	Supply Voltage (V)	Est. Power (Watts)	Notes
Core voltage supply	V_{DD}_Core = 1.025 V @ 1333 MHz	14.0	
	V_{DD}_Core = 1.00 V @ 1066 MHz	12.0	
Core PLL voltage supply	AV_{DD}_Core = 1.025 V @ 1333 MHz	0.0125	
	AV_{DD}_Core = 1.00 V @ 1066 MHz	0.0125	
Platform source supply	V_{DD}_PLAT = 1.025 V @ 1333 MHz	4.5	
	V_{DD}_PLAT = 1.00 V @ 1066 MHz	4.3	

2.6.2.2 DDR SDRAM Output AC Timing Specifications

Table 22. DDR SDRAM Output AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MCK[n] cycle time, MCK[n]/$\overline{\text{MCK}}$[n] crossing	t_{MCK}	3	10	ns	2
MCK duty cycle	t_{MCKH}/t_{MCK}			%	
533 MHz		47	53		8
400 MHz		47	53		8
333 MHz		47	53		
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		
333 MHz		2.40	—		
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		
333 MHz		2.40	—		
$\overline{\text{MCS}}$[n] output setup with respect to MCK	t_{DDKHCS}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		
333 MHz		2.40	—		
$\overline{\text{MCS}}$[n] output hold with respect to MCK	t_{DDKHCX}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		
333 MHz		2.40	—		
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
533 MHz		590	—		7
400 MHz		700	—		
333 MHz		900	—		
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
533 MHz		590	—		7
400 MHz		700	—		
333 MHz		900	—		
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6

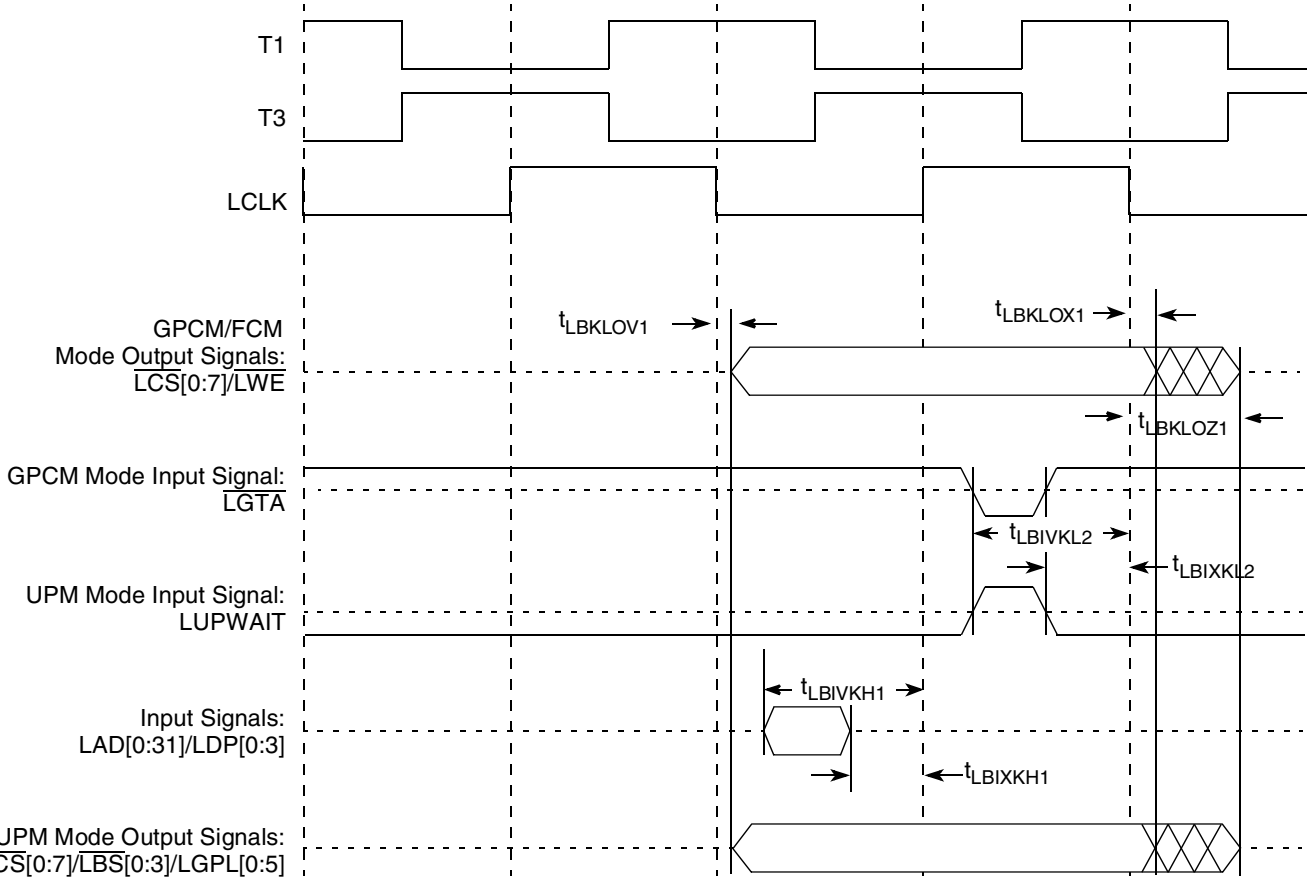


Figure 10. Local Bus Signals, GPCM/UPM/FCM Signals for LCRR[CLKDIV] = 2 (Clock Ratio of 4)

Figure 13 depicts the vertical timing (timing of one frame), including both the vertical sync pulse and the data. All parameters shown in the diagram are programmable.

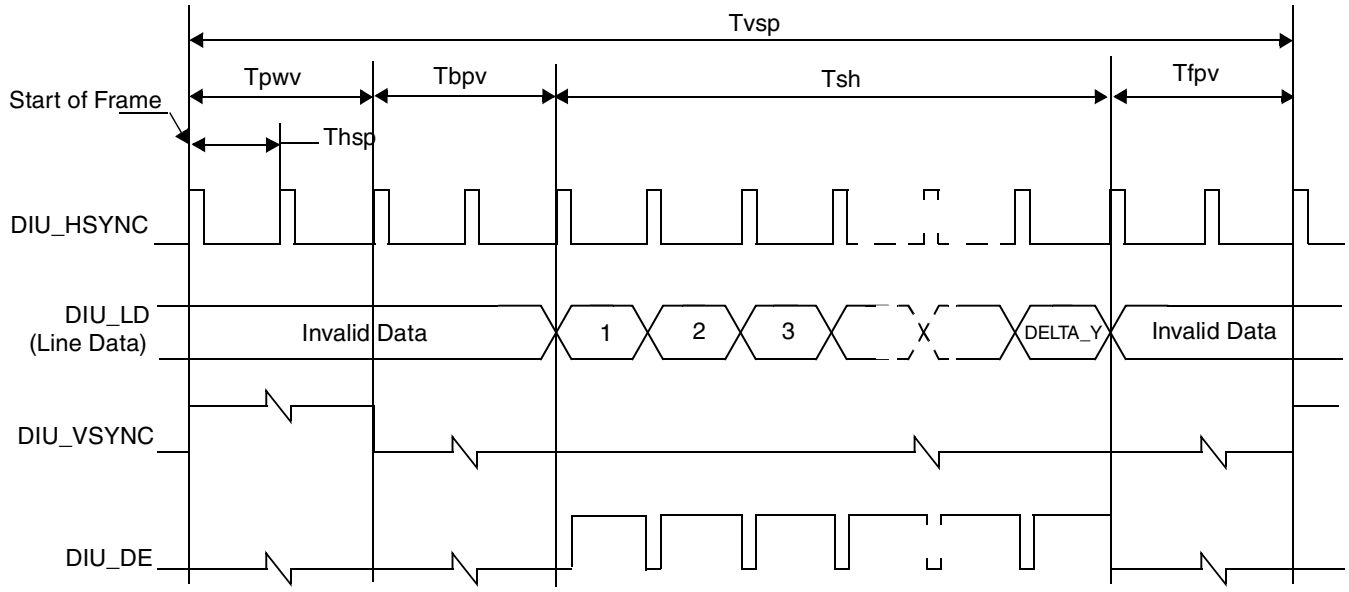


Figure 13. TFT DIU/LCD Interface Timing Diagram—Vertical Sync Pulse

Table 28 shows timing parameters of signals presented in Figure 12 and Figure 13.

Table 28. DIU Interface AC Timing Parameters—Pixel Level

Parameter	Symbol	Value	Unit	Notes
Display pixel clock period	t_{PCP}	7.5 (minimum)	ns	1, 2
HSYNC width	t_{PWH}	PW_H × t_{PCP}	ns	
HSYNC back porch width	t_{BPH}	BP_H × t_{PCP}	ns	
HSYNC front porch width	t_{FPH}	FP_H × t_{PCP}	ns	
Screen width	t_{SW}	DELTA_X × t_{PCP}	ns	
HSYNC (line) period	t_{HSP}	(PW_H + BP_H + DELTA_X + FP_H) × t_{PCP}	ns	
VSYNC width	t_{PWV}	PW_V × t_{HSP}	ns	
HSYNC back porch width	t_{BPV}	BP_V × t_{HSP}	ns	
HSYNC front porch width	t_{FPV}	FP_V × t_{HSP}	ns	
Screen height	t_{SH}	DELTA_Y × t_{HSP}	ns	
VSYNC (frame) period	t_{VSP}	(PW_V + BP_V + DELTA_Y + FP_H) × t_{HSP}	ns	

Notes:

1 Display interface pixel clock period immediate value (in nanoseconds).

2 Display pixel clock frequency must also be less than or equal to 1/3 the platform clock.

The DELTA_X and DELTA_Y parameters are programmed via the DISP_SIZE register. The PW_H, BP_H, and FP_H parameters are programmed via the HSYN_PARA register; and the PW_V, BP_V, and FP_V parameters are programmed via the VSYN_PARA register.

Figure 14 depicts the synchronous display interface timing for access level, and Table 29 lists the timing parameters.

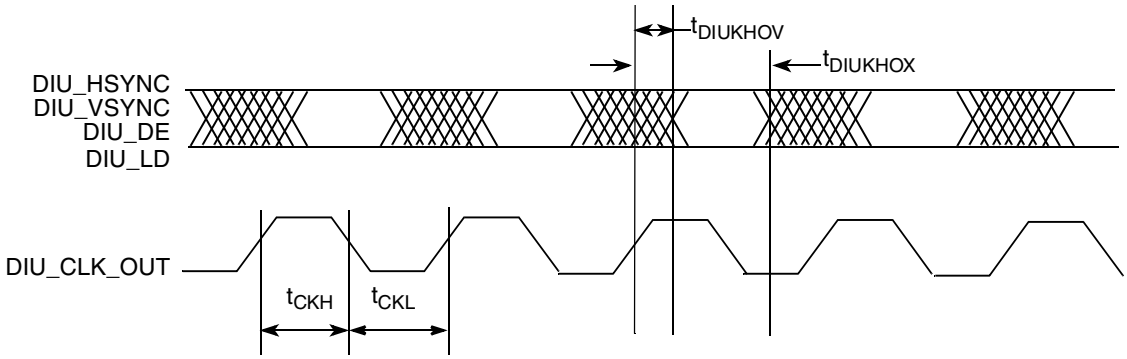


Figure 14. LCD Interface Timing Diagram—Access Level

NOTE

The DIU_OUT_CLK edge and phase delay is selectable via the Global Utilities CKDVDR register.

Table 29. LCD Interface Timing Parameters—Access Level

Parameter	Symbol	Min	Typ	Max	Unit
LCD interface pixel clock high time	t_{CKH}	$0.35 \times t_{PCP}$	$0.5 \times t_{PCP}$	$0.65 \times t_{PCP}$	ns
LCD interface pixel clock low time	t_{CKL}	$0.35 \times t_{PCP}$	$0.5 \times t_{PCP}$	$0.65 \times t_{PCP}$	ns
LCD interface pixel clock to ouput valid	$t_{DIUKHOV}$	—	—	2	ns
LCD interface output hold from pixel clock	$t_{DIUKHOX}$	$t_{PCP} - 2$	—	—	ns

2.9 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the MPC8610.

2.9.1 I²C DC Electrical Characteristics

Table 30 provides the DC electrical characteristics for the I²C interfaces.

Table 30. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	2

2.12.2.2 SSI Receiver Timing with Internal Clock

Table 36 provides the receiver timing parameters with internal clock.

Table 36. SSI Receiver with Internal Clock Timing Parameters

Parameter	Symbol	Min	Max	Unit
Internal Clock Operation				
(Tx/Rx) CK clock period	SS1	81.4	—	ns
(Tx/Rx) CK clock high period	SS2	36.0	—	ns
(Tx/Rx) CK clock rise time	SS3	—	6	ns
(Tx/Rx) CK clock low period	SS4	36.0	—	ns
(Tx/Rx) CK clock fall time	SS5	—	6	ns
(Rx) CK high to FS high	SS11	—	15.0	ns
(Rx) CK high to FS low	SS13	—	15.0	ns
SRXD setup time before (Rx) CK low	SS20	10.0	—	ns
SRXD hold time after (Rx) CK low	SS21	0	—	ns

Figure 18 provides the SSI receiver timing with internal clock.

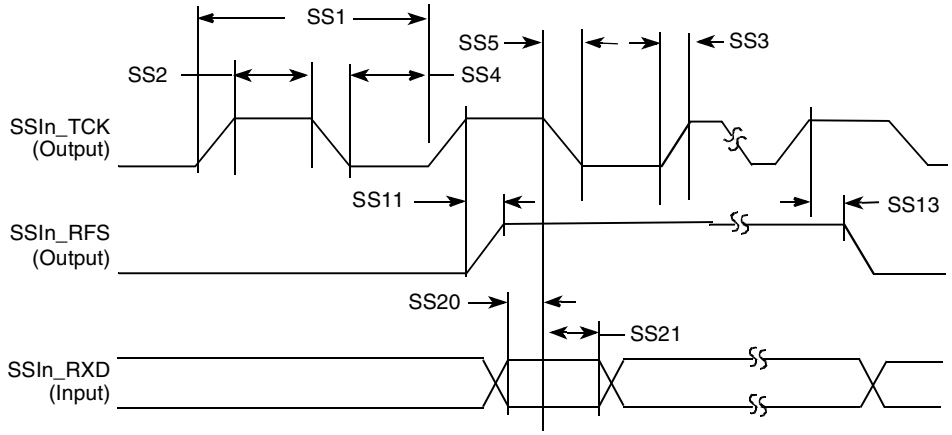


Figure 18. SSI Receiver with Internal Clock Timing Diagram

2.12.2.3 SSI Transmitter Timing with External Clock

Table 37 provides the transmitter timing parameters with external clock.

Table 37. SSI Transmitter with External Clock Timing Parameters

Parameter	Symbol	Min	Max	Unit
External Clock Operation				
(Tx/Rx) CK clock period	SS22	81.4	—	ns
(Tx/Rx) CK clock high period	SS23	36.0	—	ns
(Tx/Rx) CK clock rise time	SS24	—	6.0	ns

2.17.3 SerDes Transmitter and Receiver Reference Circuits

Figure 40 shows the reference circuits for SerDes data lane's transmitter and receiver.

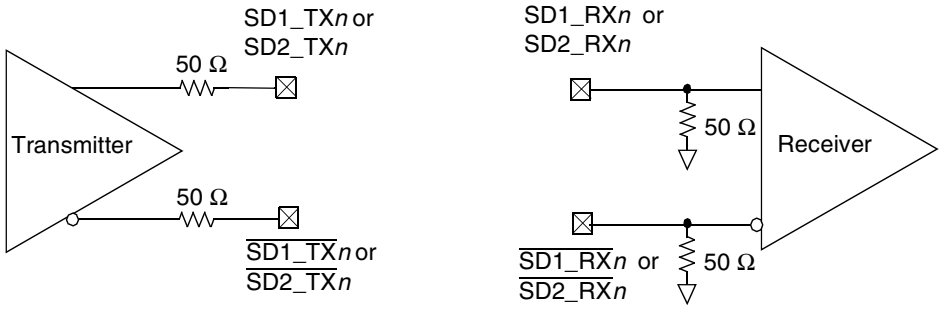


Figure 40. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express) in this document based on the application usage:"

- Section 2.18, "PCI Express"

Note that external AC Coupling capacitor is required for the above serial transmission protocols with the capacitor value defined in specification of each protocol section.

2.18 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the MPC8610.

2.18.1 DC Requirements for PCI Express SD*n*_REF_CLK and SD*n*_REF_CLK

For more information, see Section 2.17.2, "SerDes Reference Clocks."

2.18.2 AC Requirements for PCI Express SerDes Clocks

Table 48 lists AC requirements.

Table 48. SD*n*_REF_CLK and SD*n*_REF_CLK AC Requirements

Symbol	Parameter Description	Min	Typ	Max	Units
t_{REF}	REFCLK cycle time	—	10	—	ns
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–50	—	50	ps

2.18.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

Table 49. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$T_{crosslink}$	Crosslink random timeout	0		1	ms	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one downstream and one upstream port. See Note 7

Notes:

1.) No test load is necessarily associated with this value.

2.) Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 43 and measured over any 250 consecutive TX UIs. (Also refer to the transmitter compliance eye diagram shown in Figure 41.)

3.) A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

4.) The transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes—see Figure 43). Note that the series capacitors C_{TX} is optional for the return loss measurement.

5.) Measured between 20–80% at transmitter package pins into a test load as shown in Figure 43 for both V_{TX-D+} and V_{TX-D-}.

6.) See Section 4.3.1.8 of the *PCI Express Base Specifications,* Rev. 1.0a.

7.) See Section 4.2.6.3 of the *PCI Express Base Specifications*, Rev. 1.0a.

2.18.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in Figure 41 is specified using the passive compliance/test measurement load (see Figure 43) in place of any real PCI Express interconnect + RX component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit will always be relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (i.e., least squares and median deviation fits).

NOTE

The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (i.e., as measured by a vector network analyzer with 50-Ω probes—see Figure 43). Note that the series capacitors, CTX, are optional for the return loss measurement.

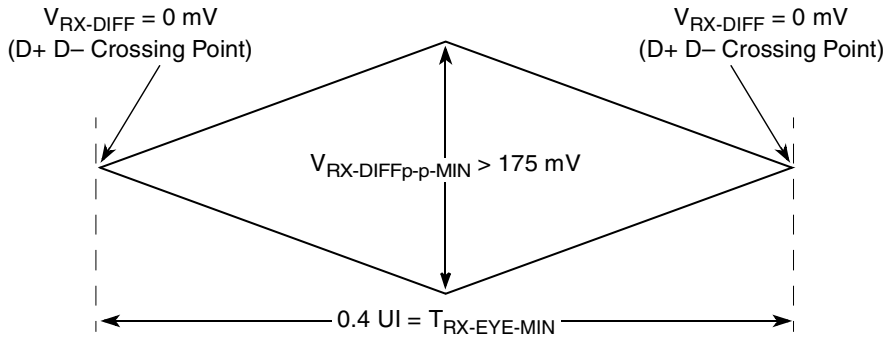


Figure 42. Minimum Receiver Eye Timing and Voltage Compliance Specification

2.18.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 43.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

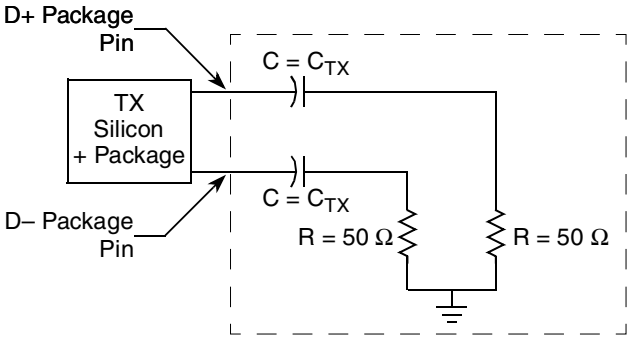


Figure 43. Compliance Test/Measurement Load

2.19 JTAG

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8610.

2.19.1 JTAG DC Electrical Characteristics

Table 51 provides the JTAG DC electrical characteristics for the JTAG interface.

- SerDes—Receiver lanes configured for PCI Express are allowed to be disconnected (as would occur when a PCI Express slot is connected but not populated). Directions for terminating the SerDes signals is discussed in Section 3.10, "Guidelines for High-Speed Interface Termination."

3.6 Pull-Up and Pull-Down Resistor Requirements

The MPC8610 requires weak pull-up resistors (2–10 kΩ is recommended) on open drain type pins including I^2C pins and PIC interrupt pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 53. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Refer to the PCI 2.2 specification for all pull-ups required for PCI.

The following pins must not be pulled down during power-on reset: DIU_LD[5:6], MSRCID[1:2], $\overline{\text{HRESET\_REQ}}$, and TRIG_OUT/READY.

The following are factory test pins and require strong pull up resistors (100 Ω – 1 kΩ) to OV_{DD}: $\overline{\text{LSSD\_MODE}}$, TEST_MODE[0:3].

The following pins require weak pull-up resistors (2–10 kΩ) to their specific power supplies: $\overline{\text{LCS}}$[0:4], $\overline{\text{LCS}}$[5]/$\overline{\text{DMA_DREQ}}$2, $\overline{\text{LCS}}$[6]/$\overline{\text{DMA\_DACK}}$[2], $\overline{\text{LCS}}$[7]/$\overline{\text{DMA\_DDONE}}$[2], IRQ_OUT, IIC1_SDA, IIC1_SCL, IIC2_SDA, IIC2_SCL, and CKSTP_OUT.

The following pins should be pulled to ground with a 100-Ω resistor: SD1_IMP_CAL_TX, SD2_IMP_CAL_TX. The following pins should be pulled to ground with a 200-Ω resistor: SD1_IMP_CAL_RX, SD2_IMP_CAL_RX.

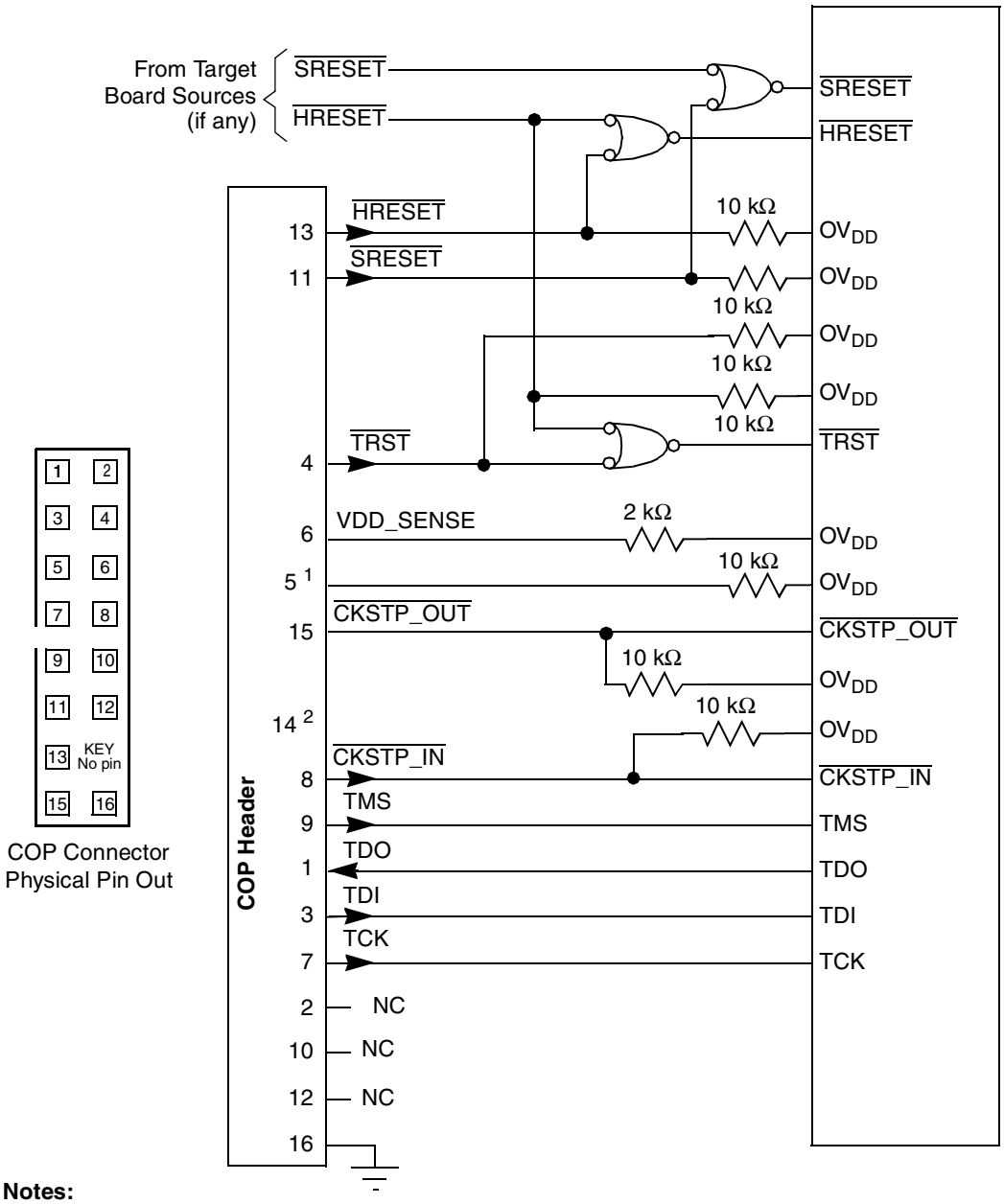
When the platform frequency is 400 MHz, cfg_platform_freq must be pulled down at reset. Also, cfg_dram_type[0 or 1] must be valid at power-up even before $\overline{\text{HRESET}}$ assertion.

For other pin pull-up or pull-down recommendations of signals, see Section 1, "Pin Assignments and Reset States."

3.7 Output Buffer DC Impedance

The MPC8610 drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 51). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and



Notes:

1. RUN/$\overline{\text{STOP}}$, normally found on pin 5 of the COP header, is not implemented. Connect pin 5 of the COP header to OV_{DD} with a 10-kΩ pull-up resistor.
2. Key location; pin 14 is not physically present on the COP header.

Figure 53. JTAG Interface Connection

3.11 Guidelines for PCI Interface Termination

PCI termination if PCI is not used at all.

Option 1

- If PCI arbiter is enabled during POR,
  - All AD pins will be driven to the stable states after POR. Therefore, all ADs pins can be floating. This includes PCI_AD[31:0], PCI_C/$\overline{BE}$[3:0], and PCI_PAR signals.
  - All PCI control pins can be grouped together and tied to OV_{DD} through a single 10-kΩ resistor.
  - It is optional to disable PCI block through DEVDISR register after POR reset.

Option 2

- If PCI arbiter is disabled during POR,
  - All AD pins will be in the input state. Therefore, all ADs pins need to be grouped together and tied to OV_{DD} through a single (or multiple) 10-kΩ resistor(s)
  - All PCI control pins can be grouped together and tied to OV_{DD} through a single 10-kΩ resistor
  - It is optional to disable PCI block through DEVDISR register after POR reset.

3.12 Thermal

This section describes the thermal specifications of the MPC8610.

3.12.1 Thermal Characteristics

Table 62 provides the package thermal characteristics for the MPC8610.

Table 62. Package Thermal Characteristics[1]

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient thermal resistance, natural convection, single-layer (1s) board	$R_{\theta JA}$	24	°C/W	1
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	$R_{\theta JA}$	18	°C/W	1
Junction-to-ambient thermal resistance, 200 ft/min airflow, single-layer (1s) board	$R_{\theta JMA}$	18	°C/W	1
Junction-to-ambient thermal resistance, 200 ft/min airflow, four-layer (2s2p) board	$R_{\theta JMA}$	15	°C/W	1
Junction-to-board thermal resistance	$R_{\theta JB}$	10	°C/W	2
Junction-to-case thermal resistance	$R_{\theta JC}$	<0.1	°C/W	3

Notes:
1. Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
2. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-case resistance is less than 0.1°C/W because the silicon die is the top of the packaging case..

3.12.2 Thermal Management Information

This section provides thermal management information for the flip-chip, plastic ball-grid array (FC_PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The MPC8610 implements several features designed to assist with thermal management, including the temperature diode. The temperature diode allows an external device to monitor the die temperature in order to detect excessive temperature conditions and alert the system; see Section 3.12.2.5, “Temperature Diode,” for more information.

Thermagon Inc. 888-246-9050
4707 Detroit Ave.
Cleveland, OH 44102
Internet: www.thermagon.com

3.12.2.3 Heat Sink Selection Example

This section provides a heat sink selection example using one of the commercially available heat sinks.

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_i + T_r + (R_{\theta JC} + R_{\theta int} + R_{\theta sa}) \times P_d$$

where:

T_j is the die-junction temperature
T_i is the inlet cabinet ambient temperature
T_r is the air temperature rise within the computer cabinet
$R_{\theta JC}$ is the junction-to-case thermal resistance
$R_{\theta int}$ is the adhesive or interface material thermal resistance
$R_{\theta sa}$ is the heat sink base-to-ambient thermal resistance
P_d is the power dissipated by the device

During operation, the die-junction temperatures (T_j) should be maintained less than the value specified in Table 3. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_i) may range from 30° to 40°C. The air temperature rise within a cabinet (T_r) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material ($R_{\theta int}$) is typically about 0.2°C/W. For example, assuming a T_i of 30°C, a T_r of 5°C, a package $R_{\theta JC}$ = 0.1, and a typical power consumption (P_d) of 10 W, the following expression for T_j is obtained:

Die-junction temperature: $T_j = 30°C + 5°C + (0.1°C/W + 0.2°C/W + \theta_{sa}) \times 10\ W$

For this example, a $R_{\theta sa}$value of 6.7°C/W or less is required to maintain the die junction temperature below the maximum value of Table 3.

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, and so on.

Due to the complexity and variety of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board as well as system-level designs.

3.12.2.4 Recommended Thermal Model

For system thermal modeling, the MPC8610 thermal model is shown in Figure 57. Four cuboids are used to represent this device. The die is modeled as 8.5 × 9.7 mm at a thickness of 0.86 mm. See Section 2.3, “Power Characteristics,” for power dissipation details. The substrate is modeled as a single block 29 × 29 × 1.18 mm with orthotropic conductivity of 23.3 W/(m • K) in the xy-plane and 0.95 W/(m • K) in the z-direction. The die is centered on the substrate. The bump/underfill layer is modeled as a collapsed thermal resistance between the die and substrate with a conductivity of 8.1 W/(m • K) in the thickness dimension of 0.07 mm. The C5 solder layer is modeled as a cuboid with dimensions 29 × 29 × 0.4 mm with orthotropic thermal conductivity of 0.034 W/(m • K) in the xy-plane and 12.1 W/(m • K) in the z-direction. An LGA solder layer would be

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