



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, SD, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I ² S, LCD, LVD, POR, PWM, WDT
Number of I/O	98
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 42x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk40dx256vlq10

Table of Contents

1 Ordering parts.....	5	5.4.2 Thermal attributes.....	23
1.1 Determining valid orderable parts.....	5	6 Peripheral operating requirements and behaviors.....	24
2 Part identification.....	5	6.1 Core modules.....	24
2.1 Description.....	5	6.1.1 Debug trace timing specifications.....	24
2.2 Format.....	5	6.1.2 JTAG electricals.....	25
2.3 Fields.....	5	6.2 System modules.....	28
2.4 Example.....	6	6.3 Clock modules.....	28
3 Terminology and guidelines.....	6	6.3.1 MCG specifications.....	28
3.1 Definition: Operating requirement.....	6	6.3.2 Oscillator electrical specifications.....	30
3.2 Definition: Operating behavior.....	7	6.3.3 32 kHz oscillator electrical characteristics.....	33
3.3 Definition: Attribute.....	7	6.4 Memories and memory interfaces.....	33
3.4 Definition: Rating.....	8	6.4.1 Flash electrical specifications.....	33
3.5 Result of exceeding a rating.....	8	6.4.2 EzPort switching specifications.....	38
3.6 Relationship between ratings and operating requirements.....	8	6.4.3 Flexbus switching specifications.....	39
3.7 Guidelines for ratings and operating requirements.....	9	6.5 Security and integrity modules.....	42
3.8 Definition: Typical value.....	9	6.6 Analog.....	42
3.9 Typical value conditions.....	10	6.6.1 ADC electrical specifications.....	42
4 Ratings.....	11	6.6.2 CMP and 6-bit DAC electrical specifications.....	50
4.1 Thermal handling ratings.....	11	6.6.3 12-bit DAC electrical characteristics.....	53
4.2 Moisture handling ratings.....	11	6.6.4 Voltage reference electrical specifications.....	56
4.3 ESD handling ratings.....	11	6.7 Timers.....	57
4.4 Voltage and current operating ratings.....	11	6.8 Communication interfaces.....	57
5 General.....	12	6.8.1 USB electrical specifications.....	57
5.1 AC electrical characteristics.....	12	6.8.2 USB DCD electrical specifications.....	58
5.2 Nonswitching electrical specifications.....	12	6.8.3 USB VREG electrical specifications.....	58
5.2.1 Voltage and current operating requirements.....	13	6.8.4 CAN switching specifications.....	59
5.2.2 LVD and POR operating requirements.....	14	6.8.5 DSPI switching specifications (limited voltage range).....	59
5.2.3 Voltage and current operating behaviors.....	14	6.8.6 DSPI switching specifications (full voltage range).....	60
5.2.4 Power mode transition operating behaviors.....	16	6.8.7 Inter-Integrated Circuit Interface (I2C) timing.....	62
5.2.5 Power consumption operating behaviors.....	17	6.8.8 UART switching specifications.....	63
5.2.6 EMC radiated emissions operating behaviors.....	20	6.8.9 SDHC specifications.....	63
5.2.7 Designing with radiated emissions in mind.....	21	6.8.10 I2S/SAI switching specifications.....	64
5.2.8 Capacitance attributes.....	21	6.9 Human-machine interfaces (HMI).....	71
5.3 Switching specifications.....	21	6.9.1 TSI electrical specifications.....	71
5.3.1 Device clock specifications.....	21	6.9.2 LCD electrical characteristics.....	72
5.3.2 General switching specifications.....	22	7 Dimensions.....	73
5.4 Thermal specifications.....	23	7.1 Obtaining package dimensions.....	73
5.4.1 Thermal operating requirements.....	23		

1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers: PK40 and MK40 .

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	- M = Fully qualified, general market flow - P = Prequalification
K##	Kinetis family	K40
A	Key attribute	- D = Cortex-M4 w/ DSP - F = Cortex-M4 w/ DSP and FPU
M	Flash memory type	- N = Program flash only - X = Program flash and FlexMemory

Table continues on the next page...

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	-0.3	3.8	V
I_{DD}	Digital supply current	—	185	mA
V_{DIO}	Digital input voltage (except RESET, EXTAL, and XTAL)	-0.3	5.5	V
V_{AIO}	Analog ¹ , RESET, EXTAL, and XTAL input voltage	-0.3	$V_{DD} + 0.3$	V
I_D	Maximum current single pin limit (applies to all digital pins)	-25	25	mA
V_{DDA}	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V
V_{USB_DP}	USB_DP input voltage	-0.3	3.63	V
V_{USB_DM}	USB_DM input voltage	-0.3	3.63	V
VREGIN	USB regulator input	-0.3	6.0	V
V_{BAT}	RTC battery supply voltage	-0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

5 General

5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

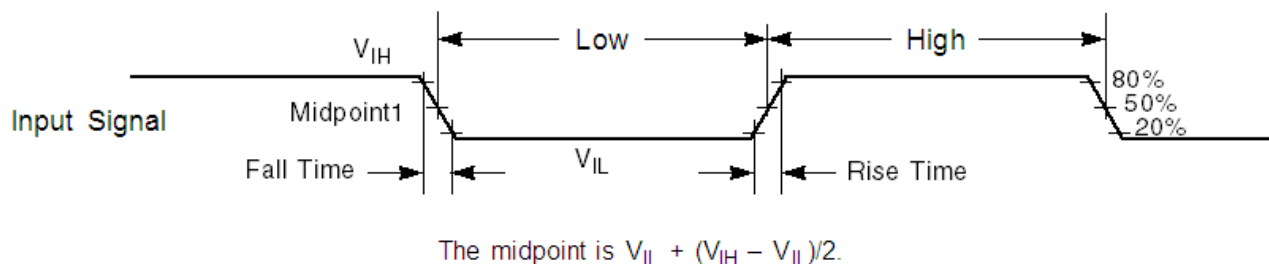


Figure 1. Input signal measurement reference

All digital I/O switching characteristics assume:

1. output pins
 - have $C_L=30\text{pF}$ loads,
 - are configured for fast slew rate ($\text{PORTx_PCRn[SRE]}=0$), and
 - are configured for high drive strength ($\text{PORTx_PCRn[DSE]}=1$)
2. input pins
 - have their passive filter disabled ($\text{PORTx_PCRn[PFE]}=0$)

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	1.71	—	mA	7
I _{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	—	0.77	—	mA	8
I _{DD_STOP}	Stop mode current at 3.0 V • @ –40 to 25°C • @ 70°C • @ 105°C	— — —	0.74 2.45 6.61	1.41 11.5 30	mA mA mA	
I _{DD_VLPS}	Very-low-power stop mode current at 3.0 V • @ –40 to 25°C • @ 70°C • @ 105°C	— — —	83 425 1280	435 2000 4000	μA μA μA	
I _{DD_LLS}	Low leakage stop mode current at 3.0 V • @ –40 to 25°C • @ 70°C • @ 105°C	— — —	4.58 30.6 137	19.9 105 500	μA μA μA	9
I _{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V • @ –40 to 25°C • @ 70°C • @ 105°C	— — —	3.0 18.6 84.9	23 43 230	μA μA μA	9
I _{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V • @ –40 to 25°C • @ 70°C • @ 105°C	— — —	2.2 9.3 41.4	5.4 35 128	μA μA μA	
I _{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V • @ –40 to 25°C • @ 70°C • @ 105°C	— — —	2.1 7.6 33.5	9 28 95.5	μA μA μA	
I _{DD_VBAT}	Average current with RTC and 32kHz disabled at 3.0 V • @ –40 to 25°C • @ 70°C • @ 105°C	— — —	0.19 0.49 2.2	0.22 0.64 3.2	μA μA μA	

Table continues on the next page...

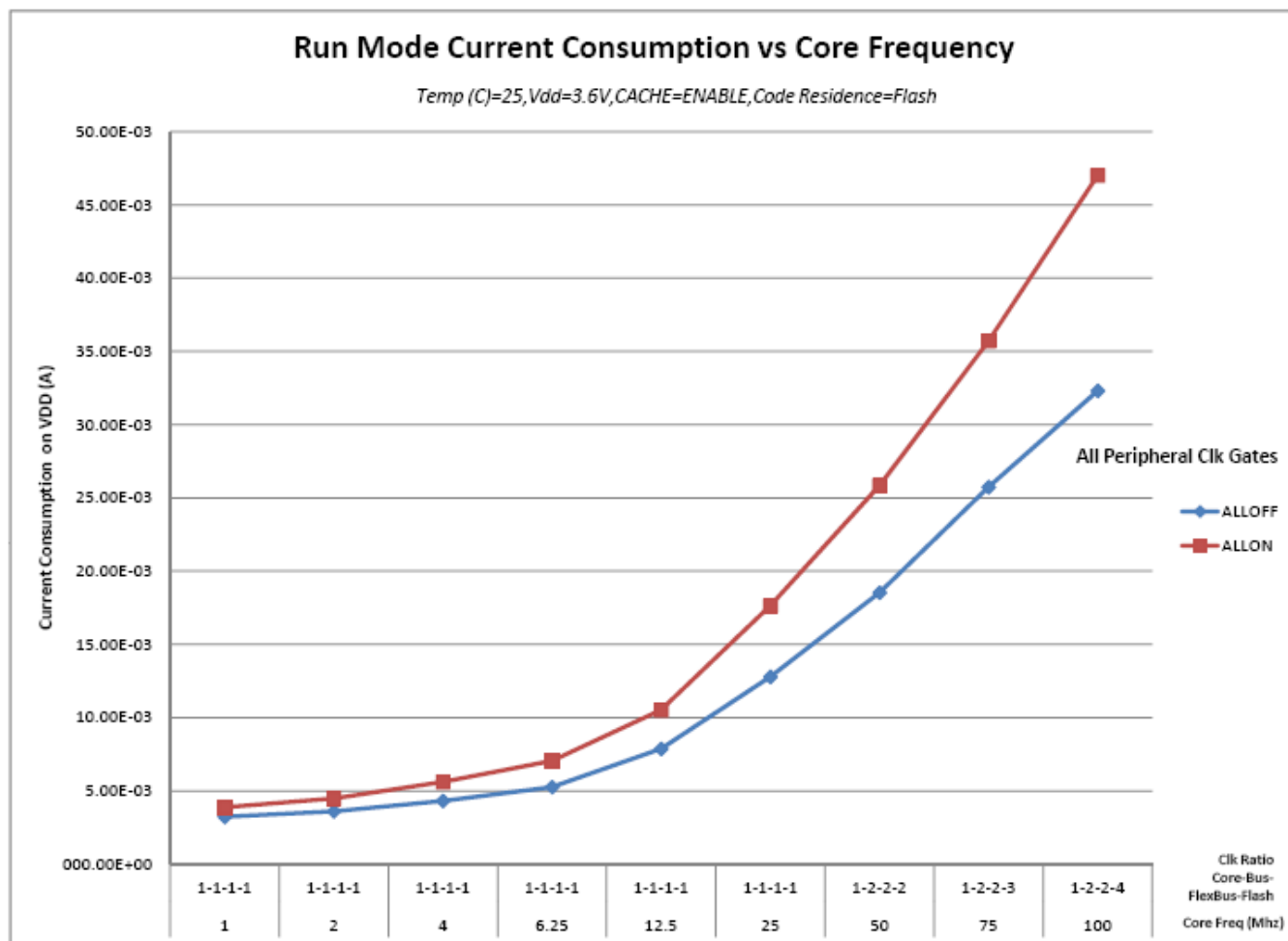


Figure 2. Run mode supply current vs. core frequency

5.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors for 144LQFP and 144MAPBGA

Symbol	Description	Frequency band (MHz)	144LQFP	144MAPBGA	Unit	Notes
V _{RE1}	Radiated emissions voltage, band 1	0.15–50	23	12	dBμV	1, 2
V _{RE2}	Radiated emissions voltage, band 2	50–150	27	24	dBμV	
V _{RE3}	Radiated emissions voltage, band 3	150–500	28	27	dBμV	
V _{RE4}	Radiated emissions voltage, band 4	500–1000	14	11	dBμV	
V _{RE_IEC}	IEC level	0.15–1000	K	K	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

Table 15. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
J_{cyc_fll}	FLL period jitter $f_{DCO} = 48 \text{ MHz}$ $f_{DCO} = 98 \text{ MHz}$	—	180	—	ps	
$t_{fll_acquire}$	FLL target frequency acquisition time	—	—	1	ms	6
PLL						
f_{vco}	VCO operating frequency	48.0	—	100	MHz	
I_{pll}	PLL operating current PLL @ 96 MHz ($f_{osc_hi_1} = 8 \text{ MHz}$, $f_{pll_ref} = 2 \text{ MHz}$, VDIV multiplier = 48)	—	1060	—	μA	7
I_{pll}	PLL operating current PLL @ 48 MHz ($f_{osc_hi_1} = 8 \text{ MHz}$, $f_{pll_ref} = 2 \text{ MHz}$, VDIV multiplier = 24)	—	600	—	μA	7
f_{pll_ref}	PLL reference frequency range	2.0	—	4.0	MHz	
J_{cyc_pll}	PLL period jitter (RMS) $f_{vco} = 48 \text{ MHz}$ $f_{vco} = 100 \text{ MHz}$	—	120	—	ps	8
J_{acc_pll}	PLL accumulated jitter over 1 μs (RMS) $f_{vco} = 48 \text{ MHz}$ $f_{vco} = 100 \text{ MHz}$	—	1350	—	ps	8
D_{lock}	Lock entry frequency tolerance	± 1.49	—	± 2.98	%	
D_{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{pll_ref})$	s	9

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Excludes any oscillator currents that are also consuming power while PLL is in operation.
8. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
9. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

6.3.2 Oscillator electrical specifications

This section provides the electrical characteristics of the module.

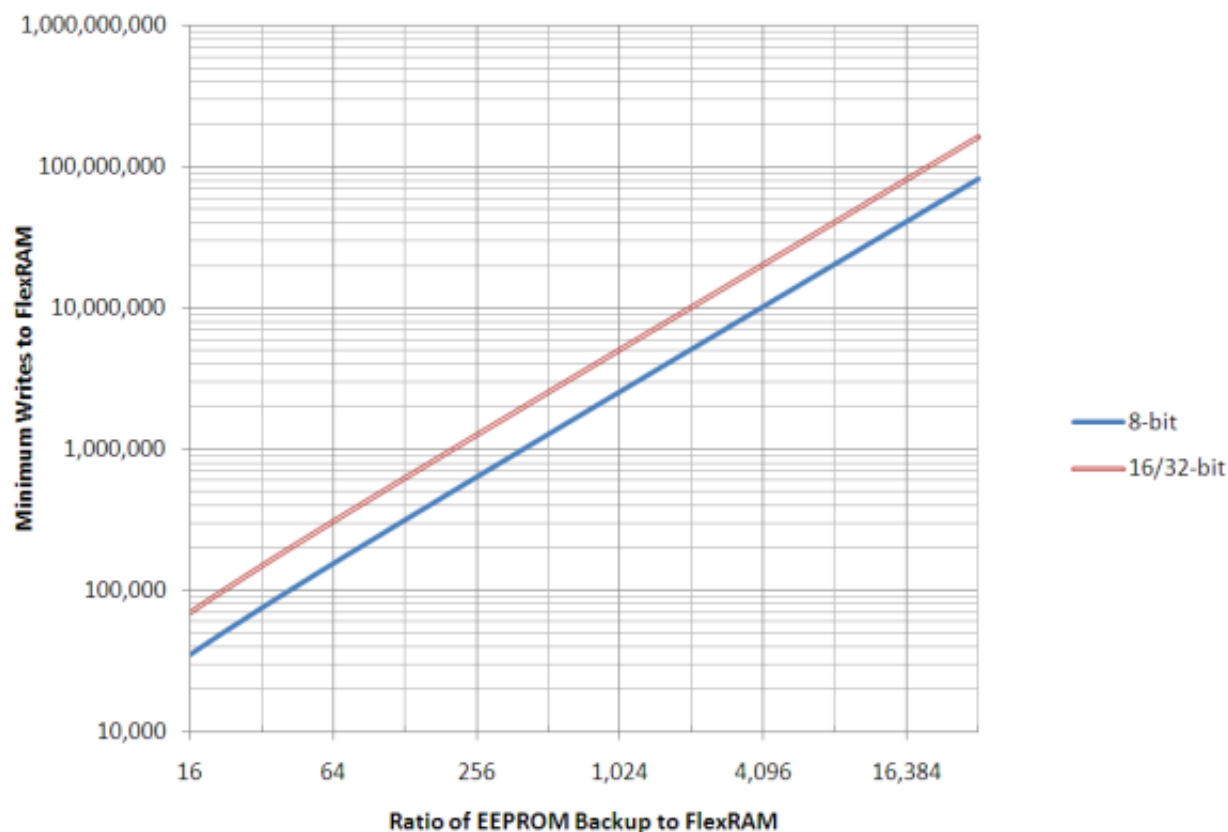


Figure 9. EEPROM backup writes to FlexRAM

6.4.2 EzPort switching specifications

Table 24. EzPort switching specifications

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
EP1	EZP_CK frequency of operation (all commands except READ)	—	$f_{SYS}/2$	MHz
EP1a	EZP_CK frequency of operation (READ command)	—	$f_{SYS}/8$	MHz
EP2	EZP_CS negation to next EZP_CS assertion	$2 \times t_{EZP_CK}$	—	ns
EP3	EZP_CS input valid to EZP_CK high (setup)	5	—	ns
EP4	EZP_CK high to EZP_CS input invalid (hold)	5	—	ns
EP5	EZP_D input valid to EZP_CK high (setup)	2	—	ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5	—	ns
EP7	EZP_CK low to EZP_Q output valid	—	16	ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	—	ns
EP9	EZP_CS negation to EZP_Q tri-state	—	12	ns

Peripheral operating requirements and behaviors

- Specification is valid for all FB_AD[31:0] and $\overline{\text{FB_TA}}$.

Table 26. Flexbus full voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	
	Frequency of operation	—	FB_CLK	MHz	
FB1	Clock period	1/FB_CLK	—	ns	
FB2	Address, data, and control output valid	—	13.5	ns	1
FB3	Address, data, and control output hold	0	—	ns	1
FB4	Data and $\overline{\text{FB_TA}}$ input setup	13.7	—	ns	2
FB5	Data and $\overline{\text{FB_TA}}$ input hold	0.5	—	ns	2

- Specification is valid for all FB_AD[31:0], $\overline{\text{FB_BE/BWE}}_n$, $\overline{\text{FB_CS}}_n$, $\overline{\text{FB_OE}}$, FB_R/W, $\overline{\text{FB_TBST}}$, FB_TSIz[1:0], FB_ALE, and $\overline{\text{FB_TS}}$.
- Specification is valid for all FB_AD[31:0] and $\overline{\text{FB_TA}}$.

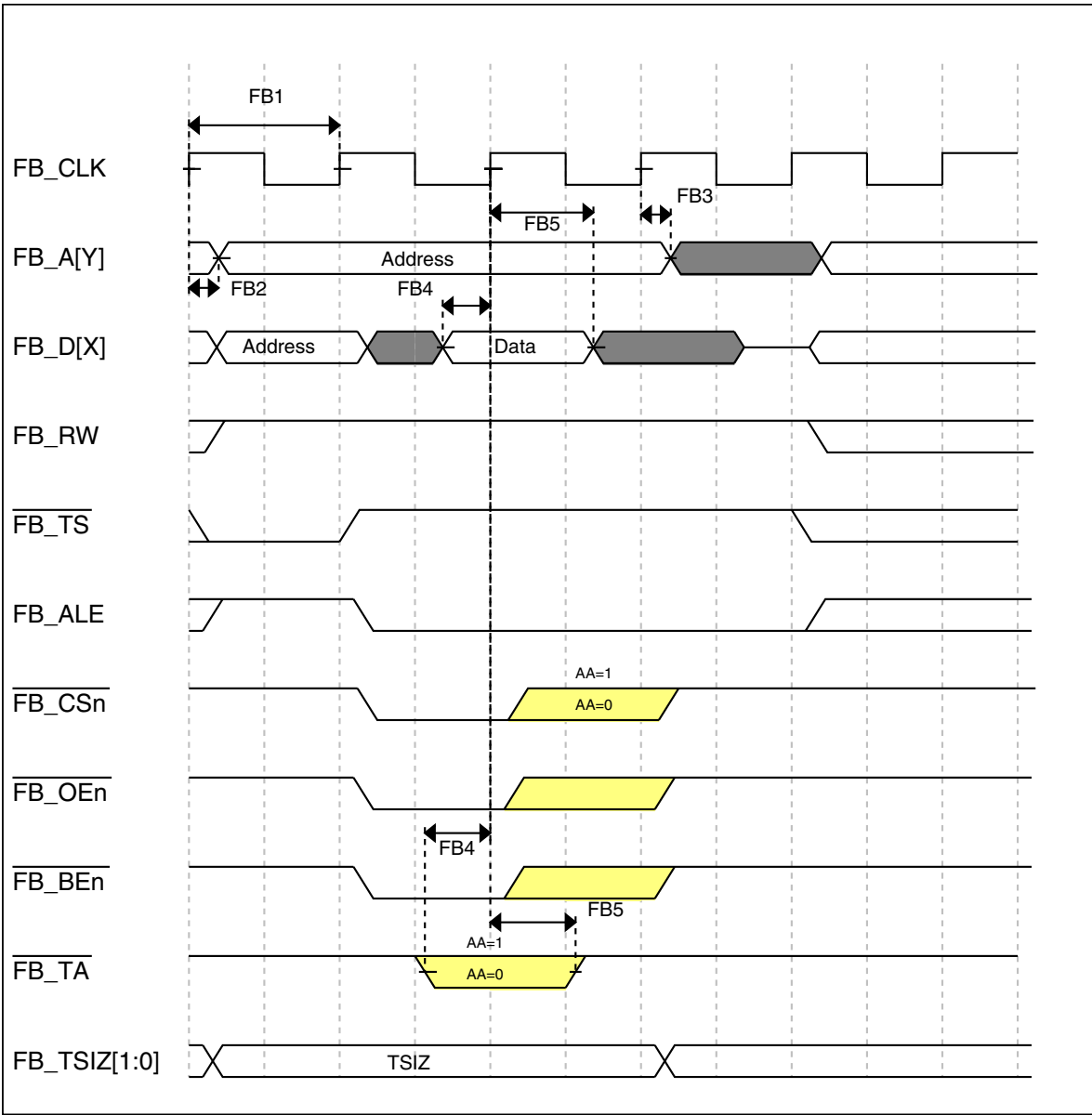


Figure 11. FlexBus read timing diagram

6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in [Table 27](#) and [Table 28](#) are achievable on the differential pins ADCx_DP0, ADCx_DM0, ADCx_DP1, ADCx_DM1, ADCx_DP3, and ADCx_DM3.

The ADCx_DP2 and ADCx_DM2 ADC inputs are connected to the PGA outputs and are not direct device pins. Accuracy specifications for these pins are defined in [Table 29](#) and [Table 30](#).

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

6.6.1.1 16-bit ADC operating conditions

Table 27. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V _{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV _{DDA}	Supply voltage	Delta to V _{DD} (V _{DD} – V _{DDA})	-100	0	+100	mV	2
ΔV _{SSA}	Ground voltage	Delta to V _{SS} (V _{SS} – V _{SSA})	-100	0	+100	mV	2
V _{REFH}	ADC reference voltage high		1.13	V _{DDA}	V _{DDA}	V	
V _{REFL}	ADC reference voltage low		V _{SSA}	V _{SSA}	V _{SSA}	V	
V _{ADIN}	Input voltage	16-bit differential mode - All other modes	V _{REFL} V _{REFL}	— —	31/32 * V _{REFH} V _{REFH}	V	
C _{ADIN}	Input capacitance	16-bit mode 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	
R _{ADIN}	Input resistance		—	2	5	kΩ	
R _{AS}	Analog source resistance	13-bit / 12-bit modes f _{ADCK} < 4 MHz	—	—	5	kΩ	3
f _{ADCK}	ADC conversion clock frequency	≤ 13-bit mode	1.0	—	18.0	MHz	4
f _{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	4
C _{rate}	ADC conversion rate	≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	5

Table continues on the next page...

Table 28. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
f_{ADACK}	ADC asynchronous clock source	- ADLPC = 1, ADHSC = 0 - ADLPC = 1, ADHSC = 1 - ADLPC = 0, ADHSC = 0 - ADLPC = 0, ADHSC = 1	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	$t_{ADACK} = 1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	12-bit modes <12-bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB ⁴	5
DNL	Differential non-linearity	12-bit modes <12-bit modes	— —	±0.7 ±0.2	-1.1 to +1.9 -0.3 to 0.5	LSB ⁴	5
INL	Integral non-linearity	12-bit modes <12-bit modes	— —	±1.0 ±0.5	-2.7 to +1.9 -0.7 to +0.5	LSB ⁴	5
E_{FS}	Full-scale error	12-bit modes <12-bit modes	— —	-4 -1.4	-5.4 -1.8	LSB ⁴	$V_{ADIN} = V_{DDA}$ 5
E_Q	Quantization error	16-bit modes ≤13-bit modes	— —	-1 to 0 —	— ±0.5	LSB ⁴	
ENOB	Effective number of bits	16-bit differential mode - Avg = 32 - Avg = 4 16-bit single-ended mode - Avg = 32 - Avg = 4	12.8 11.9 12.2 11.4	14.5 13.8 13.9 13.1	— — — —	bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	$6.02 \times \text{ENOB} + 1.76$			dB	
THD	Total harmonic distortion	16-bit differential mode - Avg = 32 16-bit single-ended mode - Avg = 32	— —	-94 -85	— —	dB dB	7
SFDR	Spurious free dynamic range	16-bit differential mode - Avg = 32 16-bit single-ended mode - Avg = 32	82 78	95 90	— —	dB dB	7

Table continues on the next page...

Table 31. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
V_H	Analog comparator hysteresis ¹				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOH}	Output high	$V_{DD} - 0.5$	—	—	V
V_{CMPOI}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay ²	—	—	40	μ s
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	μ A
INL	6-bit DAC integral non-linearity	−0.5	—	0.5	LSB ³
DNL	6-bit DAC differential non-linearity	−0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD}-0.6$ V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}/64$

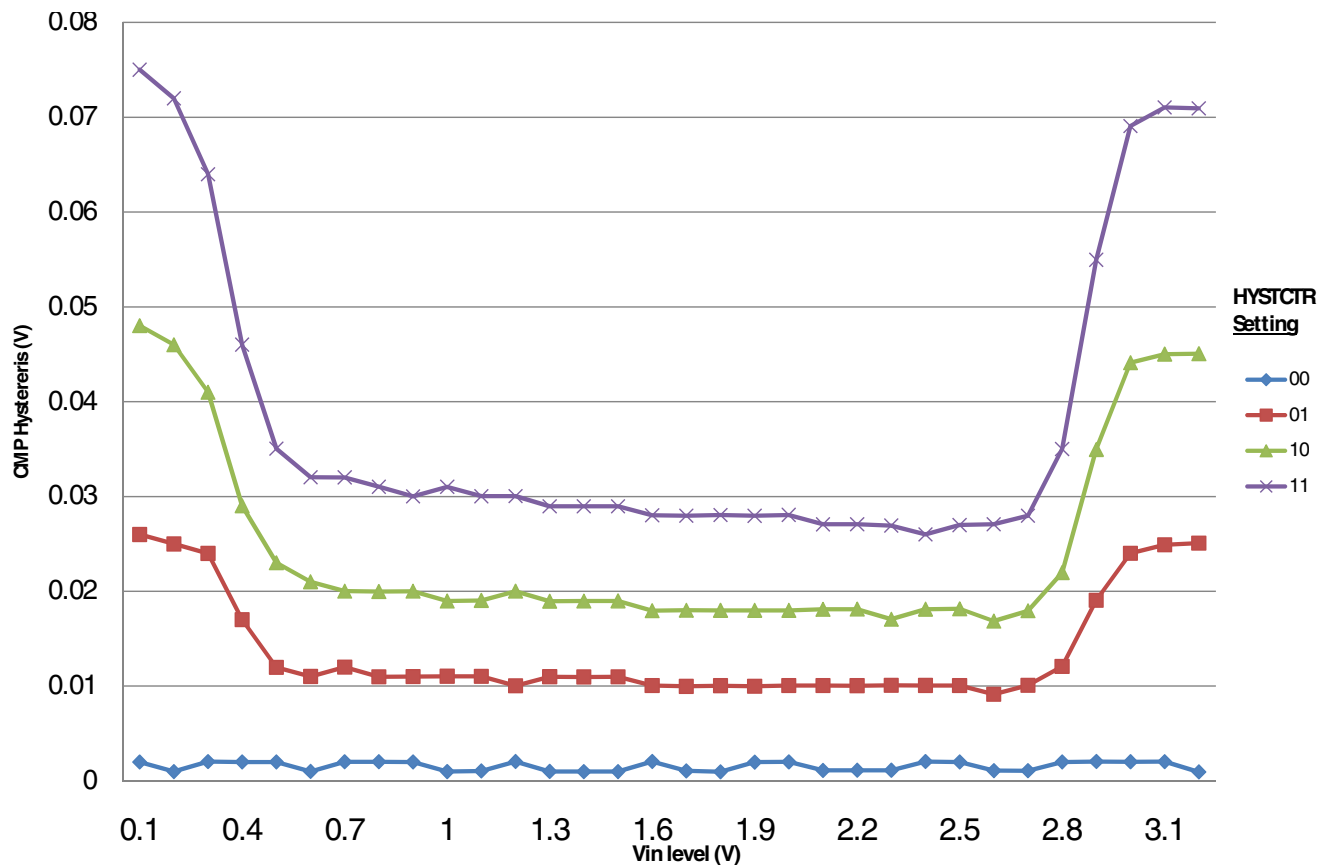


Figure 16. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=0)

Table 35. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim at nominal V_{DDA} and temperature=25C	1.1915	1.195	1.1977	V	
V_{out}	Voltage reference output — factory trim	1.1584	—	1.2376	V	
V_{out}	Voltage reference output — user trim	1.193	—	1.197	V	
V_{step}	Voltage reference trim step	—	0.5	—	mV	
V_{tdrift}	Temperature drift ($V_{max} - V_{min}$ across the full temperature range)	—	—	80	mV	
I_{bg}	Bandgap only current	—	—	80	μA	1
I_{lp}	Low-power buffer current	—	—	360	μA	1
I_{hp}	High-power buffer current	—	—	1	mA	1
ΔV_{LOAD}	Load regulation • current = ± 1.0 mA	—	200	—	μV	1, 2
T_{stup}	Buffer startup time	—	—	100	μs	
V_{vdift}	Voltage drift ($V_{max} - V_{min}$ across the full voltage range)	—	2	—	mV	1

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

Table 36. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_A	Temperature	0	50	$^{\circ}C$	

Table 37. VREF limited-range operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim	1.173	1.225	V	

6.7 Timers

See [General switching specifications](#).

6.8 Communication interfaces

6.8.1 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit usb.org.

6.8.2 USB DCD electrical specifications

Table 38. USB DCD electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V _{DP_SRC}	USB_DP source voltage (up to 250 μ A)	0.5	—	0.7	V
V _{LGC}	Threshold voltage for logic high	0.8	—	2.0	V
I _{DP_SRC}	USB_DP source current	7	10	13	μ A
I _{DM_SINK}	USB_DM sink current	50	100	150	μ A
R _{DM_DWN}	D- pulldown resistance for data pin contact detect	14.25	—	24.8	k Ω
V _{DAT_REF}	Data detect voltage	0.25	0.33	0.4	V

6.8.3 USB VREG electrical specifications

Table 39. USB VREG electrical specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
V _{REGIN}	Input supply voltage	2.7	—	5.5	V	
I _{DDon}	Quiescent current — Run mode, load current equal zero, input supply (V _{REGIN}) > 3.6 V	—	120	186	μ A	
I _{DDstby}	Quiescent current — Standby mode, load current equal zero	—	1.1	10	μ A	
I _{DDoff}	Quiescent current — Shutdown mode - V_{REGIN} = 5.0 V and temperature=25 °C - Across operating voltage and temperature	—	650	—	nA	
		—	—	4	μ A	
I _{LOADrun}	Maximum load current — Run mode	—	—	120	mA	
I _{LOADstby}	Maximum load current — Standby mode	—	—	1	mA	
V _{Reg33out}	Regulator output voltage — Input supply (V _{REGIN}) > 3.6 V - Run mode - Standby mode	3	3.3	3.6	V	
		2.1	2.8	3.6	V	
V _{Reg33out}	Regulator output voltage — Input supply (V _{REGIN}) < 3.6 V, pass-through mode	2.1	—	3.6	V	2
C _{OUT}	External output capacitor	1.76	2.2	8.16	μ F	
ESR	External output capacitor equivalent series resistance	1	—	100	m Ω	

Table continues on the next page...

**Table 39. USB VREG electrical specifications
(continued)**

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
I_{LIM}	Short circuit current	—	290	—	mA	

1. Typical values assume VREGIN = 5.0 V, Temp = 25 °C unless otherwise stated.

2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to I_{Load} .

6.8.4 CAN switching specifications

See [General switching specifications](#).

6.8.5 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 40. Master mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	25	MHz	
DS1	DSPI_SCK output cycle time	$2 \times t_{BUS}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{SCK}/2) - 2$	$(t_{SCK}/2) + 2$	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	$(t_{BUS} \times 2) - 2$	—	ns	1
DS4	DSPI_SCK to DSPI_PCSn invalid delay	$(t_{BUS} \times 2) - 2$	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	0	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	14	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].

2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

Table 44. I²C timing (continued)

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
Fall time of SDA and SCL signals	t_f	—	300	20 + 0.1C _b ⁵	300	ns
Set-up time for STOP condition	t_{SU} ; STO	4	—	0.6	—	μs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	μs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum t_{HD}; DAT must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
3. Input signal Slew = 10 ns and Output Load = 50 pF
4. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
5. A Fast mode I²C bus device can be used in a Standard mode I²C bus system, but the requirement t_{SU}; DAT ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line t_{rmax} + t_{SU}; DAT = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification) before the SCL line is released.
6. C_b = total capacitance of the one bus line in pF.

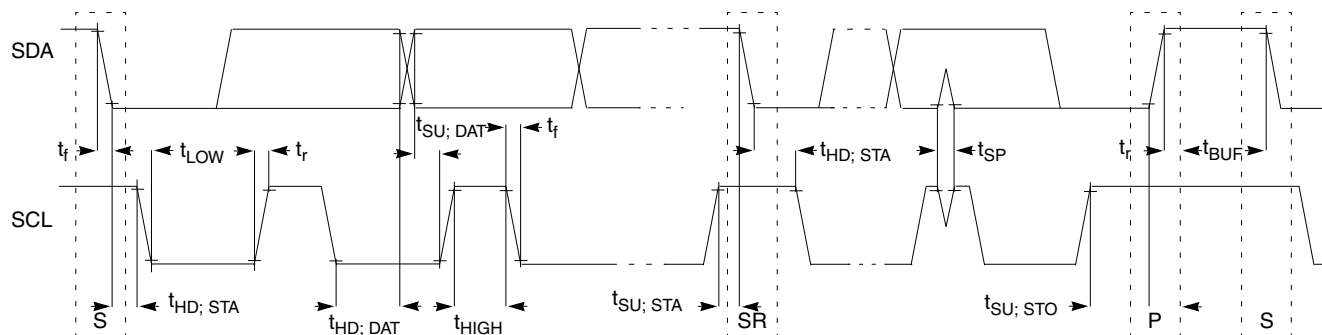


Figure 24. Timing definition for fast and standard mode devices on the I²C bus

6.8.8 UART switching specifications

See [General switching specifications](#).

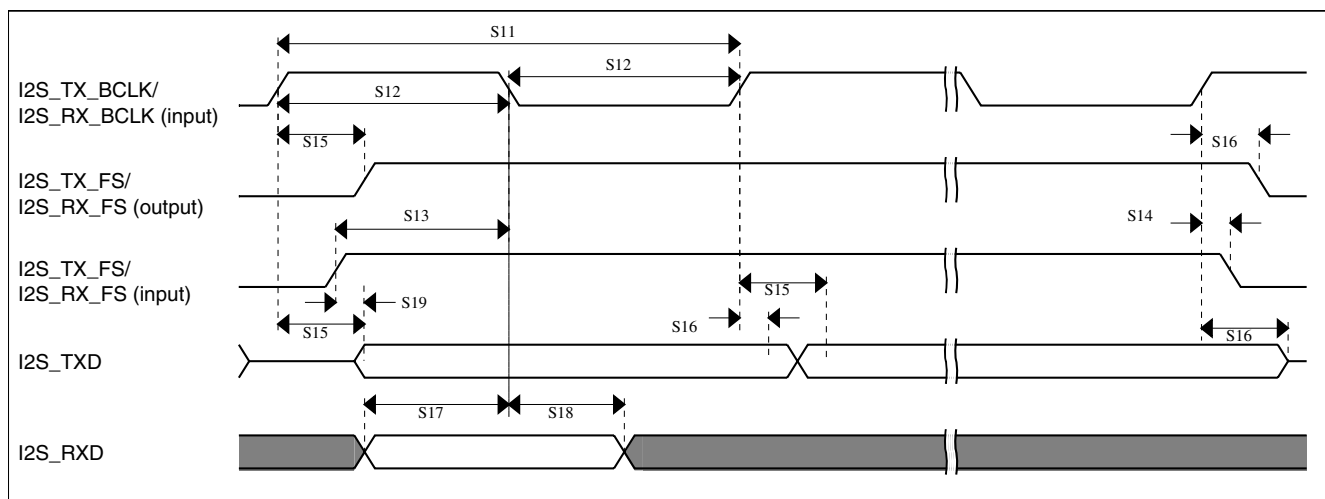


Figure 29. I2S/SAI timing — slave modes

6.8.10.3 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Table 50. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	45	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

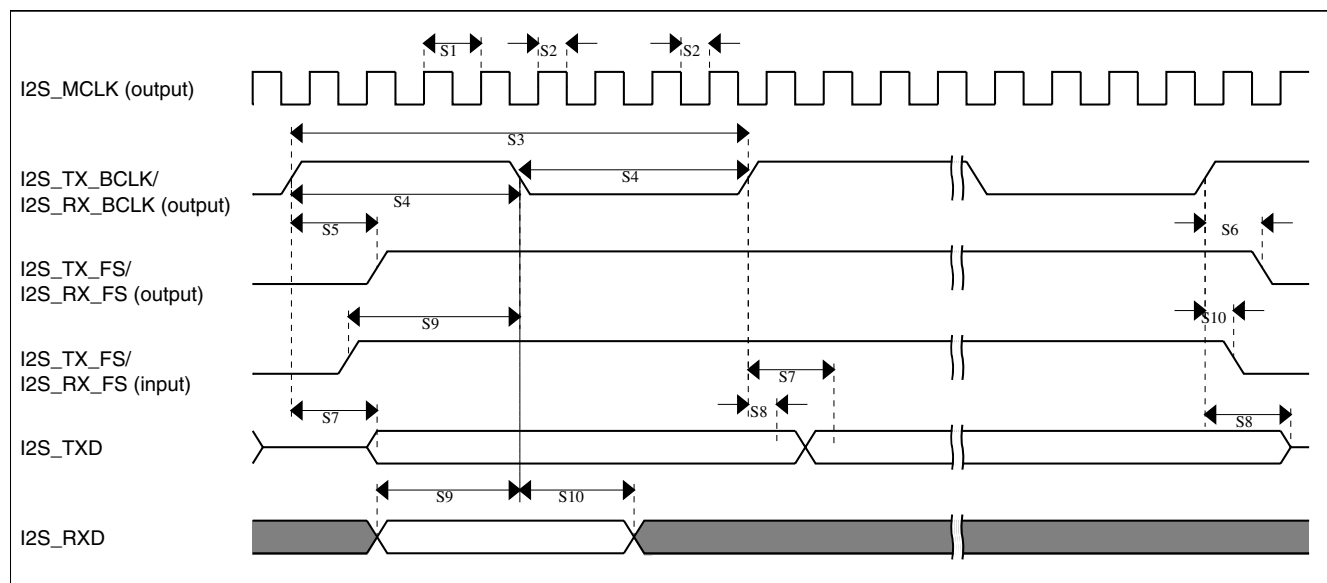


Figure 30. I2S/SAI timing — master modes

Table 51. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	3	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	63	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
15	G3	PTE12	DISABLED		PTE12			I2S0_TX_ BCLK	FB_AD0			
16	E6	VDD	VDD	VDD								
17	F7	VSS	VSS	VSS								
18	H3	VSS	VSS	VSS								
19	H1	USB0_DP	USB0_DP	USB0_DP								
20	H2	USB0_DM	USB0_DM	USB0_DM								
21	G1	VOUT33	VOUT33	VOUT33								
22	G2	VREGIN	VREGIN	VREGIN								
23	J1	ADC0_DP1	ADC0_DP1	ADC0_DP1								
24	J2	ADC0_DM1	ADC0_DM1	ADC0_DM1								
25	K1	ADC1_DP1	ADC1_DP1	ADC1_DP1								
26	K2	ADC1_DM1	ADC1_DM1	ADC1_DM1								
27	L1	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DP/ ADC0_DP0/ ADC1_DP3								
28	L2	PGA0_DM/ ADC0_DM0/ ADC1_DM3	PGA0_DM/ ADC0_DM0/ ADC1_DM3	PGA0_DM/ ADC0_DM0/ ADC1_DM3								
29	M1	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DP/ ADC1_DP0/ ADC0_DP3								
30	M2	PGA1_DM/ ADC1_DM0/ ADC0_DM3	PGA1_DM/ ADC1_DM0/ ADC0_DM3	PGA1_DM/ ADC1_DM0/ ADC0_DM3								
31	H5	VDDA	VDDA	VDDA								
32	G5	VREFH	VREFH	VREFH								
33	G6	VREFL	VREFL	VREFL								
34	H6	VSSA	VSSA	VSSA								
35	K3	ADC1_SE16/ CMP2_IN2/ ADC0_SE22	ADC1_SE16/ CMP2_IN2/ ADC0_SE22	ADC1_SE16/ CMP2_IN2/ ADC0_SE22								
36	J3	ADC0_SE16/ CMP1_IN2/ ADC0_SE21	ADC0_SE16/ CMP1_IN2/ ADC0_SE21	ADC0_SE16/ CMP1_IN2/ ADC0_SE21								
37	M3	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18								
38	L3	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23								
39	L4	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23								