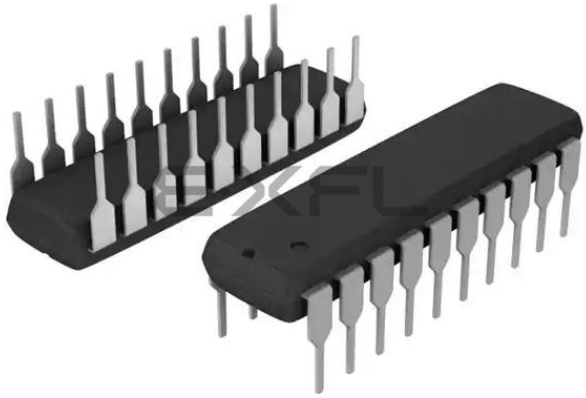


Welcome to E-XFL.COM

Understanding Embedded - PLDs (Programmable Logic Devices)

Embedded - PLDs, or Programmable Logic Devices, are a type of digital electronic component used to build reconfigurable digital circuits. Unlike fixed-function logic devices, PLDs can be programmed to perform specific functions by the user. This flexibility allows designers to customize the logic to meet the exact needs of their applications, making PLDs a crucial component in modern embedded systems.

Applications of Embedded - PLDs (Programmable Logic Devices)

The versatility of PLDs makes them suitable for a wide range of applications. In consumer electronics, PLDs are used to enhance the functionality and performance of

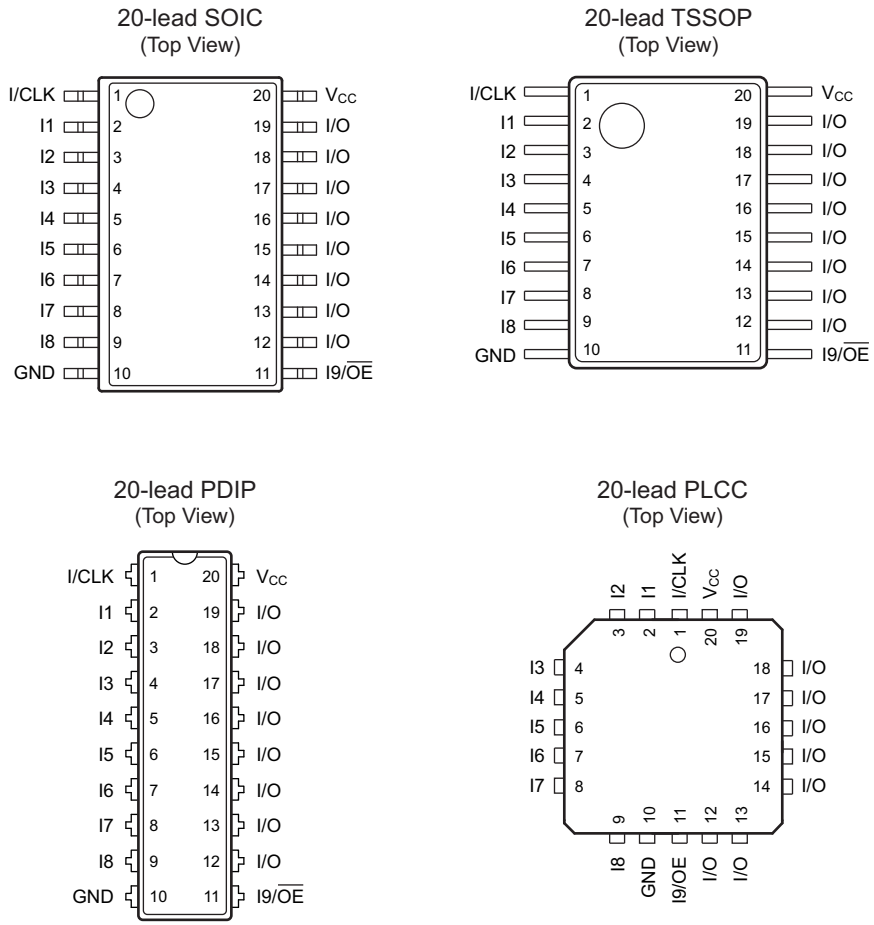
Details	
Product Status	Active
Programmable Type	EE PLD
Number of Macrocells	8
Voltage - Input	5V
Speed	15 ns
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atf16v8bql-15pu

1. Pin Configurations and Pinouts

Table 1-1. Pin Configurations

Pin Name	Function
CLK	Clock
GND	Ground
I	Logic Inputs
I/O	Bi-directional Buffers
$\overline{OE}$	Output Enable
V_{CC}	+5V Power Supply

Figure 1-1. Pinouts



Note: Drawings are not to scale.

3.4 DC Characteristics

Table 3-3. DC Characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{IL}	Input or I/O Low Leakage Current	$0 \le V_{IN} \le V_{IL}$(Max)			-35	-100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5 \le V_{IN} \le V_{CC}$				10	µA
I_{CC}	Power Supply Current, Standby	V_{CC} = Max V_{IN} = Max, Outputs Open	B-10		55	95	mA
			B-15		50	80	
			BQL-15		5	15	
I_{CC2}	Clocked Power Supply Current	V_{CC} = Max, Outputs Open f = 15MHz	B-10		60	100	mA
			B-15		55	95	
			BQL-15		20	40	
I_{OS}[1]	Output Short Circuit Current	V_{OUT} = 0.5 V				-130	mA
V_{IL}	Input Low Voltage			-0.5		0.8	V
V_{IH}	Input High Voltage			2.0		V_{CC} + 0.75	V
V_{OL}	Output High Voltage	$V_{IN} = V_{IH}$ or V_{IL} V_{CC} = Min	I_{OL} = 24mA			0.5	V
V_{OH}	Output High Voltage	$V_{IN} = V_{IH}$ or V_{IL} V_{CC} = Min	I_{OH} = -4.0 mA	2.4			V

Note: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30s.

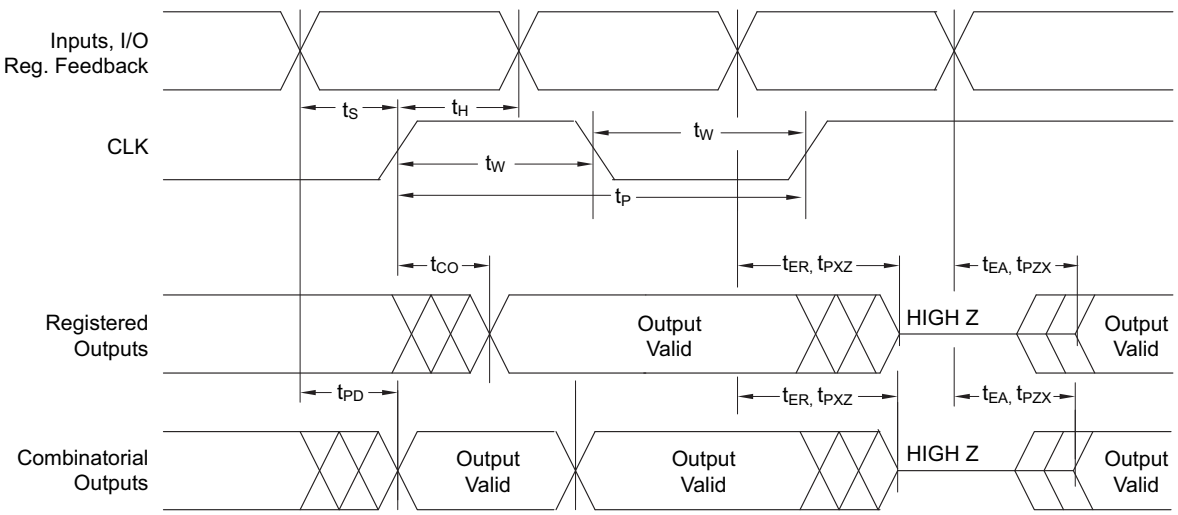
3.5 AC Characteristics

Table 3-4. AC Characteristics[1]

Symbol	Parameter		-10		-15		Units
			Min	Max	Min	Max	
t_{PD}	Input or Feedback to Non-Registered Output	8 outputs switching	3	10	3	15	ns
t_{CF}	Clock to Feedback			6		8	ns
t_{CO}	Clock to Output		2	7	2	10	ns
t_S	Input or Feedback Setup Time		7.5		12		ns
t_H	Hold Time		0		0		ns
t_P	Clock Period		12		16		ns
t_W	Clock Width		6		8		ns
f_{MAX}	External Feedback $1/(t_S + t_{CO})$			68		45	MHz
	Internal Feedback $1/(t_S + t_{CF})$			74		50	
	No Feedback $1/(t_P)$			83		62	
t_{EA}	Input to Output Enable — Product Term		3	10	3	15	ns
t_{ER}	Input to Output Disable — Product Term		2	10	2	15	ns
t_{PZX}	$\overline{OE}$ pin to Output Enable		2	10	2	15	ns
t_{PXZ}	$\overline{OE}$ pin to Output Disable		1.5	10	1.5	15	ns

Note: 1. See ordering information for valid part numbers and speed grades.

Figure 3-1. AC Waveforms[3.6]

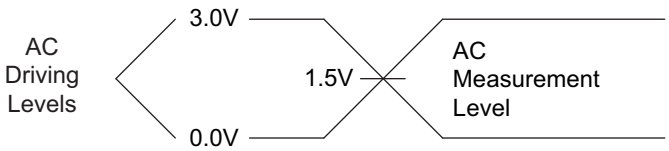


Note 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V 3.0V, unless otherwise specified.

3.6 Input Test Waveforms

3.6.1 Input Test Waveforms and Measurement Levels

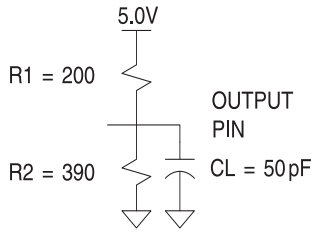
Figure 3-2. Input Test Waveforms and Measurement Levels



t_R, t_F < 5ns (10% to 90%)

3.6.2 Output Test Loads (Commercial)

Figure 3-3. Output Test Loads



C_L includes Test fixture and Probe capacitance

3.7 Power-up Reset

The registers in the ATF16V8B(QL) are designed to reset during power-up. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be reset to the low state. As a result, the registered output state will always be high on power-up.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic,
2. After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and
3. The clock must remain stable during t_{PR}.

Figure 3-4. Power-up Reset Waveforms

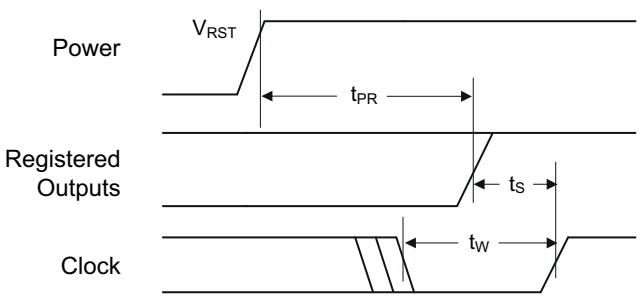


Table 3-5. Power-up Reset Parameters

Parameter	Description	Typ	Max	Units
t_{PR}	Power-up Reset Time	600	1,000	ns
V_{RST}	Power-up Reset Voltage	3.8	4.5	V

3.8 Preload of Registered Outputs

The ATF16V8B(QL) device registers are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file with vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically by most of the approved programmers after the programming.

4. Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF16V8B(QL) fuse patterns. Once programmed, fuse verify and preload are inhibited. However, the 64-bit User Signature remains accessible.

The security fuse should be programmed last, as its effect is immediate.

5. Electronic Signature Word

There are 64 bits of programmable memory that are always available to the user, even if the device is secured. These bits can be used for user-specific data.

6. Programming/Erasing

Programming/erasing is performed using standard PLD programmers.

7. Input and I/O Pull-ups

All ATF16V8B(QL) family members have internal input and I/O pull-up resistors. Therefore, whenever inputs or I/Os are not being driven externally, they will float to V_{CC}. This ensures that all logic array inputs are at known states. These are relatively weak active pull-ups that can easily be over driven by TTL-compatible drivers (see input and I/O diagrams below).

Figure 7-1. Input Diagram

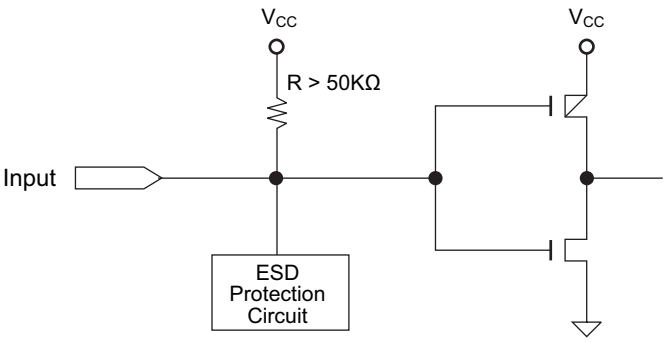
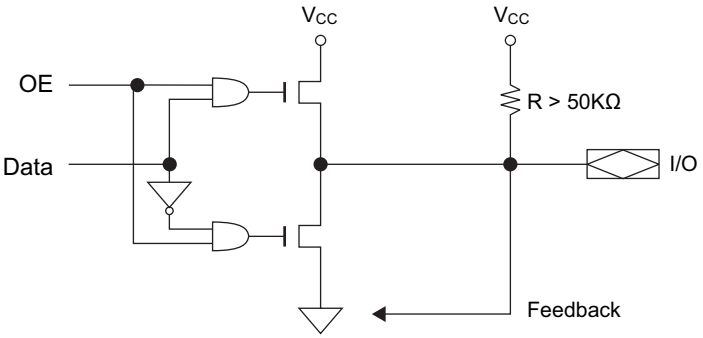


Figure 7-2. I/O Diagram



8. Functional Logic Diagram Description

The logic option and functional diagrams describe the ATF16V8B(QL) architecture. Eight configurable macrocells can be configured as a registered output, combinatorial I/O, combinatorial output, or dedicated input.

The ATF16V8B(QL) can be configured in one of three different modes. Each mode makes the ATF16V8B(QL) look like a different device. Most PLD compilers can choose the right mode automatically. The user can also force the selection by supplying the compiler with a mode selection. The determining factors would be the usage of register versus combinatorial outputs and dedicated outputs versus outputs with output enable control.

The ATF16V8B(QL) universal architecture can be programmed to emulate many 20-pin PAL devices. These architectural subsets can be found in each of the configuration modes described in the following pages. The user can download the listed subset device JEDEC programming file to the PLD programmer, and the ATF16V8B(QL) can be configured to act like the chosen device. Check with your programmer manufacturer for this capability.

Unused product terms are automatically disabled by the compiler to decrease power consumption. A security fuse, when programmed, protects the content of the ATF16V8B(QL). Eight bytes (64 fuses) of User Signature are accessible to the user for purposes such as storing project name, part number, revision, or date. The User Signature is accessible regardless of the state of the security fuse.

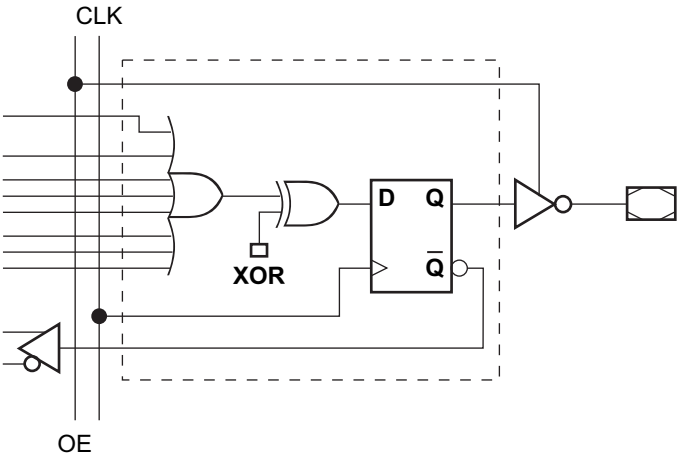
9. Software Support

Atmel WinCUPL is a free tool, available on Atmel's web site and can be used to design in all members of the ATF16V8B(QL) family of SPLDs. The below table lists the Atmel WinCUPL device mnemonics for the different macrocell configuration modes.

Table 9-1. Compiler Mode Selection

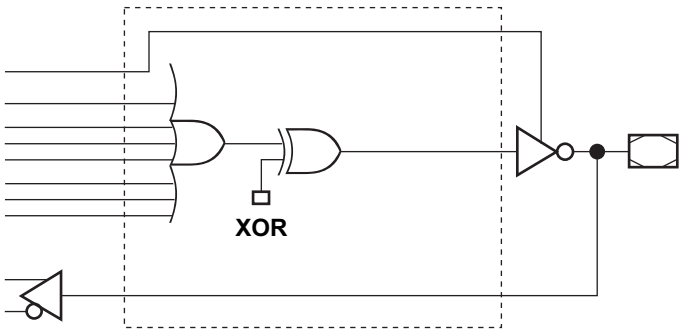
	Registered	Complex	Simple	Auto Select
CUPL, Atmel WinCUPL	G16V8MS	G16V8MA	G16V8AS	G16V8

Figure 10-1. Registered Configuration for Registered Mode[1][2]



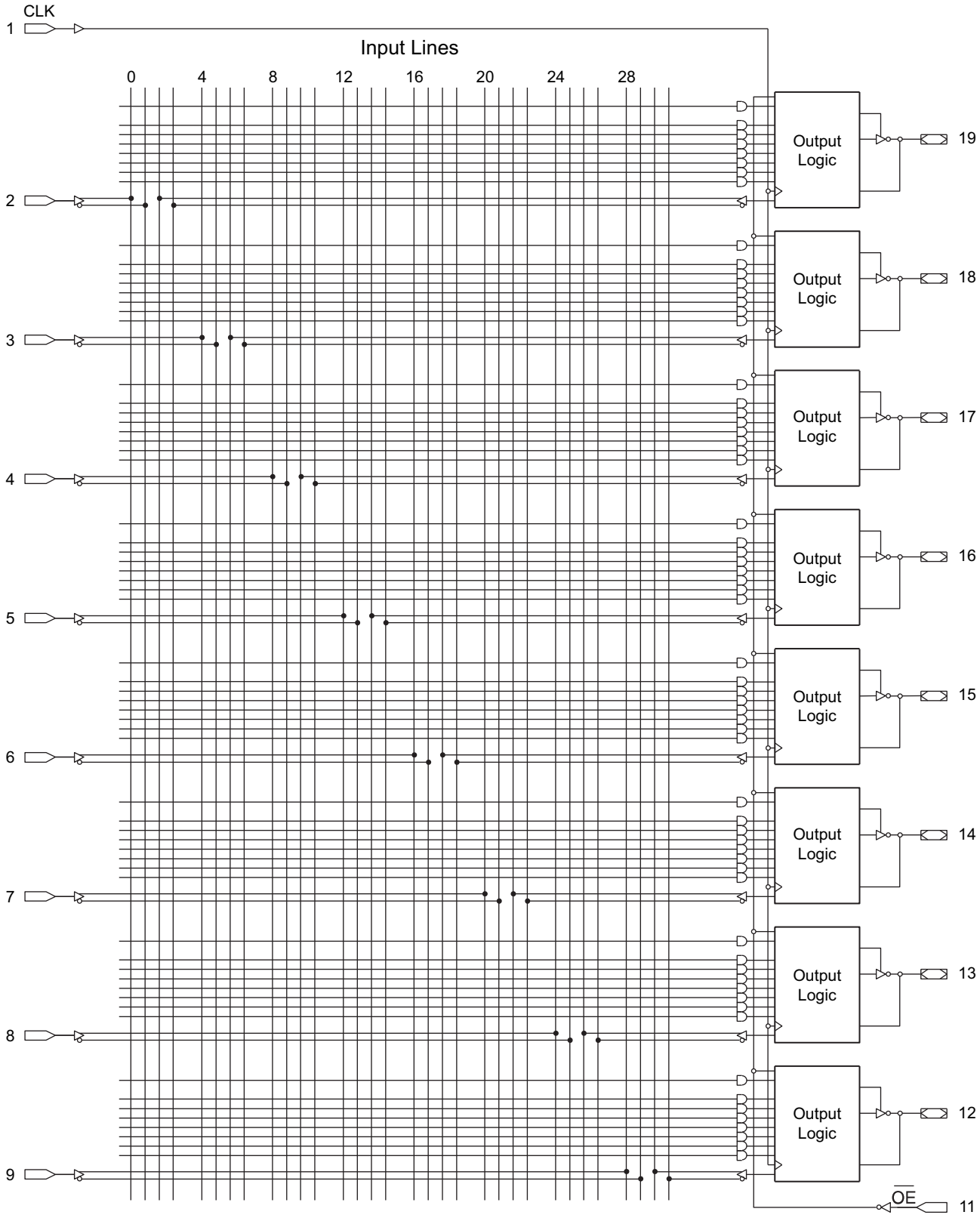
Notes:
1. Pin 1 controls common CLK for the registered outputs. Pin 11 controls common $\overline{OE}$ for the registered outputs. Pin 1 and Pin 11 are permanently configured as CLK and $\overline{OE}$.
2. The development software configures all the architecture control bits and checks for proper pin usage automatically.

Figure 10-2. Combinatorial Configuration for Registered Mode[1][2]



Notes:
1. Pin 1 and Pin 11 are permanently configured as CLK and $\overline{OE}$.
2. The development software configures all the architecture control bits and checks for proper pin usage automatically.

Figure 10-3. Registered Mode Logic Diagram



10.2 ATF16V8B(QL) Complex Mode

PAL Device Emulation/PAL Replacement. In the complex mode, combinatorial output and I/O functions are possible. Pins 1 and 11 are regular inputs to the array. Pins 13 through 18 have pin feedback paths back to the AND-array, which makes full I/O capability possible. Pins 12 and 19 (outermost macrocells) are outputs only. They do not have input capability. In this mode, each macrocell has seven product terms going to the sum term and one product term enabling the output.

Combinatorial applications with an OE requirement will make the compiler select this mode. The following devices can be emulated using this mode:

- 16L8
- 16H8
- 16P8

Figure 10-4. Complex Mode Option

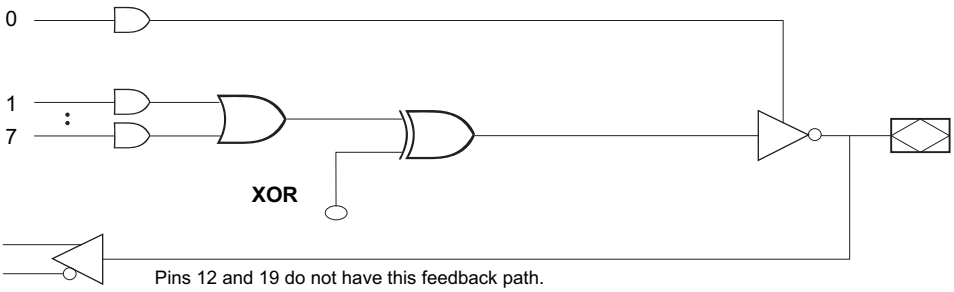
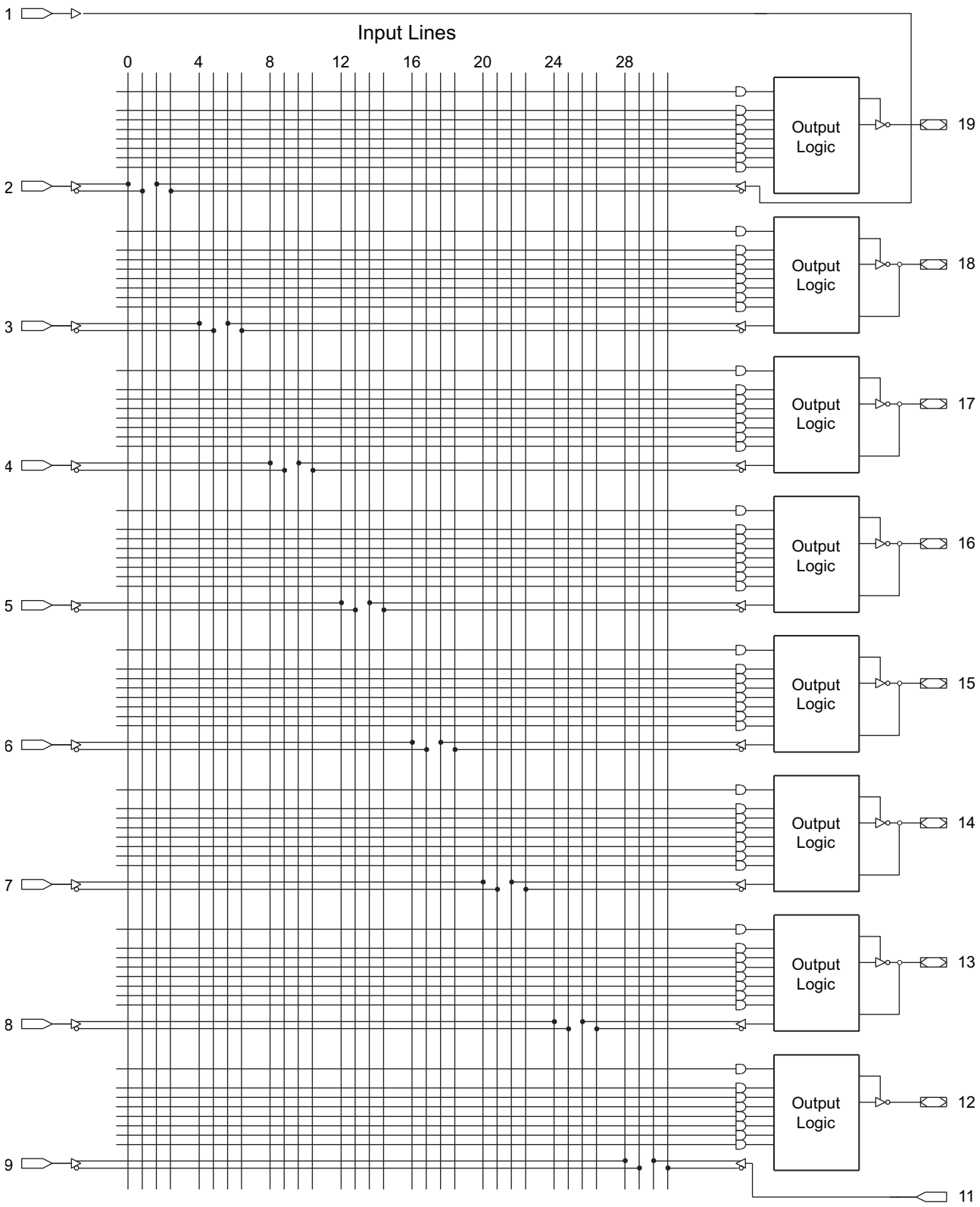


Figure 10-5. Complex Mode Logic Diagram



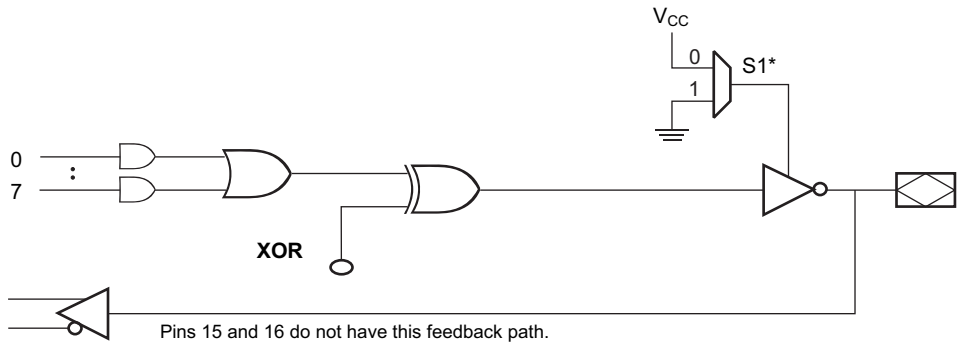
10.3 ATF16V8B(QL) Simple Mode

PAL Device Emulation/PAL Replacement. In the Simple Mode, 8 product terms are allocated to the sum term. Pins 15 and 16 (center macrocells) are permanently configured as combinatorial outputs. Other macrocells can be either inputs or combinatorial outputs with pin feedback to the AND-array. Pins 1 and 11 are regular inputs.

The compiler selects this mode when all outputs are combinatorial without OE control. The following simple PALs can be emulated using this mode:

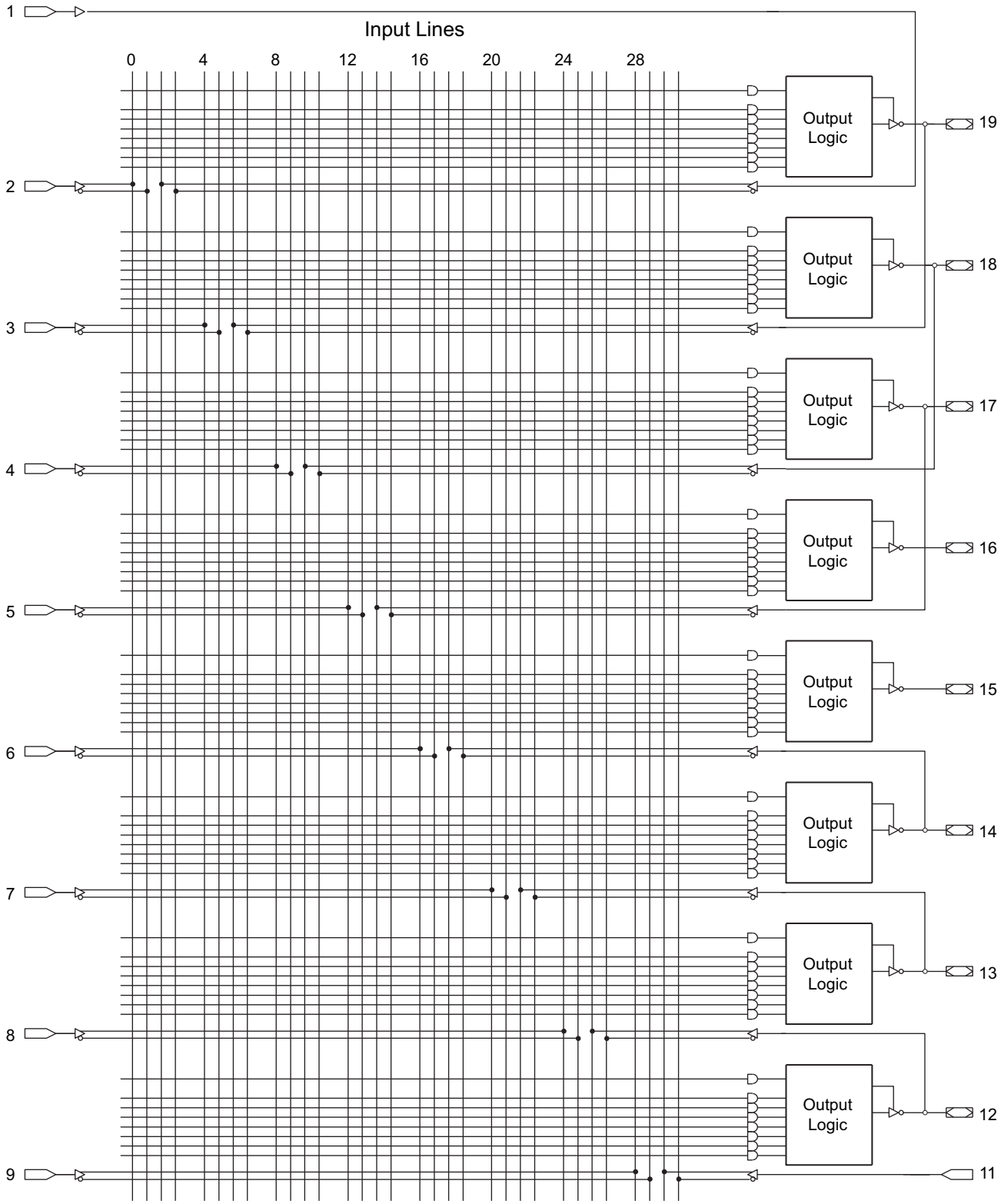
- 10L8
- 10H8
- 10P8
- 12L6
- 12H6
- 12P6
- 14L4
- 14H4
- 14P4
- 16L2
- 16H2
- 16P2

Figure 10-6. Simple Mode Option



* Pins 15 and 16 are always enabled.

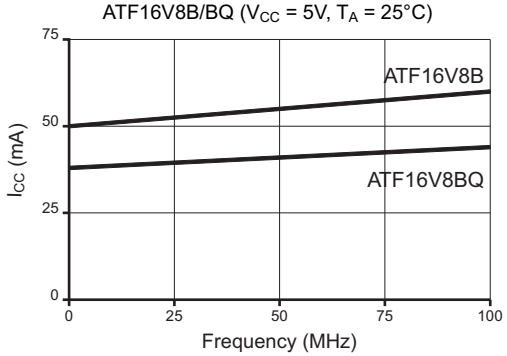
Figure 10-7. Simple Mode Logic Diagram



11. Test Characterization Data

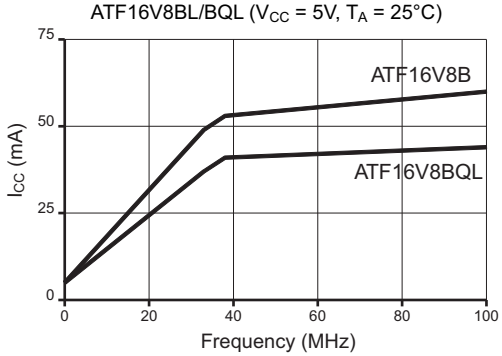
Supply Current vs Input Frequency

ATF16V8B/BQ (V_{CC} = 5V, T_A = 25°C)



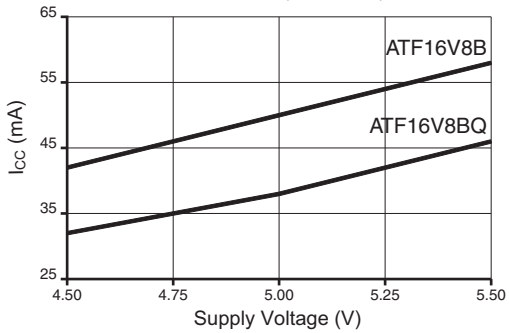
Supply Current vs Input Frequency

ATF16V8BL/BQL (V_{CC} = 5V, T_A = 25°C)



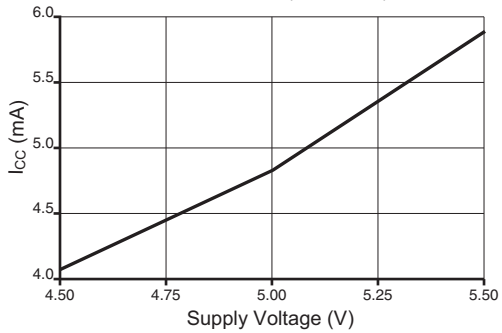
Supply Current vs Supply Voltage

ATF16V8B/BQ (T_A = 25°C)



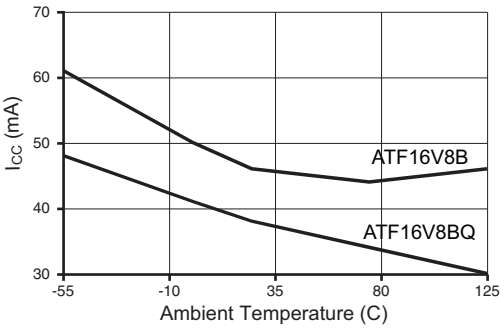
Supply Current vs Supply Voltage

ATF16V8BL/BQL (T_A = 25°C)



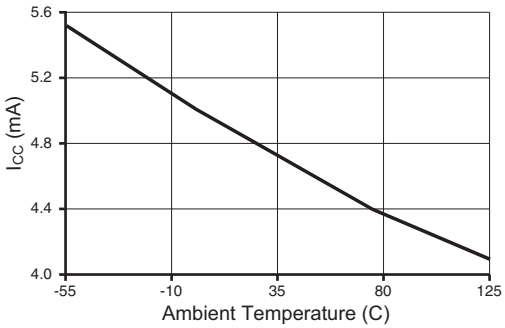
Supply Current vs Ambient Temperature

ATF16V8B/BQ (V_{CC} = 5.0V)



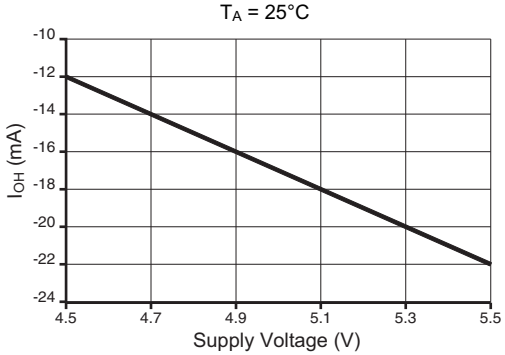
Supply Current vs Ambient Temperature

ATF16V8BL/BQL (V_{CC} = 5.0V)



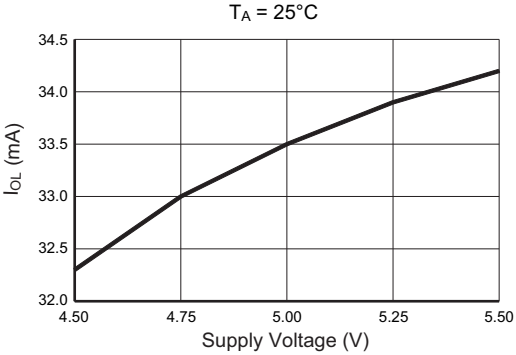
Output Source Current vs Supply Current

T_A = 25°C



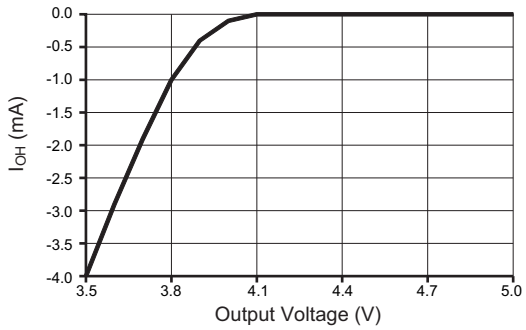
Output Sink Current vs Supply Current

T_A = 25°C



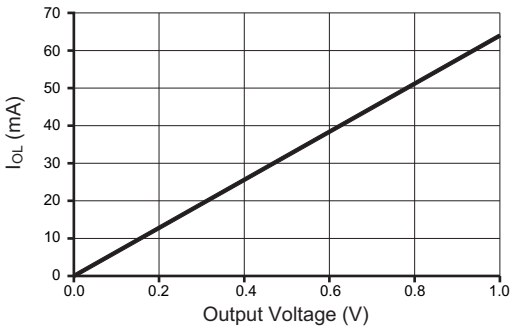
Output Source Current vs Outpute Voltage

(V_{CC} = 5.0V, T_A = 25°C)



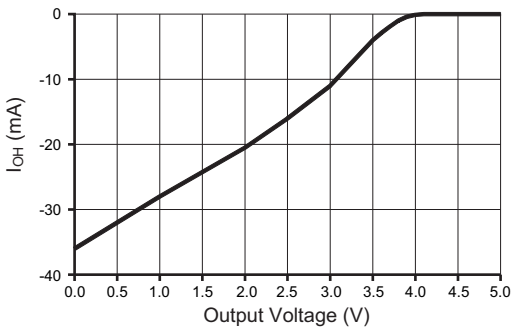
Output Sink Current vs Output Voltage

(V_{CC} = 5.0V, T_A = 25°C)



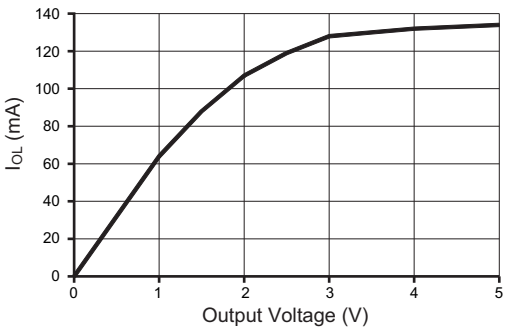
Output Source Current vs Output Voltage

(V_{CC} = 5.0V, T_A = 25°C)



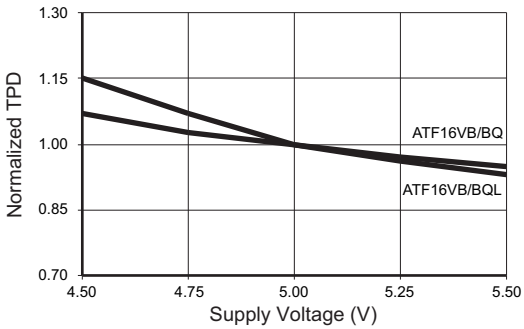
Output Sink Current vs Output Voltage

(V_{CC} = 5.0V, T_A = 25°C)



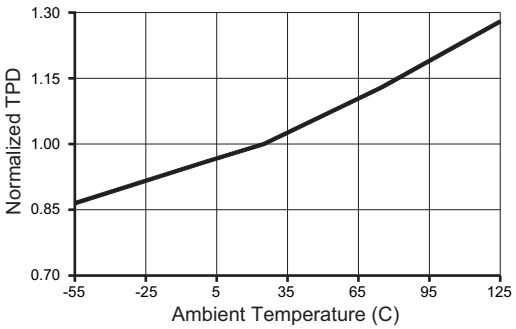
Normalized TPD vs Supply Voltage

(T_A = 25°C)



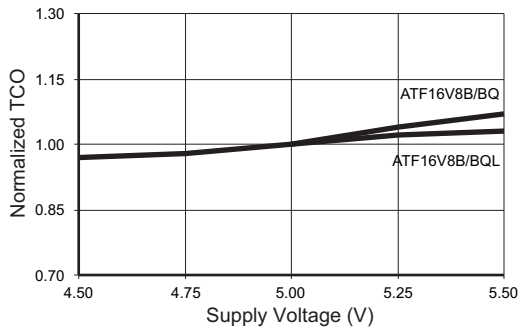
Normalized TPD vs Ambient Temperature

(V_{CC} = 5.0V)



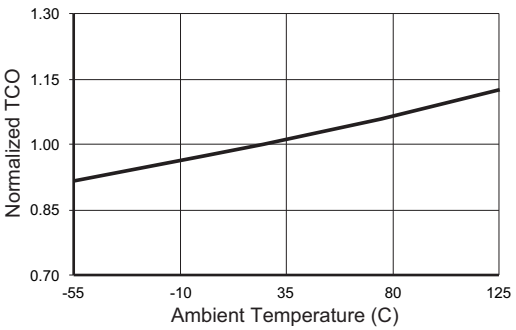
Normalized TCO vs Supply Voltage

(T_A = 25°C)



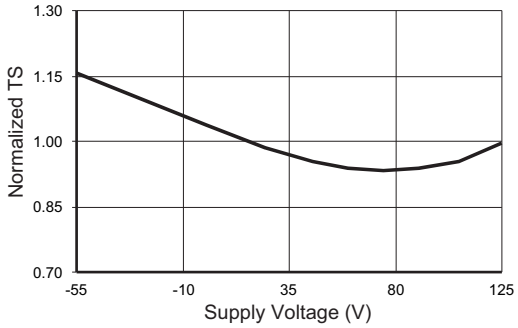
Normalized TCO vs Ambient Temperature

(V_{CC} = 5.0V)



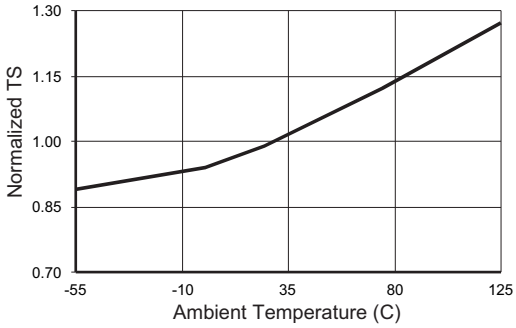
Normalized TS vs Supply Voltage

(T_A = 25°C)



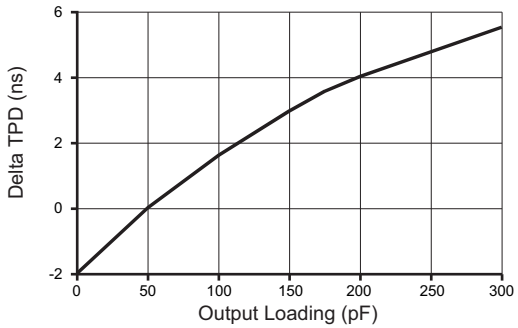
Normalized TS vs Ambient Temperature

(V_{CC} = 5.0V)



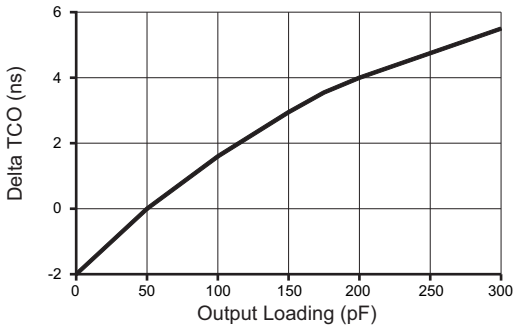
Delta TPD vs Output Loading

(V_{CC} = 5.0V, T_A = 25°C)



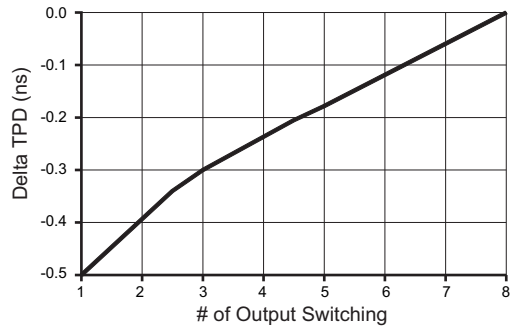
Delta TCO vs Output Loading

(V_{CC} = 5V, T_A = 25°C)



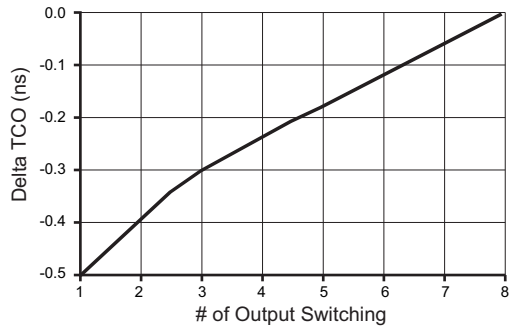
Delta TPD vs # Output Switching

(V_{CC} = 5.0V, T_A = 25°C)



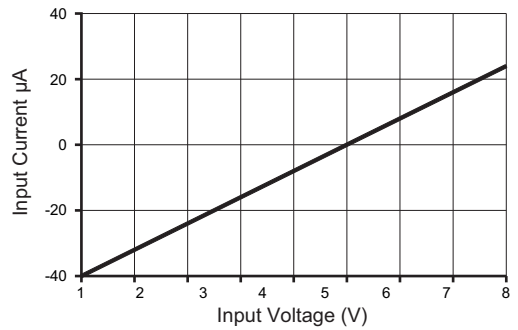
Delta TCO vs # Output Switching

(V_{CC} = 5.0V, T_A = 25°C)



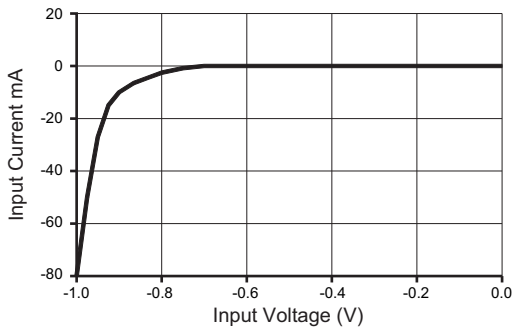
Input Current vs Input Voltage

(V_{CC} = 5.0V, T_A = 25°C)

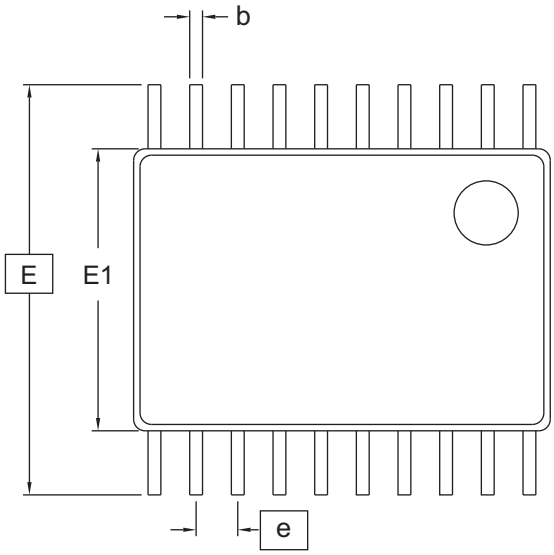


Input Clamp Current vs Input Voltage

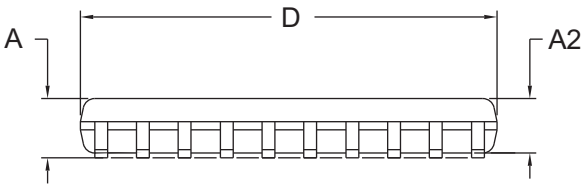
(V_{CC} = 5.0V, T_A = 25°C)



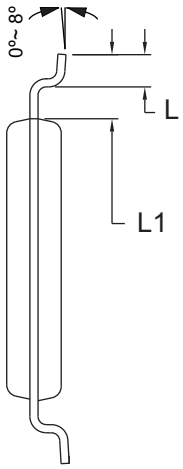
13.2 20X — 20-lead TSSOP



Top View



Side View



End View

COMMON DIMENSIONS
(Unit of Measure = mm)

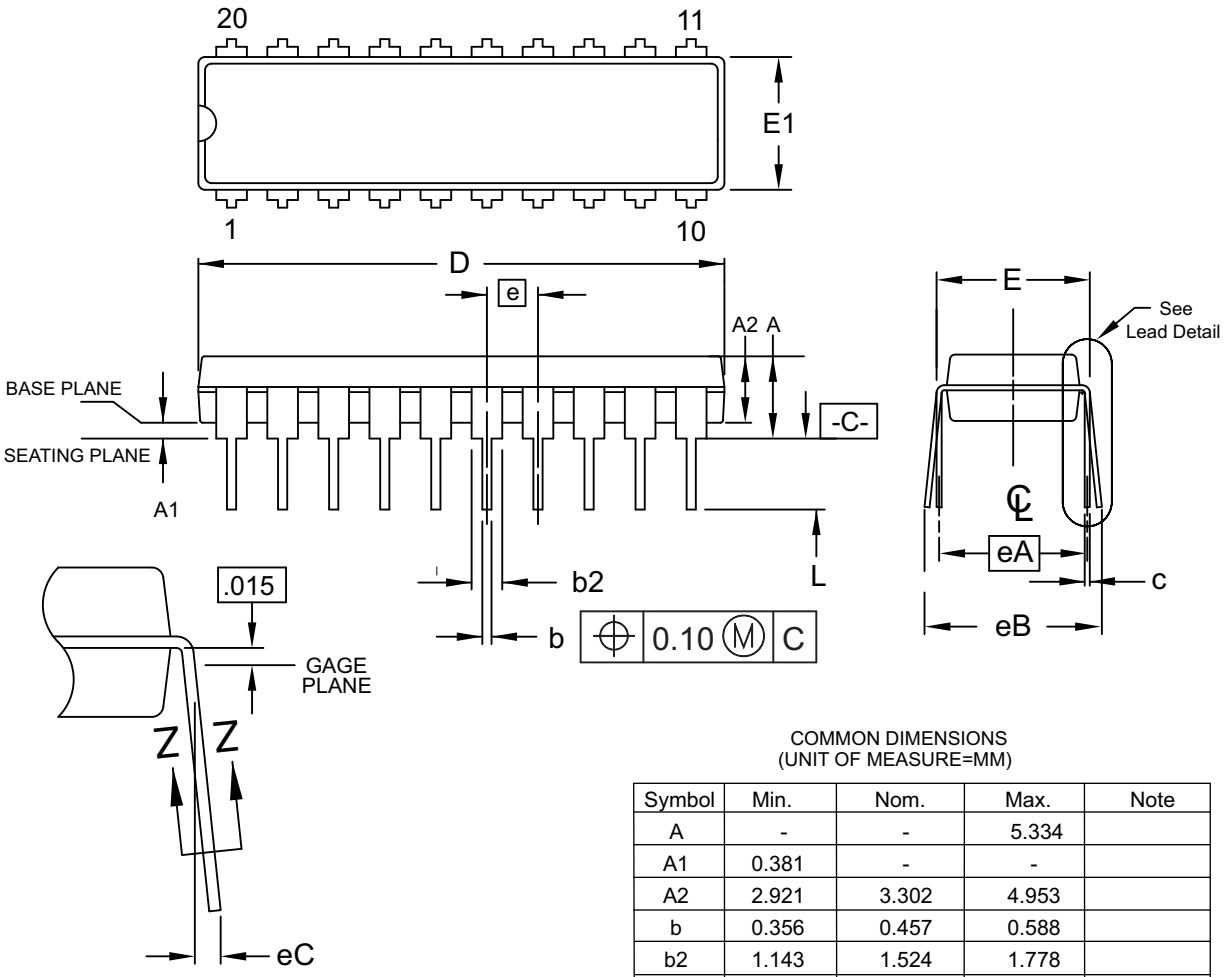
SYMBOL	MIN	NOM	MAX	NOTE
D	6.40	6.50	6.60	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
A	–	–	1.20	
A2	0.80	1.00	1.05	
b	0.19	–	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		

Notes:
1. This drawing is for general information only. Please refer to JEDEC Drawing MO-153, Variation AC, for additional information.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
5. Dimension D and E1 to be determined at Datum Plane H.

09/26/11

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 20X, 20-lead 4.4 x 6.5 mm Body, 0.65 mm Lead Pitch, Thin Shrink Small Outline Package (TSSOP)	**GPC** TLN	**DRAWING NO.** 20X	**REV.** D

13.3 20P3 — 20-lead PDIP



Lead Detail

COMMON DIMENSIONS
(UNIT OF MEASURE=MM)

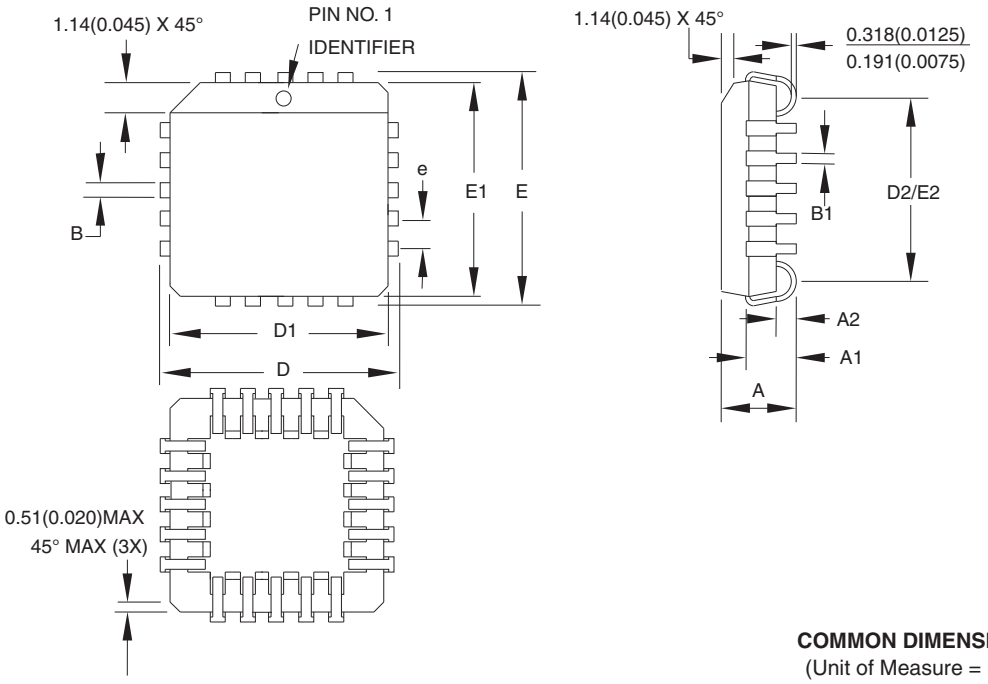
Symbol	Min.	Nom.	Max.	Note
A	-	-	5.334	
A1	0.381	-	-	
A2	2.921	3.302	4.953	
b	0.356	0.457	0.588	
b2	1.143	1.524	1.778	
c	0.203	0.254	0.356	
D	24.892	26.162	26.924	Note 2
E	7.620	7.874	8.255	
E1	6.096	6.350	7.112	Note 2
L	2.921	3.302	3.810	
e	2.54 BSC			
eA	7.62 BSC			
eB	-	-	10.922	
eC	0.000	-	1.524	

Notes:
1. This package conforms to JEDEC reference MS-001, Variation AD.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

1/6/12

Atmel	Package Drawing Contact: packagedrawings@atmel.com	TITLE **20P3**, 20-lead, 0.300”/7.62 mm Wide Plastic Dual Inline Package (PDIP)	GPC PQD	DRAWING NO. 20P3	REV. F

13.4 20J — 20-lead PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	9.779	–	10.033	
D1	8.890	–	9.042	Note 2
E	9.779	–	10.033	
E1	8.890	–	9.042	Note 2
D2/E2	7.366	–	8.382	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AA
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102mm) maximum

10/04/01

Atmel	Package Drawing Contact: packagedrawings@atmel.com	TITLE	DRAWING NO.	REV.
		20J, 20-lead, Plastic J-leaded Chip Carrier (PLCC)	20J	B

14. Revision History

Doc. Rev.	Date	Comments
0364K	07/2014	Removed ATF16V8BQ device and commercial options due to becoming obsolete. Updated package drawings to most current versions and the 20S to 20S2 package drawing. Updated template, Atmel logos, disclaimer page.
0364J	07/2005	Green Package options added in 2005.
	1999	ATF16V8B-25 JC/PC/SC/XC/JI/PI/SI/XI and ATF16V8BQL-25 JC/PC/SC/XC/JI/PI/SI/XI were obsoleted in August 1999 and removed from the datasheet.

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