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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	672-LBGA
Supplier Device Package	672-LBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8347eczuajdb

- Address translation units for address mapping between host and peripheral
- Dual address cycle for target
- Internal configuration registers accessible from PCI
- Security engine is optimized to handle all the algorithms associated with IPSec, SSL/TLS, SRTP, IEEE Std. 802.11i®, iSCSI, and IKE processing. The security engine contains four crypto-channels, a controller, and a set of crypto execution units (EUs):
 - Public key execution unit (PKEU) :
 - RSA and Diffie-Hellman algorithms
 - Programmable field size up to 2048 bits
 - Elliptic curve cryptography
 - F2m and F(p) modes
 - Programmable field size up to 511 bits
 - Data encryption standard (DES) execution unit (DEU)
 - DES and 3DES algorithms
 - Two key (K1, K2) or three key (K1, K2, K3) for 3DES
 - ECB and CBC modes for both DES and 3DES
 - Advanced encryption standard unit (AESU)
 - Implements the Rijndael symmetric-key cipher
 - Key lengths of 128, 192, and 256 bits
 - ECB, CBC, CCM, and counter (CTR) modes
 - XOR parity generation accelerator for RAID applications
 - ARC four execution unit (AFEU)
 - Stream cipher compatible with the RC4 algorithm
 - 40- to 128-bit programmable key
 - Message digest execution unit (MDEU)
 - SHA with 160-, 224-, or 256-bit message digest
 - MD5 with 128-bit message digest
 - HMAC with either algorithm
 - Random number generator (RNG)
 - Four crypto-channels, each supporting multi-command descriptor chains
 - Static and/or dynamic assignment of crypto-execution units through an integrated controller
 - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
- Universal serial bus (USB) dual role controller
 - USB on-the-go mode with both device and host functionality
 - Complies with USB specification Rev. 2.0
 - Can operate as a stand-alone USB device
 - One upstream facing port
 - Six programmable USB endpoints

4.3 TSEC Gigabit Reference Clock Timing

Table 8 provides the TSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications.

Table 8. EC_GTX_CLK125 AC Timing Specifications

At recommended operating conditions with $LV_{DD} = 2.5 \pm 0.125$ mV/ 3.3 ± 0.165 mV

Parameter	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	t_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK125 rise and fall time $LV_{DD} = 2.5$ V $LV_{DD} = 3.3$ V	t_{G125R}/t_{G125F}	—	—	0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125L}	45 47	—	55 53	%	2
EC_GTX_CLK125 jitter	—	—	—	± 150	ps	2

Notes:

1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for $LV_{DD} = 2.5$ V and from 0.6 and 2.7 V for $LV_{DD} = 3.3$ V.
2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. The EC_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 8.2.4, "RGMII and RTBI AC Timing Specifications" for the duty cycle for 10Base-T and 100Base-T reference clock.

5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8347EA.

5.1 RESET DC Electrical Characteristics

Table 9 provides the DC electrical characteristics for the RESET pins of the MPC8347EA.

Table 9. RESET Pins DC Electrical Characteristics¹

Parameter	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	−0.3	0.8	V
Input current	I_{IN}	—	—	± 5	μA
Output high voltage ²	V_{OH}	$I_{OH} = -8.0$ mA	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0$ mA	—	0.5	V

Table 9. RESET Pins DC Electrical Characteristics¹ (continued)

Parameter	Symbol	Condition	Min	Max	Unit
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.4	V

Notes:

1. This table applies for pins $\overline{\text{PORESET}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, and $\overline{\text{QUIESCE}}$.
2. $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are open drain pins, thus V_{OH} is not relevant for those pins.

5.2 RESET AC Electrical Characteristics

Table 10 provides the reset initialization AC timing specifications of the MPC8347EA.

Table 10. RESET Initialization Timing Specifications

Parameter	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$ or $\overline{\text{SRESET}}$ (input) to activate reset flow	32	—	$t_{\text{PCI_SYNC_IN}}$	1
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to CLKIN when the MPC8347EA is in PCI host mode	32	—	t_{CLKIN}	2
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to PCI_SYNC_IN when the MPC8347EA is in PCI agent mode	32	—	$t_{\text{PCI_SYNC_IN}}$	1
$\overline{\text{HRESET}}/\overline{\text{SRESET}}$ assertion (output)	512	—	$t_{\text{PCI_SYNC_IN}}$	1
$\overline{\text{HRESET}}$ negation to $\overline{\text{SRESET}}$ negation (output)	16	—	$t_{\text{PCI_SYNC_IN}}$	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the MPC8347EA is in PCI host mode	4	—	t_{CLKIN}	2
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the MPC8347EA is in PCI agent mode	4	—	$t_{\text{PCI_SYNC_IN}}$	1
Input hold time for POR configuration signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	—
Time for the MPC8347EA to turn off POR configuration signals with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the MPC8347EA to turn on POR configuration signals with respect to the negation of $\overline{\text{HRESET}}$	1	—	$t_{\text{PCI_SYNC_IN}}$	1, 3

Notes:

1. $t_{\text{PCI_SYNC_IN}}$ is the clock period of the input clock applied to PCI_SYNC_IN. In PCI host mode, the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual*.
2. t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is valid only in PCI host mode. See the *MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual*.
3. POR configuration signals consist of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

Table 11 lists the PLL and DLL lock times.

Table 11. PLL and DLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	μs	—
DLL lock times	7680	122,880	csb_clk cycles	1, 2

Notes:

1. DLL lock times are a function of the ratio between the output clock and the coherency system bus clock (csb_clk). A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.
2. The csb_clk is determined by the CLKIN and system PLL ratio. See [Section 19, “Clocking.”](#)

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8347EA. Note that DDR SDRAM is $GV_{DD}(\text{typ}) = 2.5 \text{ V}$ and DDR2 SDRAM is $GV_{DD}(\text{typ}) = 1.8 \text{ V}$. The AC electrical specifications are the same for DDR and DDR2 SDRAM.

NOTE

The information in this document is accurate for revision 3.0 silicon and later. For information on revision 1.1 silicon and earlier versions see the *MPC8347E PowerQUICC II Pro Integrated Host Processor Hardware Specifications*. See [Section 22.1, “Part Numbers Fully Addressed by This Document,”](#) for silicon revision level determination.

6.1 DDR and DDR2 SDRAM DC Electrical Characteristics

Table 12 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8347EA when $GV_{DD}(\text{typ}) = 1.8 \text{ V}$.

Table 12. DDR2 SDRAM DC Electrical Characteristics for $GV_{DD}(\text{typ}) = 1.8 \text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.71	1.89	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.125$	$GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	-0.3	$MV_{REF} - 0.125$	V	—
Output leakage current	I_{OZ}	-9.9	9.9	μA	4
Output high current ($V_{OUT} = 1.420 \text{ V}$)	I_{OH}	-13.4	—	mA	—

6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 20 shows the DDR and DDR2 output AC timing specifications.

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) $\pm$ 5%.

Parameter	Symbol ¹	Min	Max	Unit	Notes
MCK[n] cycle time, (MCK[n]/ $\overline{MCK[n]}$ crossing) (PBGA package)	t_{MCK}	5	—	ns	2
MCK[n] cycle time, (MCK[n]/ $\overline{MCK[n]}$ crossing) (TBGA package)	t_{MCK}	7.5	—	ns	2
ADDR/CMD/MODT output setup with respect to MCK 400 MHz 333 MHz 266 MHz 200 MHz	t_{DDKHAS}	1.95 2.40 3.15 4.20	— — — —	ns	3
ADDR/CMD/MODT output hold with respect to MCK 400 MHz 333 MHz 266 MHz 200 MHz	t_{DDKHAX}	1.95 2.40 3.15 4.20	— — — —	ns	3
$\overline{MCS}(n)$ output setup with respect to MCK 400 MHz 333 MHz 266 MHz 200 MHz	t_{DDKHCS}	1.95 2.40 3.15 4.20	— — — —	ns	3
$\overline{MCS}(n)$ output hold with respect to MCK 400 MHz 333 MHz 266 MHz 200 MHz	t_{DDKHGX}	1.95 2.40 3.15 4.20	— — — —	ns	3
MCK to MDQS Skew	t_{DDKMHM}	−0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS 400 MHz 333 MHz 266 MHz 200 MHz	t_{DDKHDS} , t_{DDKLDS}	700 775 1100 1200	— — — —	ps	5
MDQ/MECC/MDM output hold with respect to MDQS 400 MHz 333 MHz	t_{DDKHDX} , t_{DDKLDX}	700 900	— —	ps	5

Table 28. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD}/OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
RX_CLK clock rise (20%–80%)	t_{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time (80%–20%)	t_{MRXF}	1.0	—	4.0	ns

Note:

- The symbols for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 12 provides the AC test load for TSEC.

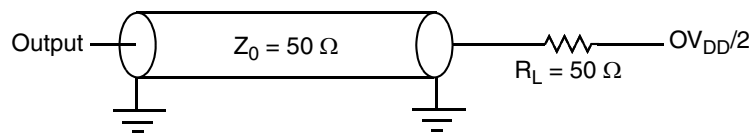


Figure 12. TSEC AC Test Load

Figure 13 shows the MII receive AC timing diagram.

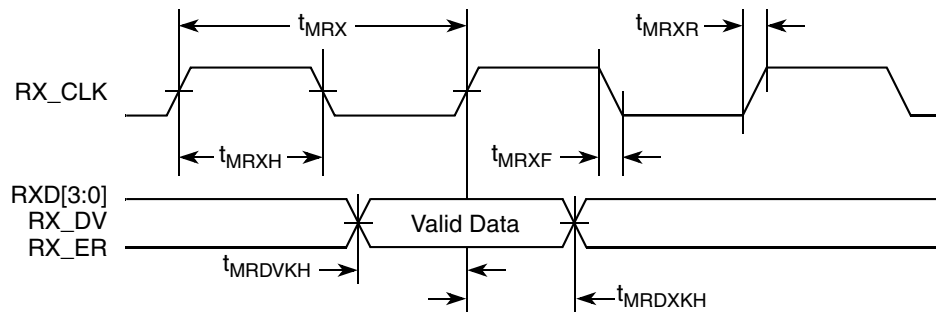


Figure 13. MII Receive AC Timing Diagram

8.2.3 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

Table 34. MII Management AC Timing Specifications (continued)

At recommended operating conditions with V_{DD} is 3.3 V $\pm$ 10% or 2.5 V $\pm$ 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit	Notes
MDC fall time	t_{MDHF}	—	—	10	ns	—

Notes:

1. The symbols for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a csb_clk of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz).
3. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 267 MHz, the delay is 70 ns and for a csb_clk of 333 MHz, the delay is 58 ns).

Figure 17 shows the MII management AC timing diagram.

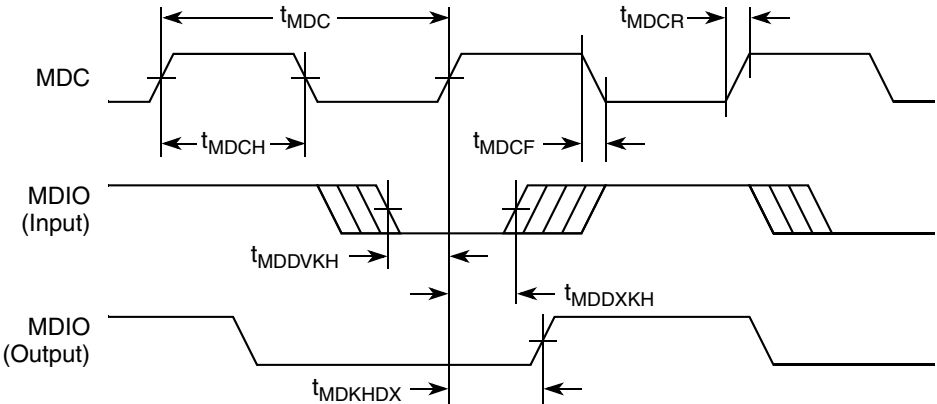


Figure 17. MII Management Interface Timing Diagram

Pitch	1.00 mm
Module height (typical)	1.46 mm
Solder balls	62 Sn/36 Pb/2 Ag (ZU package) 96.5 Sn/3.5Ag (VV package)
Ball diameter (typical)	0.64 mm

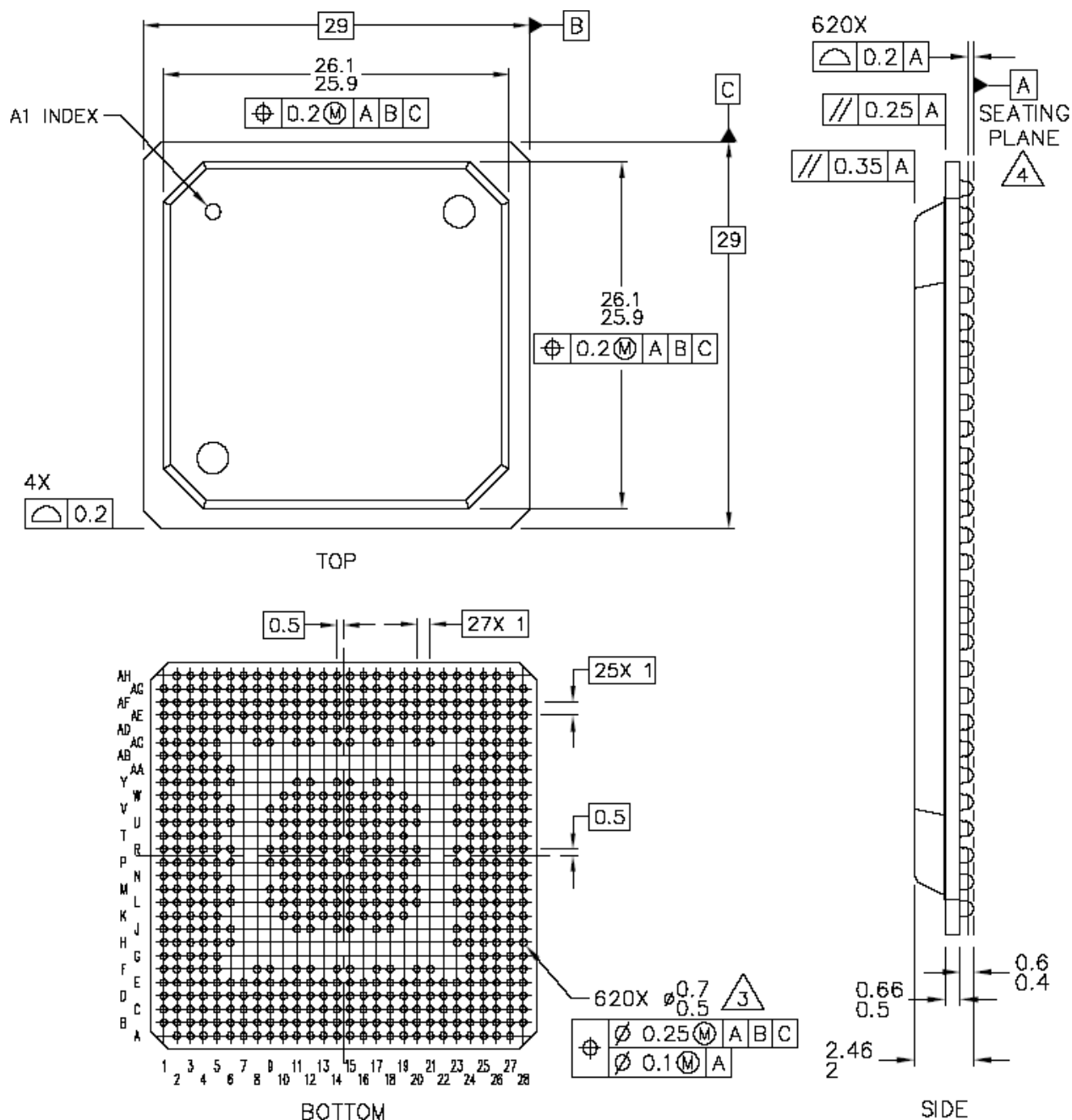
18.3 Package Parameters for the MPC8347EA PBGA

The package parameters are as provided in the following list. The package type is 29 mm × 29 mm, 620 plastic ball grid array (PBGA).

Package outline	29 mm × 29 mm
Interconnects	620
Pitch	1.00 mm
Module height (maximum)	2.46 mm
Module height (typical)	2.23 mm
Module height (minimum)	2.00 mm
Solder balls	62 Sn/36 Pb/2 Ag (ZQ package) 96.5 Sn/3.5Ag (VR package)
Ball diameter (typical)	0.60 mm

18.4 Mechanical Dimensions for the MPC8347EA PBGA

Figure 41 shows the mechanical dimensions and bottom surface nomenclature for the MPC8347EA, 620-PBGA package.



Notes:

1. All dimensions are in millimeters.
2. Dimensioning and tolerancing per ASME Y14. 5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

Figure 41. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC8347EA PBGA

18.5 Pinout Listings

Table 55 provides the pinout listing for the MPC8347EA, 672 TBGA package.

Table 55. MPC8347EA (TBGA) Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI				
PCI_INTA/IRQ_OUT	B34	O	OV _{DD}	2
PCI_RESET_OUT	C33	O	OV _{DD}	—
PCI_AD[31:0]	G30, G32, G34, H31, H32, H33, H34, J29, J32, J33, L30, K31, K33, K34, L33, L34, P34, R29, R30, R33, R34, T31, T32, T33, U31, U34, V31, V32, V33, V34, W33, W34	I/O	OV _{DD}	—
PCI_C/BE[3:0]	J30, M31, P33, T34	I/O	OV _{DD}	—
PCI_PAR	P32	I/O	OV _{DD}	—
PCI_FRAME	M32	I/O	OV _{DD}	5
PCI_TRDY	N29	I/O	OV _{DD}	5
PCI_IRDY	M34	I/O	OV _{DD}	5
PCI_STOP	N31	I/O	OV _{DD}	5
PCI_DEVSEL	N30	I/O	OV _{DD}	5
PCI_IDSEL	J31	I	OV _{DD}	—
PCI_SERR	N34	I/O	OV _{DD}	5
PCI_PERR	N33	I/O	OV _{DD}	5
PCI_REQ[0]	D32	I/O	OV _{DD}	—
PCI_REQ[1]/CPCI1_HS_ES	D34	I	OV _{DD}	—
PCI_REQ[2:4]	E34, F32, G29	I	OV _{DD}	—
PCI_GNT0	C34	I/O	OV _{DD}	—
PCI_GNT1/CPCI1_HS_LED	D33	O	OV _{DD}	—
PCI_GNT2/CPCI1_HS_ENUM	E33	O	OV _{DD}	—
PCI_GNT[3:4]	F31, F33	O	OV _{DD}	—
M66EN	A19	I	OV _{DD}	—
DDR SDRAM Memory Interface				
MDQ[0:63]	D5, A3, C3, D3, C4, B3, C2, D4, D2, E5, G2, H6, E4, F3, G4, G3, H1, J2, L6, M6, H2, K6, L2, M4, N2, P4, R2, T4, P6, P3, R1, T2, AB5, AA3, AD6, AE4, AB4, AC2, AD3, AE6, AE3, AG4, AK5, AK4, AE2, AG6, AK3, AK2, AL2, AL1, AM5, AP5, AM2, AN1, AP4, AN5, AJ7, AN7, AM8, AJ9, AP6, AL7, AL9, AN8	I/O	GV _{DD}	—

Table 55. MPC8347EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LALÉ	AK24	O	OV _{DD}	—
LGPL0/LSDA10/cfg_reset_source0	AP27	I/O	OV _{DD}	—
LGPL1/LSDWE/cfg_reset_source1	AL25	I/O	OV _{DD}	—
LGPL2/LSDRAS/LOE	AJ24	O	OV _{DD}	—
LGPL3/LSDCAS/cfg_reset_source2	AN27	I/O	OV _{DD}	—
LGPL4/LGTÁ/LUPWAIT/LPBSE	AP28	I/O	OV _{DD}	13
LGPL5/cfg_clkin_div	AL26	I/O	OV _{DD}	—
LCKE	AM27	O	OV _{DD}	—
LCLK[0:2]	AN28, AK26, AP29	O	OV _{DD}	—
LSYNC_OUT	AM12	O	OV _{DD}	—
LSYNC_IN	AJ10	I	OV _{DD}	—
General Purpose I/O Timers				
GPIO1[0]/DMA_DREQ0/GTM1_TIN1/ GTM2_TIN2	F24	I/O	OV _{DD}	—
GPIO1[1]/DMA_DACK0/GTM1_TGATE1/ GTM2_TGATE2	E24	I/O	OV _{DD}	—
GPIO1[2]/DMA_DDONE0/GTM1_TOUT1	B25	I/O	OV _{DD}	—
GPIO1[3]/DMA_DREQ1/GTM1_TIN2/ GTM2_TIN1	D24	I/O	OV _{DD}	—
GPIO1[4]/DMA_DACK1/GTM1_TGATE2/ GTM2_TGATE1	A25	I/O	OV _{DD}	—
GPIO1[5]/DMA_DDONE1/GTM1_TOUT2/ GTM2_TOUT1	B24	I/O	OV _{DD}	—
GPIO1[6]/DMA_DREQ2/GTM1_TIN3/ GTM2_TIN4	A24	I/O	OV _{DD}	—
GPIO1[7]/DMA_DACK2/GTM1_TGATE3/ GTM2_TGATE4	D23	I/O	OV _{DD}	—
GPIO1[8]/DMA_DDONE2/GTM1_TOUT3	B23	I/O	OV _{DD}	—
GPIO1[9]/DMA_DREQ3/GTM1_TIN4/ GTM2_TIN3	A23	I/O	OV _{DD}	—
GPIO1[10]/DMA_DACK3/GTM1_TGATE4/ GTM2_TGATE3	F22	I/O	OV _{DD}	—
GPIO1[11]/DMA_DDONE3/GTM1_TOUT4/ GTM2_TOUT3	E22	I/O	OV _{DD}	—
USB Port 1				
MPH1_D0_ENABLEN/DR_D0_ENABLEN	A26	I/O	OV _{DD}	—
MPH1_D1_SER_TXD/DR_D1_SER_TXD	B26	I/O	OV _{DD}	—
MPH1_D2_VMO_SE0/DR_D2_VMO_SE0	D25	I/O	OV _{DD}	—

Table 55. MPC8347EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GV _{DD}	A2, E2, G5, G6, J5, K4, K5, L4, N4, P5, R6, T6, U5, V1, W5, Y5, AA4, AB3, AC4, AD5, AF3, AG5, AH2, AH5, AH6, AJ6, AK6, AK8, AK9, AL6	Power for DDR DRAM I/O voltage (2.5 V)	GV _{DD}	—
LV _{DD} 1	C9, D11	Power for three-speed Ethernet #1 and for Ethernet management interface I/O (2.5 V, 3.3 V)	LV _{DD} 1	—
LV _{DD} 2	C6, D9	Power for three-speed Ethernet #2 I/O (2.5 V, 3.3 V)	LV _{DD} 2	—
V _{DD}	E19, E29, F7, F9, F11, F13, F15, F17, F18, F21, F23, F25, F29, H29, J6, K29, M29, N6, P29, T29, U30, V6, V29, W29, AB29, AC5, AD29, AF6, AF29, AH29, AJ8, AJ12, AJ14, AJ16, AJ18, AJ20, AJ21, AJ23, AJ25, AJ26, AJ27, AJ28, AJ29, AK10	Power for core (1.2 V nominal, 1.3 V for 667 MHz)	V _{DD}	—
OV _{DD}	B22, B28, C16, C17, C24, C26, D13, D15, D19, D29, E31, F28, G33, H30, L29, L32, N32, P31, R31, U32, W31, Y29, AA29, AC30, AE31, AF30, AG29, AJ17, AJ30, AK11, AL15, AL19, AL21, AL29, AL30, AM20, AM23, AM24, AM26, AM28, AN11, AN13	PCI, 10/100 Ethernet, and other standard (3.3 V)	OV _{DD}	—
MVREF1	M3	I	DDR reference voltage	—
MVREF2	AD2	I	DDR reference voltage	—

Table 56. MPC8347EA (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC1_RX_CLK	U26	I	LV _{DD1}	—
TSEC1_RX_DV	U24	I	LV _{DD1}	—
TSEC1_RX_ER/GPIO2[26]	L28	I/O	OV _{DD}	—
TSEC1_RXD[7:4]/GPIO2[22:25]	M27, M28, N26, N27	I/O	OV _{DD}	—
TSEC1_RXD[3:0]	W26, W24, Y28, Y27	I	LV _{DD1}	—
TSEC1_TX_CLK	N25	I	OV _{DD}	—
TSEC1_TXD[7:4]/GPIO2[27:30]	N28, P25, P26, P27	I/O	OV _{DD}	—
TSEC1_TXD[3:0]	V28, V27, V26, W28	O	LV _{DD1}	10
TSEC1_TX_EN	W27	O	LV _{DD1}	—
TSEC1_TX_ER/GPIO2[31]	N24	I/O	OV _{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_COL/GPIO1[21]	P28	I/O	OV _{DD}	—
TSEC2_CRS/GPIO1[22]	AC28	I/O	LV _{DD2}	—
TSEC2_GTX_CLK	AC27	O	LV _{DD2}	—
TSEC2_RX_CLK	AB25	I	LV _{DD2}	—
TSEC2_RX_DV/GPIO1[23]	AC26	I/O	LV _{DD2}	—
TSEC2_RXD[7:4]/GPIO1[26:29]	R28, T24, T25, T26	I/O	OV _{DD}	—
TSEC2_RXD[3:0]/GPIO1[13:16]	AA25, AA26, AA27, AA28	I/O	LV _{DD2}	—
TSEC2_RX_ER/GPIO1[25]	R25	I/O	OV _{DD}	—
TSEC2_TXD[7]/GPIO1[31]	T27	I/O	OV _{DD}	—
TSEC2_TXD[6]/DR_XCVR_TERM_SEL	T28	O	OV _{DD}	—
TSEC2_TXD[5]/DR_UTMI_OPMODE1	U28	O	OV _{DD}	—
TSEC2_TXD[4]/DR_UTMI_OPMODE0	U27	O	OV _{DD}	—
TSEC2_TXD[3:0]/GPIO1[17:20]	AB26, AB27, AA24, AB28	I/O	LV _{DD2}	—
TSEC2_TX_ER/GPIO1[24]	R27	I/O	OV _{DD}	—
TSEC2_TX_EN/GPIO1[12]	AD28	I/O	LV _{DD2}	3
TSEC2_TX_CLK/GPIO1[30]	R26	I/O	OV _{DD}	—
DUART				
UART_SOUT[1:2]/MSRCID[0:1]/LSRCID[0:1]	B4, A4	O	OV _{DD}	—
UART_SIN[1:2]/MSRCID[2:3]/LSRCID[2:3]	D5, C5	I/O	OV _{DD}	—
UART_CTS[1]/MSRCID4/LSRCID4	B5	I/O	OV _{DD}	—
UART_CTS[2]/MDVAL/LDVAL	A5	I/O	OV _{DD}	—
UART_RTS[1:2]	D6, C6	O	OV _{DD}	—

Table 56. MPC8347EA (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Thermal Management				
THERM0	B15	I	—	8
Power and Ground Signals				
AV _{DD1}	C15	Power for e300 PLL (1.2 V) nominal, 1.3 V for 667 MHz)	AV _{DD1}	—
AV _{DD2}	U1	Power for system PLL (1.2 V) nominal, 1.3 V for 667 MHz)	AV _{DD2}	—
AV _{DD3}	AF9	Power for DDR DLL (1.2 V nominal, 1.3 V for 667 MHz)		—
AV _{DD4}	U2	Power for LBIU DLL (1.2 V nominal, 1.3 V for 667 MHz)	AV _{DD4}	—
GND	A2, B1, B2, D10, D18, E6, E14, E22, F9, F12, F15, F18, F21, F24, G5, H6, J23, L4, L6, L12, L13, L14, L15, L16, L17, M11, M12, M13, M14, M15, M16, M17, M18, M23, N11, N12, N13, N14, N15, N16, N17, N18, P6, P11, P12, P13, P14, P15, P16, P17, P18, P24, R5, R11, R12, R13, R14, R15, R16, R17, R18, R23, T11, T12, T13, T14, T15, T16, T17, T18, U6, U11, U12, U13, U14, U15, U16, U17, U18, V12, V13, V14, V15, V16, V17, V23, V25, W4, Y6, AA23, AB24, AC5, AC8, AC11, AC14, AC17, AC20, AD9, AD15, AD21, AE12, AE18, AF3, AF26	—	—	—
GV _{DD}	U9, V9, W10, W19, Y11, Y12, Y14, Y15, Y17, Y18, AA6, AB5, AC9, AC12, AC15, AC18, AC21, AC24, AD6, AD8, AD14, AD20, AE5, AE11, AE17, AG2, AG27	Power for DDR DRAM I/O voltage (2.5 V)	GV _{DD}	—

19 Clocking

Figure 42 shows the internal distribution of the clocks.

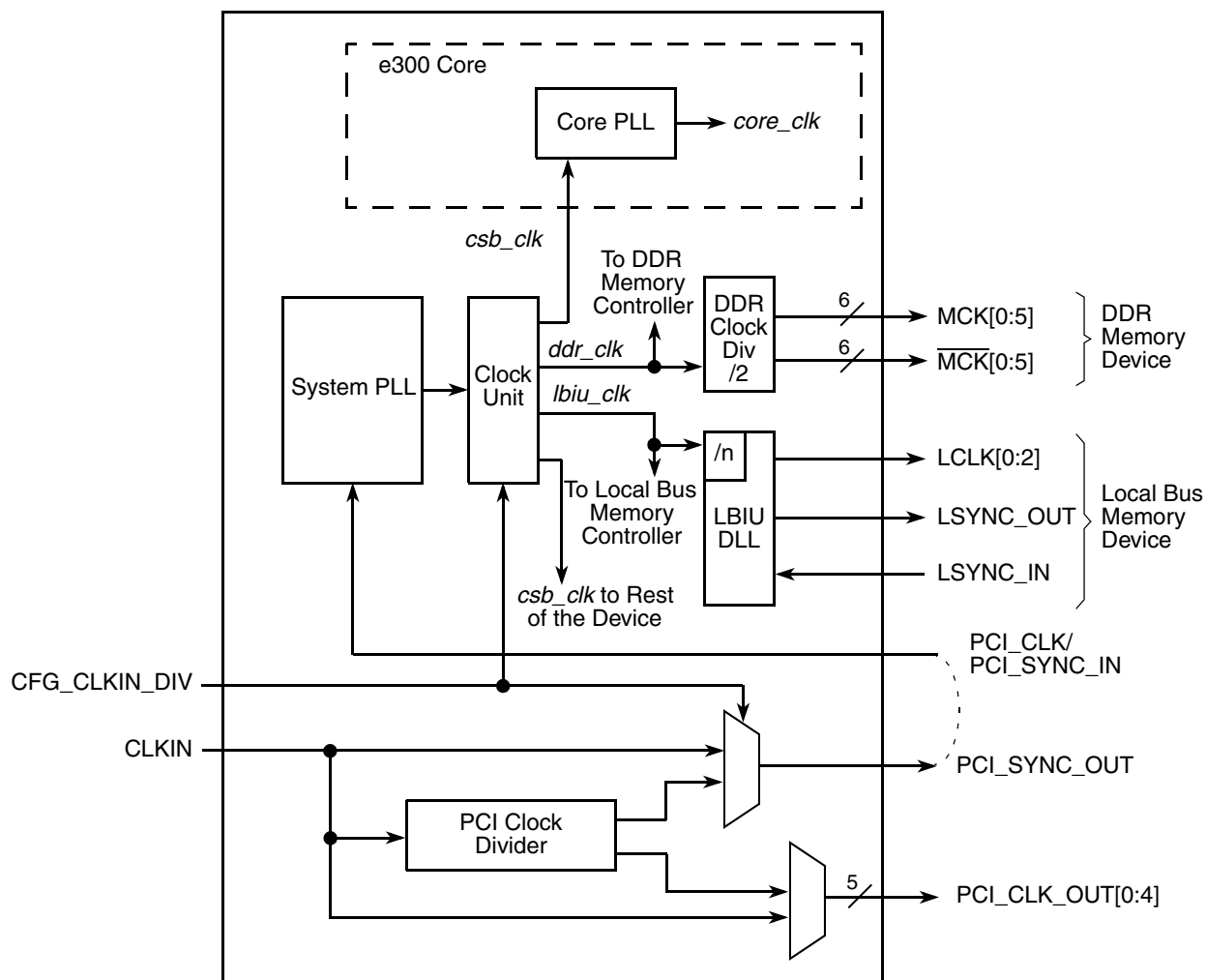


Figure 42. MPC8347EA Clock Subsystem

The primary clock source can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. When the MPC8347EA is configured as a PCI host device, CLKIN is its primary input clock. CLKIN feeds the PCI clock divider ($\div 2$) and the multiplexers for PCI_SYNC_OUT and PCI_CLK_OUT. The CFG_CLKIN_DIV configuration input selects whether CLKIN or CLKIN/2 is driven out on the PCI_SYNC_OUT signal. The OCCR[PCICDn] parameters select whether CLKIN or CLKIN/2 is driven out on the PCI_CLK_OUTn signals.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the MPC8347EA to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input clock and the CLKIN signal should be tied to GND.

20.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J , can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Generally, the value obtained on a single-layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

20.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

20.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature and a measure of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per the JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

20.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

Some application environments require a heat sink to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

The thermal performance of devices with heat sinks has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

However, while $\overline{\text{HRESET}}$ is asserted, these pins are treated as inputs, and the value on these pins is latched when $\overline{\text{PORESET}}$ deasserts. Then the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for the output pins.

21.7 Pull-Up Resistor Requirements

The MPC8347EA requires high resistance pull-up resistors (10 k Ω is recommended) on open-drain pins, including I²C pins, and IPIC interrupt pins.

For more information on required pull-up resistors and the connections required for the JTAG interface, refer to application note AN2931, “PowerQUICC Design Checklist.”

22 Ordering Information

This section presents ordering information for the device discussed in this document, and it shows an example of how the parts are marked.

NOTE

The information in this document is accurate for revision 3.x silicon and later (in other words, for orderable part numbers ending in A or B). For information on revision 1.1 silicon and earlier versions, see the *MPC8347E PowerQUICC II Pro Integrated Host Processor Hardware Specifications* (Document Order No. MPC8347EEC).

22.1 Part Numbers Fully Addressed by This Document

Table 70 shows an analysis of the Freescale part numbering nomenclature for the MPC8347EA. The individual part numbers correspond to a maximum processor core frequency. Each part number also contains a revision code that refers to the die mask revision number. For available frequency configuration

Table 72. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
8	2/2009	- Added footnote 6 to Table 7. - In Section 9.2, "USB AC Electrical Specifications," clarified that AC table is for ULPI only. - In Table 39, corrected t_{LBKHOV} parameter to t_{LBKLOV} (output data is driven on falling edge of clock in DLL bypass mode). Similarly, made the same correction to Figure 22, Figure 24, and Figure 25 for output signals. - Added footnote 10 and 11 to Table 55 and Table 56. - In Section 21.1, "System Clocking," removed "(AVDD1)" and "(AVDD2)" from bulleted list. - In Section 21.2, "PLL Power Supply Filtering," in the second paragraph, changed "provide five independent filter circuits," and "the five AVDD pins" to provide four independent filter circuits," and "the four AVDD pins." - In Table 58, corrected the max csb_clk to 266 MHz. - In Table 64, added PLL configurations 903, 923, A03, A23, and 503 for 533 MHz - Added footnote 4 to Table 70. - In Table 70, updated note 1 to say the following: "For temperature range = C, processor frequency is limited to 533 (TBGA) and 400 (PBGA) with a platform frequency of 266."
7	4/2007	- In Table 3, "Output Drive Capability," changed the values in the Output Impedance column and added USB to the seventh row. - In Table 4, "Operating Frequencies for TBGA," added column for 400 MHz. - In Section 21.7, "Pull-Up Resistor Requirements," deleted last two paragraphs and after first paragraph, added a new paragraph. - Deleted Section 21.8, "JTAG Configuration Signals," and Figure 43, "JTAG Interface Connection."
6	3/2007	- Page 1, updated first paragraph to reflect PowerQUICC II Pro information. - In Table 18, "DDR and DDR2 SDRAM Input AC Timing Specifications," added note 2 to t_{CISKEW} and deleted original note 3; renumbered the remaining notes. - In Figure 43, "JTAG Interface Connection," updated with new figure. - In Table 57, "Operating Frequencies for TBGA," in the 'Coherent system bus frequency (<i>csb_clk</i>)' row, changed the value in the 533 MHz column to 100-333. - In Table 63, "Suggested PLL Configurations," under the subhead, '33 MHz CLKIN/PCI_CLK Options,' added row A03 between Ref. No. 724 and 804. Under the subhead '66 MHz CLKIN/PCI_CLK Options,' added row 503 between Ref. No. 305 and 404. For Ref. No. 306, changed the CORE PLL value to 0000110. - In Section 23, "Ordering Information," replaced first paragraph and added a note. - In Section 23.1, "Part Numbers Fully Addressed by this Document," replaced first paragraph.
5	1/2007	- In Table 1, "Absolute Maximum Ratings," added (1.36 max for 667-MHz core frequency). - In Table 2, "Recommended Operating Conditions," added a row showing nominal core supply voltage of 1.3 V for 667-MHz parts. - In Table 4, "MPC8347EA Power Dissipation," added two footnotes to 667-MHz row showing nominal core supply voltage of 1.3 V for 667-MHz parts. - In Table 54, "MPC8347EA (TBGA) Pinout Listing," updated V_{DD} row to show nominal core supply voltage of 1.3 V for 667-MHz parts.
4	12/2006	Table 19, "DDR and DDR2 SDRAM Output AC Timing Specifications," modified T_{ddkhd} for 333 MHz from 900 ps to 775 ps.
3	11/2006	- Updated note in introduction. - In the features list in Section 1, "Overview," updated DDR data rate to show 266 MHz for PBGA parts for all silicon revisions, and 400 MHz for DDR2 for TBGA parts for silicon Rev. 2 and 3. - In Table 5, "MPC8347EA Typical I/O Power Dissipation," added GV_{DD} 1.8-V values for DDR2; added table footnote to designate rates that apply only to the TBGA package. - In Section 23, "Ordering Information," replicated note from document introduction.