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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	672-LBGA
Supplier Device Package	672-LBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8347evvagdb

- Address translation units for address mapping between host and peripheral
- Dual address cycle for target
- Internal configuration registers accessible from PCI
- Security engine is optimized to handle all the algorithms associated with IPSec, SSL/TLS, SRTP, IEEE Std. 802.11i®, iSCSI, and IKE processing. The security engine contains four crypto-channels, a controller, and a set of crypto execution units (EUs):
 - Public key execution unit (PKEU) :
 - RSA and Diffie-Hellman algorithms
 - Programmable field size up to 2048 bits
 - Elliptic curve cryptography
 - F2m and F(p) modes
 - Programmable field size up to 511 bits
 - Data encryption standard (DES) execution unit (DEU)
 - DES and 3DES algorithms
 - Two key (K1, K2) or three key (K1, K2, K3) for 3DES
 - ECB and CBC modes for both DES and 3DES
 - Advanced encryption standard unit (AESU)
 - Implements the Rijndael symmetric-key cipher
 - Key lengths of 128, 192, and 256 bits
 - ECB, CBC, CCM, and counter (CTR) modes
 - XOR parity generation accelerator for RAID applications
 - ARC four execution unit (AFEU)
 - Stream cipher compatible with the RC4 algorithm
 - 40- to 128-bit programmable key
 - Message digest execution unit (MDEU)
 - SHA with 160-, 224-, or 256-bit message digest
 - MD5 with 128-bit message digest
 - HMAC with either algorithm
 - Random number generator (RNG)
 - Four crypto-channels, each supporting multi-command descriptor chains
 - Static and/or dynamic assignment of crypto-execution units through an integrated controller
 - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
- Universal serial bus (USB) dual role controller
 - USB on-the-go mode with both device and host functionality
 - Complies with USB specification Rev. 2.0
 - Can operate as a stand-alone USB device
 - One upstream facing port
 - Six programmable USB endpoints

- On-chip digital filtering rejects spikes on the bus
- System initialization data optionally loaded from I²C-1 EPROM by boot sequencer embedded hardware
- DMA controller
 - Four independent virtual channels
 - Concurrent execution across multiple channels with programmable bandwidth control
 - Handshaking (external control) signals for all channels: $\overline{\text{DMA_DREQ}}[0:3]$, $\overline{\text{DMA_DACK}}[0:3]$, $\overline{\text{DMA_DDONE}}[0:3]$
 - All channels accessible to local core and remote PCI masters
 - Misaligned transfer capability
 - Data chaining and direct mode
 - Interrupt on completed segment and chain
- DUART
 - Two 4-wire interfaces (RxD, TxD, RTS, CTS)
 - Programming model compatible with the original 16450 UART and the PC16550D
- Serial peripheral interface (SPI) for master or slave
- General-purpose parallel I/O (GPIO)
 - 52 parallel I/O pins multiplexed on various chip interfaces
- System timers
 - Periodic interrupt timer
 - Real-time clock
 - Software watchdog timer
 - Eight general-purpose timers
- Designed to comply with IEEE Std. 1149.1™, JTAG boundary scan
- Integrated PCI bus and SDRAM clock generation

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8347EA. The device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

Figure 3 shows the undershoot and overshoot voltage of the PCI interface of the MPC8347EA for the 3.3-V signals, respectively.

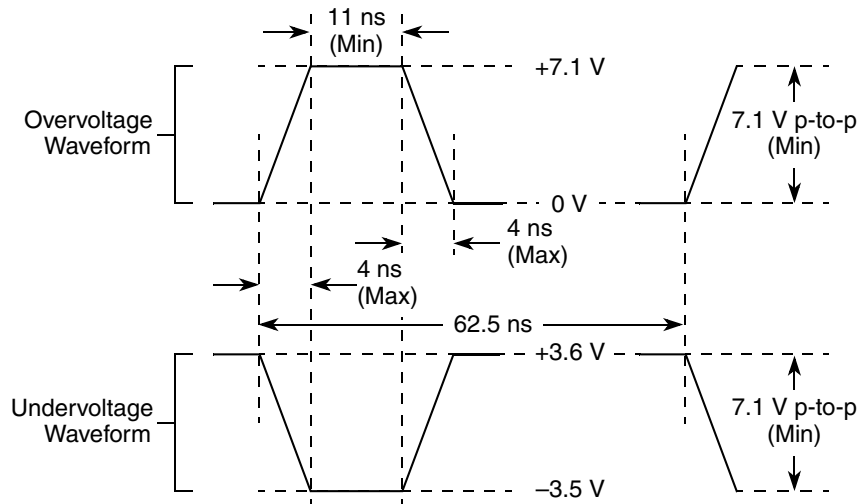


Figure 3. Maximum AC Waveforms on PCI Interface for 3.3-V Signaling

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	40	$OV_{DD} = 3.3 \text{ V}$
PCI signals (not including PCI output clocks)	25	
PCI output clocks (including PCI_SYNC_OUT)	40	
DDR signal	18	$GV_{DD} = 2.5 \text{ V}$
DDR2 signal	18 36 (half-strength mode)	$GV_{DD} = 1.8 \text{ V}$
TSEC/10/100 signals	40	$LV_{DD} = 2.5/3.3 \text{ V}$
DUART, system control, I ² C, JTAG, USB	40	$OV_{DD} = 3.3 \text{ V}$
GPIO signals	40	$OV_{DD} = 3.3 \text{ V}$, $LV_{DD} = 2.5/3.3 \text{ V}$

2.2 Power Sequencing

This section details the power sequencing considerations for the MPC8347EA.

2.2.1 Power-Up Sequencing

MPC8347EA does not require the core supply voltage (V_{DD} and AV_{DD}) and I/O supply voltages (GV_{DD} , LV_{DD} , and OV_{DD}) to be applied in any particular order. During the power ramp up, before the power

6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 20 shows the DDR and DDR2 output AC timing specifications.

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) $\pm$ 5%.

Parameter	Symbol ¹	Min	Max	Unit	Notes
MCK[n] cycle time, (MCK[n]/ $\overline{MCK[n]}$ crossing) (PBGA package)	t_{MCK}	5	—	ns	2
MCK[n] cycle time, (MCK[n]/ $\overline{MCK[n]}$ crossing) (TBGA package)	t_{MCK}	7.5	—	ns	2
ADDR/CMD/MODT output setup with respect to MCK 400 MHz 333 MHz 266 MHz 200 MHz	t_{DDKHAS}	1.95 2.40 3.15 4.20	— — — —	ns	3
ADDR/CMD/MODT output hold with respect to MCK 400 MHz 333 MHz 266 MHz 200 MHz	t_{DDKHAX}	1.95 2.40 3.15 4.20	— — — —	ns	3
$\overline{MCS}(n)$ output setup with respect to MCK 400 MHz 333 MHz 266 MHz 200 MHz	t_{DDKHCS}	1.95 2.40 3.15 4.20	— — — —	ns	3
$\overline{MCS}(n)$ output hold with respect to MCK 400 MHz 333 MHz 266 MHz 200 MHz	t_{DDKHGX}	1.95 2.40 3.15 4.20	— — — —	ns	3
MCK to MDQS Skew	t_{DDKMHM}	−0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS 400 MHz 333 MHz 266 MHz 200 MHz	t_{DDKHDS} , t_{DDKLDS}	700 775 1100 1200	— — — —	ps	5
MDQ/MECC/MDM output hold with respect to MDQS 400 MHz 333 MHz	t_{DDKHDX} , t_{DDKLDX}	700 900	— —	ps	5

Table 30. TBI Receive AC Timing Specifications (continued)

At recommended operating conditions with V_{DD}/OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
RXD[7:0], RX_DV, RX_ER (RCG[9:0]) setup time to rising PMA_RX_CLK	t_{TRDVKH}^2	2.5	—	—	ns
RXD[7:0], RX_DV, RX_ER (RCG[9:0]) hold time to rising PMA_RX_CLK	t_{TRDXKH}^2	1.5	—	—	ns
RX_CLK clock rise time (20%–80%)	t_{TRXR}	0.7	—	2.4	ns
RX_CLK clock fall time (80%–20%)	t_{TRXF}	0.7	—	2.4	ns

Notes:

- The symbols for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript SK followed by the clock that is being skewed (TRX).
- Setup and hold time of even numbered RCG are measured from the rising edge of PMA_RX_CLK1. Setup and hold times of odd-numbered RCG are measured from the rising edge of PMA_RX_CLK0.

Figure 15 shows the TBI receive AC timing diagram.

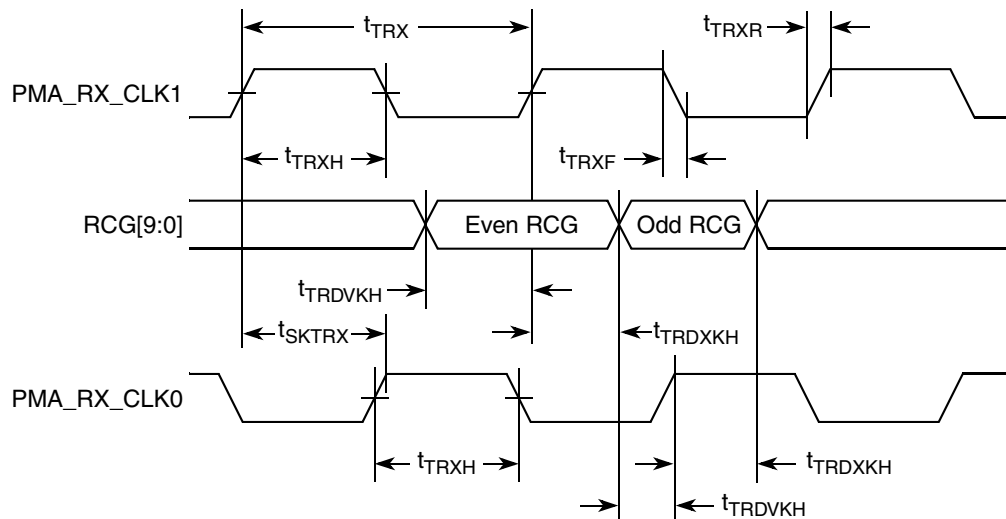


Figure 15. TBI Receive AC Timing Diagram

10.2 Local Bus AC Electrical Specification

Table 38 and Table 39 describe the general timing parameters of the local bus interface of the MPC8347EA.

Table 38. Local Bus General Timing Parameters—DLL On

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	—	ns	2
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	1.5	—	ns	3, 4
LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	2.2	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	1.0	—	ns	3, 4
LUPWAIT Input hold from local bus clock	$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
Local bus clock to LALE rise	t_{LBKHLR}	—	4.5	ns	—
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	4.5	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	4.5	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	4.5	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	1	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	1	—	ns	3
Local bus clock to output high impedance for LAD/LDP	t_{LBKHOZ}	—	3.8	ns	8

Notes:

1. The symbols for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to the rising edge of LSYNC_IN.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is not set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is set and when the load on the LALE output pin equals the load on the LAD output pins.
8. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

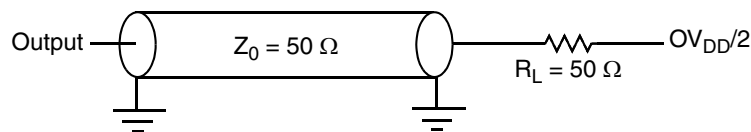
Table 39. Local Bus General Timing Parameters—DLL Bypass⁹

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	15	—	ns	2
Input setup to local bus clock	t_{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock	t_{LBIXKH}	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
Local bus clock to output valid	t_{LBKLOV}	—	3	ns	3
Local bus clock to output high impedance for LAD/LDP	t_{LBKHOZ}	—	4	ns	8

Notes:

1. The symbols for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to the falling edge of LCLK0 (for all outputs and for $\overline{LGTA}$ and LUPWAIT inputs) or the rising edge of LCLK0 (for all other inputs).
3. All signals are measured from $OV_{DD}/2$ of the rising/falling edge of LCLK0 to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is not set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is not set and when the load on the LALE output pin equals to the load on the LAD output pins.
8. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
9. DLL bypass mode is not recommended for use at frequencies above 66 MHz.

Figure 20 provides the AC test load for the local bus.


Figure 20. Local Bus C Test Load

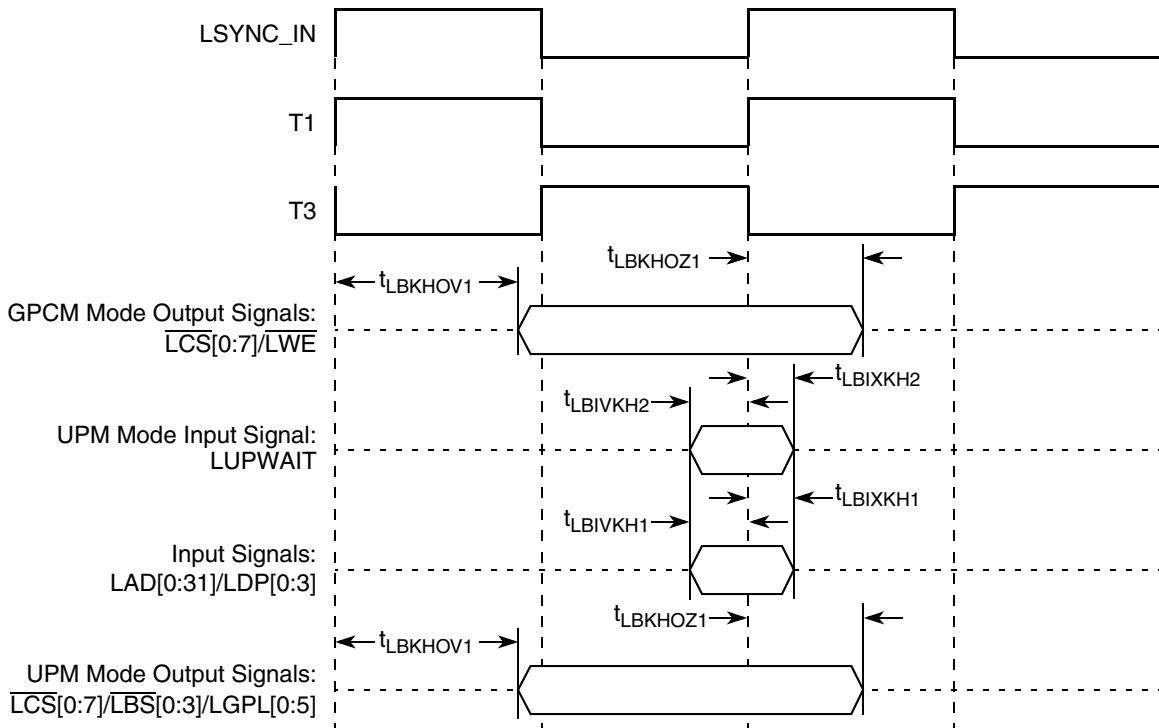


Figure 23. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Enabled)

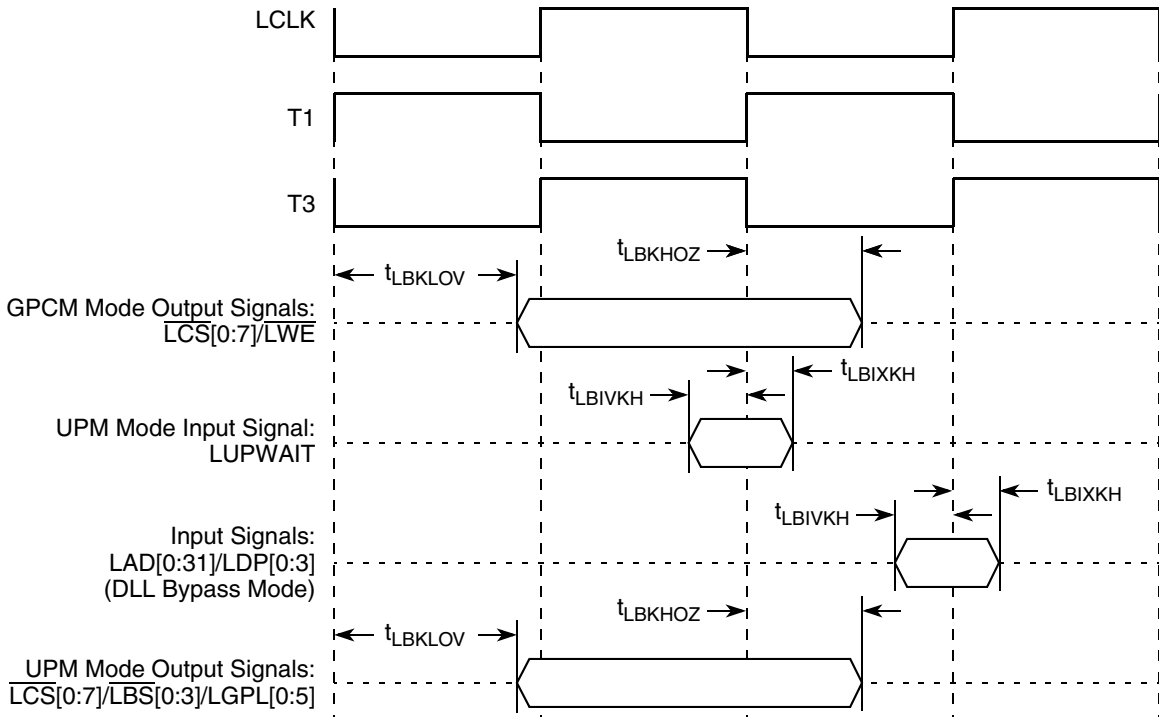


Figure 24. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Bypass Mode)

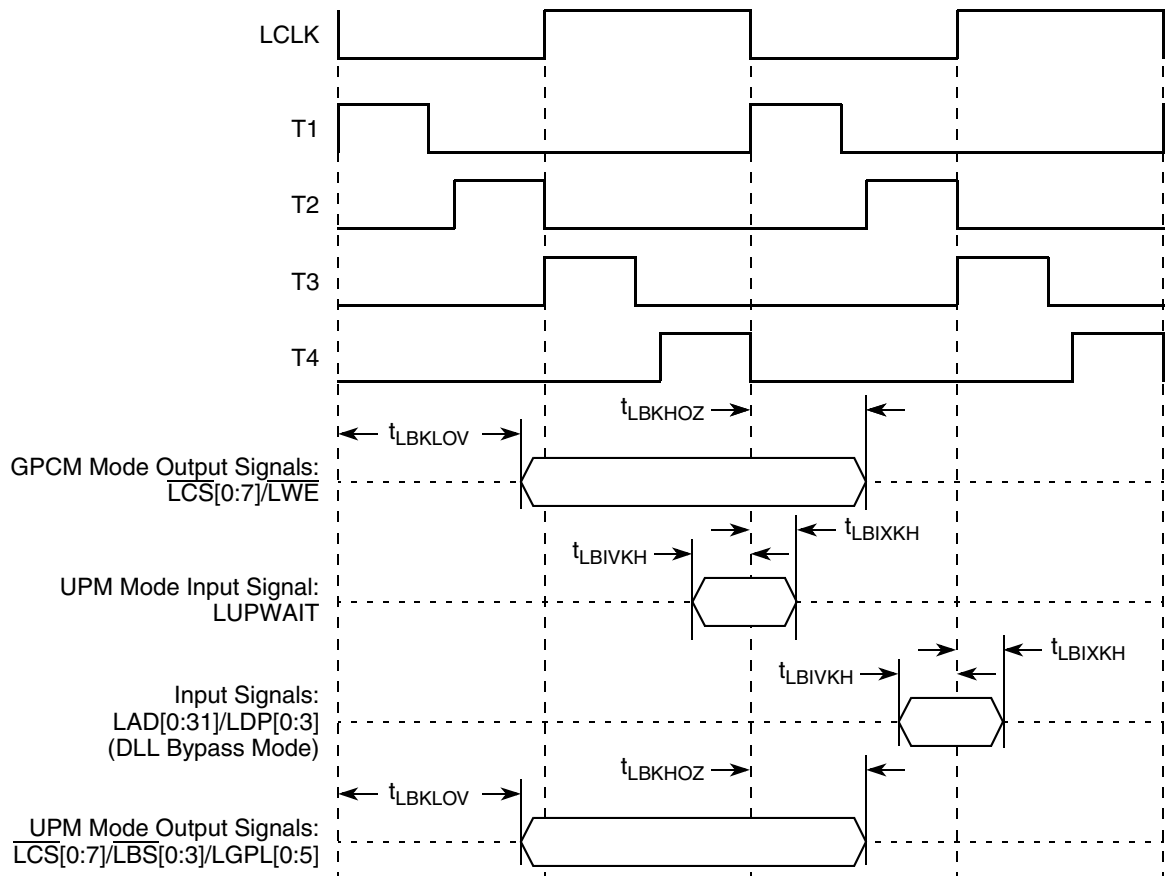


Figure 25. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (DLL Bypass Mode)

Table 41. JTAG AC Timing Specifications (Independent of CLKIN)¹ (continued)

At recommended operating conditions (see Table 2).

Parameter	Symbol ²	Min	Max	Unit	Notes
JTAG external clock to output high impedance: Boundary-scan data TDO	t_{JTKLDZ} t_{JTKLOZ}	2 2	19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50 Ω load (see Figure 18). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{JTDVXH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDVXH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{TRST}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK} .
5. Non-JTAG signal output timing with respect to t_{TCLK} .
6. Guaranteed by design and characterization.

Figure 27 provides the AC test load for TDO and the boundary-scan outputs of the MPC8347EA.

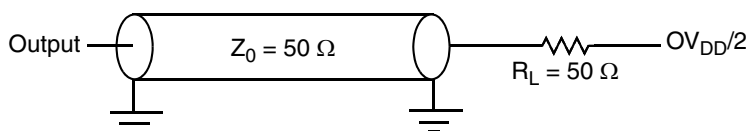

Figure 27. AC Test Load for the JTAG Interface

Figure 28 provides the JTAG clock input timing diagram.

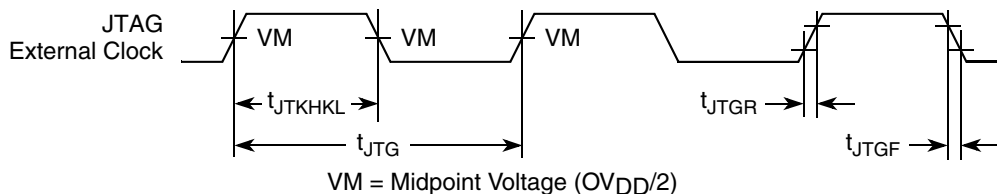
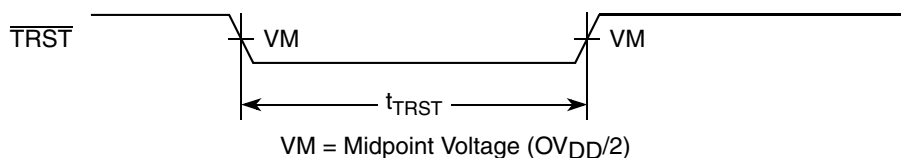

Figure 28. JTAG Clock Input Timing Diagram

Figure 29 provides the $\overline{TRST}$ timing diagram.


Figure 29. $\overline{TRST}$ Timing Diagram

13 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8347EA.

13.1 PCI DC Electrical Characteristics

Table 44 provides the DC electrical characteristics for the PCI interface of the MPC8347EA.

Table 44. PCI DC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH} \text{ (min) or } V_{OUT} \leq V_{OL} \text{ (max)}$	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}		-0.3	0.8	V
Input current	I_{IN}	$V_{IN}^1 = 0 \text{ V or } V_{IN} = OV_{DD}$	—	± 5	μA
High-level output voltage	V_{OH}	$OV_{DD} = \text{min, } I_{OH} = -100 \mu\text{A}$	$OV_{DD} - 0.2$	—	V
Low-level output voltage	V_{OL}	$OV_{DD} = \text{min, } I_{OL} = 100 \mu\text{A}$	—	0.2	V

Note:

1. The symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1.

13.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8347EA. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the device is configured as a host or agent device. Table 45 provides the PCI AC timing specifications at 66 MHz.

Table 45. PCI AC Timing Specifications at 66 MHz¹

Parameter	Symbol ²	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	6.0	ns	3
Output hold from clock	t_{PCKHOX}	1	—	ns	3
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	3, 4
Input setup to clock	t_{PCIVKH}	3.0	—	ns	3, 5

14.2 Timer AC Timing Specifications

Table 48 provides the timer input and output AC timing specifications.

Table 48. Timers Input AC Timing Specifications¹

Parameter	Symbol ²	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:

1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

15 GPIO

This section describes the DC and AC electrical specifications for the GPIO.

15.1 GPIO DC Electrical Characteristics

Table 49 provides the DC electrical characteristics for the MPC8347EA GPIO.

Table 49. GPIO DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	−0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	$I_{OH} = -8.0$ mA	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0$ mA	—	0.5	V
Output low voltage	V_{OL}	$I_{OL} = 3.2$ mA	—	0.4	V

15.2 GPIO AC Timing Specifications

Table 50 provides the GPIO input and output AC timing specifications.

Table 50. GPIO Input AC Timing Specifications¹

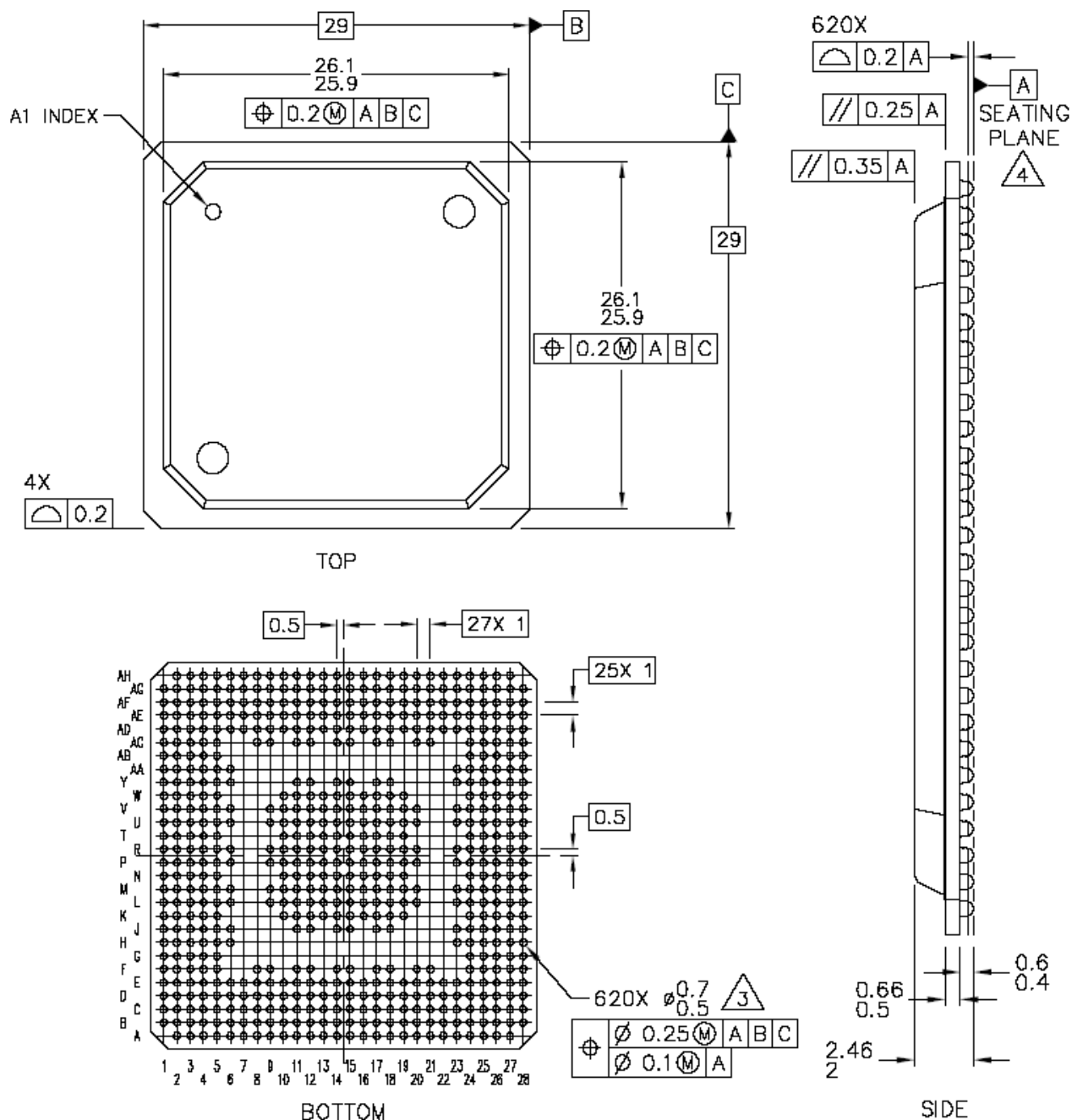
Parameter	Symbol ²	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:

1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by external synchronous logic. GPIO inputs must be valid for at least t_{PIWID} ns to ensure proper operation.

18.4 Mechanical Dimensions for the MPC8347EA PBGA

Figure 41 shows the mechanical dimensions and bottom surface nomenclature for the MPC8347EA, 620-PBGA package.



Notes:

1. All dimensions are in millimeters.
2. Dimensioning and tolerancing per ASME Y14. 5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

Figure 41. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC8347EA PBGA

Table 55. MPC8347EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MECC[0:4]/MSRCID[0:4]	W4, W3, Y3, AA6, T1	I/O	GV _{DD}	—
MECC[5]/MDVAL	U1	I/O	GV _{DD}	—
MECC[6:7]	Y1, Y6	I/O	GV _{DD}	—
MDM[0:8]	B1, F1, K1, R4, AD4, AJ1, AP3, AP7, Y4	O	GV _{DD}	—
MDQS[0:8]	B2, F5, J1, P2, AC1, AJ2, AN4, AL8, W2	I/O	GV _{DD}	—
MBA[0:1]	AD1, AA5	O	GV _{DD}	—
MA[0:14]	W1, U4, T3, R3, P1, M1, N1, L3, L1, K2, Y2, K3, J3, AP2, AN6	O	GV _{DD}	—
$\overline{MWE}$	AF1	O	GV _{DD}	—
$\overline{MRAS}$	AF4	O	GV _{DD}	—
$\overline{MCAS}$	AG3	O	GV _{DD}	—
MCS[0:3]	AG2, AG1, AK1, AL4	O	GV _{DD}	—
MCKE[0:1]	H3, G1	O	GV _{DD}	3
MCK[0:5]	U2, F4, AM3, V3, F2, AN3	O	GV _{DD}	—
$\overline{MCK}$ [0:5]	U3, E3, AN2, V4, E1, AM4	O	GV _{DD}	—
MODT[0:3]	AH3, AJ5, AH1, AJ4	O	GV _{DD}	—
MBA[2]	H4	O	GV _{DD}	—
MDIC0	AB1	I/O	—	10
MDIC1	AA1	I/O	—	10
Local Bus Controller Interface				
LAD[0:31]	AM13, AP13, AL14, AM14, AN14, AP14, AK15, AJ15, AM15, AN15, AP15, AM16, AL16, AN16, AP16, AL17, AM17, AP17, AK17, AP18, AL18, AM18, AN18, AP19, AN19, AM19, AP20, AK19, AN20, AL20, AP21, AN21	I/O	OV _{DD}	—
LDP[0]/ $\overline{CKSTOP_OUT}$	AM21	I/O	OV _{DD}	—
LDP[1]/ $\overline{CKSTOP_IN}$	AP22	I/O	OV _{DD}	—
LDP[2]/LCS[4]	AN22	I/O	OV _{DD}	—
LDP[3]/LCS[5]	AM22	I/O	OV _{DD}	—
LA[27:31]	AK21, AP23, AN23, AP24, AK22	O	OV _{DD}	—
$\overline{LCS}$ [0:3]	AN24, AL23, AP25, AN25	O	OV _{DD}	—
$\overline{LWE}$ [0:3]/LSDDQM[0:3]/ $\overline{LBS}$ [0:3]	AK23, AP26, AL24, AM25	O	OV _{DD}	—
LBCTL	AN26	O	OV _{DD}	—

Table 55. MPC8347EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
No Connection				
NC	W32, AA31, AA32, AA33, AA34, AB31, AB32, AB33, AB34, AC29, AC31, AC33, AC34, AD30, AD32, AD33, AD34, AE29, AE30, AH32, AH33, AH34, AM33, AJ31, AJ32, AJ33, AJ34, AK32, AK33, AK34, AM34, AL33, AL34, AK31, AH30, AC32, AE32, AH31, AL32, AG34, AE33, AF32, AE34, AF34, AF33, AG33, AG32, AL11, AM11, AP10, Y32, Y34, Y31, Y33	—	—	—

Notes:

1. This pin is an open-drain signal. A weak pull-up resistor (1 k Ω) should be placed on this pin to OV_{DD}.
2. This pin is an open-drain signal. A weak pull-up resistor (2–10 k Ω) should be placed on this pin to OV_{DD}.
3. During reset, this output is actively driven rather than three-stated.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull-up if the chip is in PCI host mode. Follow the PCI specifications.
6. This pin must always be tied to GND.
7. This pin must always be pulled up to OV_{DD}.
8. This pin must always be left not connected.
9. Thermal sensitive resistor.
10. It is recommended that MDIC0 be tied to GRD using an 18 Ω resistor and MDIC1 be tied to DDR power using an 18 Ω resistor.
11. TSEC1_TXD[3] is required an external pull-up resistor. For proper functionality of the device, this pin must be pulled up or actively driven high during a hard reset. No external pull-down resistors are allowed to be attached to this net.
12. A weak pull-up resistor (2–10 k Ω) should be placed on this pin to LV_{DD1}.
13. For systems that boot from local bus (GPCM)-controlled NOR flash, a pullup on LGPL4 is required.

Table 56 provides the pinout listing for the MPC8347EA, 620 PBGA package.

Table 56. MPC8347EA (PBGA) Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI				
PCI1_INTA/IRQ_OUT	D20	O	OV _{DD}	2
PCI1_RESET_OUT	B21	O	OV _{DD}	—
PCI1_AD[31:0]	E19, D17, A16, A18, B17, B16, D16, B18, E17, E16, A15, C16, D15, D14, C14, A12, D12, B11, C11, E12, A10, C10, A9, E11, E10, B9, B8, D9, A8, C9, D8, C8	I/O	OV _{DD}	—
PCI1_C/ $\overline{\text{BE}}$ [3:0]	A17, A14, A11, B10	I/O	OV _{DD}	—
PCI1_PAR	D13	I/O	OV _{DD}	—
PCI1_FRAME	B14	I/O	OV _{DD}	5

Table 56. MPC8347EA (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1_TRDY	A13	I/O	OV _{DD}	5
PCI1_IRDY	E13	I/O	OV _{DD}	5
PCI1_STOP	C13	I/O	OV _{DD}	5
PCI1_DEVSEL	B13	I/O	OV _{DD}	5
PCI1_IDSEL	C17	I	OV _{DD}	—
PCI1_SERR	C12	I/O	OV _{DD}	5
PCI1_PERR	B12	I/O	OV _{DD}	5
PCI1_REQ[0]	A21	I/O	OV _{DD}	
PCI1_REQ[1]/CPCI1_HS_ES	C19	I	OV _{DD}	—
PCI1_REQ[2:4]	C18, A19, E20	I	OV _{DD}	—
PCI1_GNT0	B20	I/O	OV _{DD}	—
PCI1_GNT1/CPCI1_HS_LED	C20	O	OV _{DD}	—
PCI1_GNT2/CPCI1_HS_ENUM	B19	O	OV _{DD}	—
PCI1_GNT[3:4]	A20, E18	O	OV _{DD}	—
M66EN	L26	I	OV _{DD}	—
DDR SDRAM Memory Interface				
MDQ[0:63]	AC25, AD27, AD25, AH27, AE28, AD26, AD24, AF27, AF25, AF28, AH24, AG26, AE25, AG25, AH26, AH25, AG22, AH22, AE21, AD19, AE22, AF23, AE19, AG20, AG19, AD17, AE16, AF16, AF18, AG18, AH17, AH16, AG9, AD12, AG7, AE8, AD11, AH9, AH8, AF6, AF8, AE6, AF1, AE4, AG8, AH3, AG3, AG4, AH2, AD7, AB4, AB3, AG1, AD5, AC2, AC1, AC4, AA3, Y4, AA4, AB1, AB2, Y5, Y3	I/O	GV _{DD}	—
MECC[0:4]/MSRCID[0:4]	AG13, AE14, AH12, AH10, AE15	I/O	GV _{DD}	—
MECC[5]/MDVAL	AH14	I/O	GV _{DD}	—
MECC[6:7]	AE13, AH11	I/O	GV _{DD}	—
MDM[0:8]	AG28, AG24, AF20, AG17, AE9, AH5, AD1, AA2, AG12	O	GV _{DD}	—
MDQS[0:8]	AE27, AE26, AE20, AH18, AG10, AF5, AC3, AA1, AH13	I/O	GV _{DD}	—
MBA[0:1]	AF10, AF11	O	GV _{DD}	—
MA[0:14]	AF13, AF15, AG16, AD16, AF17, AH20, AH19, AH21, AD18, AG21, AD13, AF21, AF22, AE1, AA5	O	GV _{DD}	—
MWE	AD10	O	GV _{DD}	—

19 Clocking

Figure 42 shows the internal distribution of the clocks.

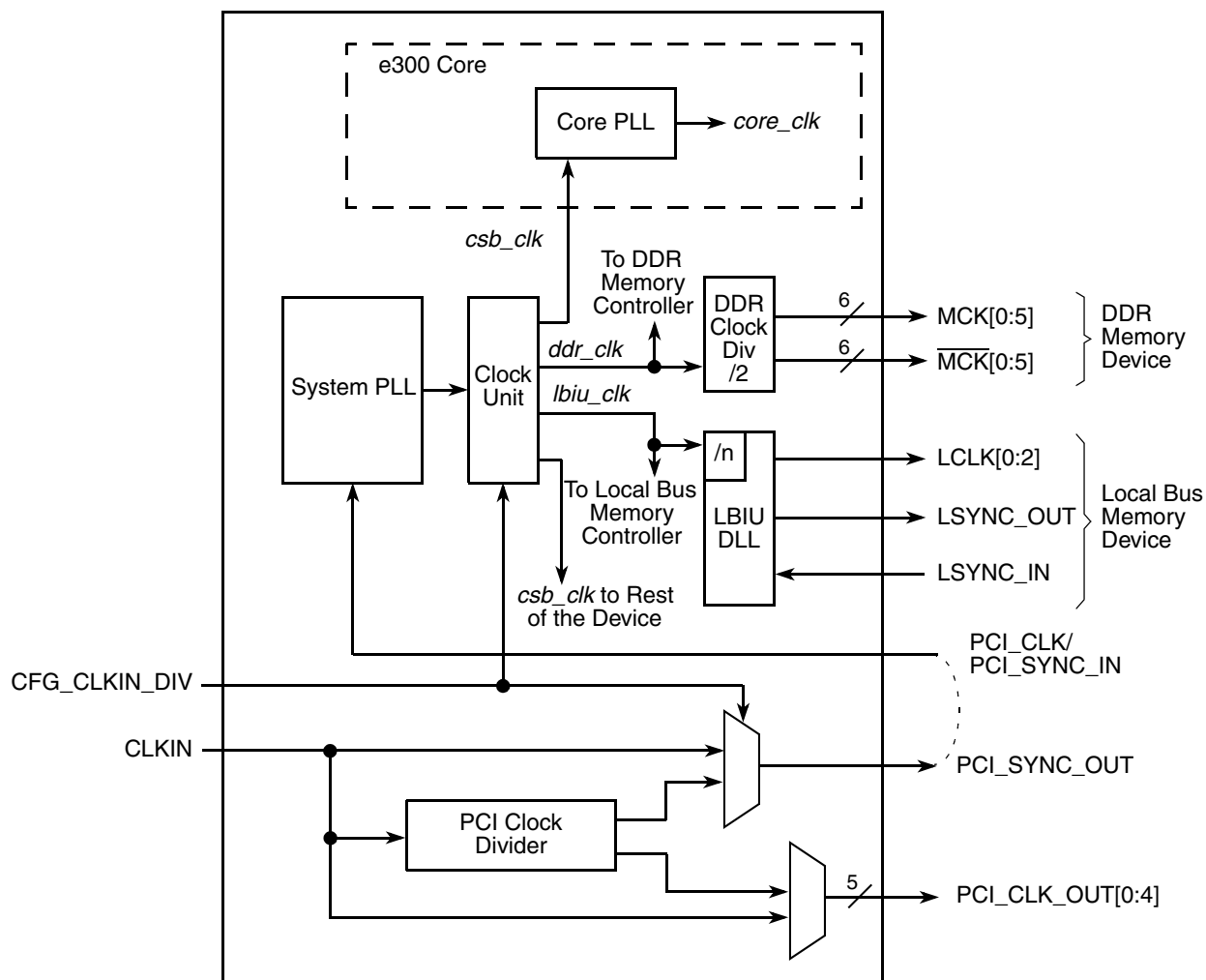


Figure 42. MPC8347EA Clock Subsystem

The primary clock source can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. When the MPC8347EA is configured as a PCI host device, CLKIN is its primary input clock. CLKIN feeds the PCI clock divider ($\div 2$) and the multiplexers for PCI_SYNC_OUT and PCI_CLK_OUT. The CFG_CLKIN_DIV configuration input selects whether CLKIN or CLKIN/2 is driven out on the PCI_SYNC_OUT signal. The OCCR[PCICDn] parameters select whether CLKIN or CLKIN/2 is driven out on the PCI_CLK_OUTn signals.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the MPC8347EA to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input clock and the CLKIN signal should be tied to GND.

[Addressed by This Document](#),” for part ordering details and contact your Freescale Sales Representative or authorized distributor for more information.

Table 58. Operating Frequencies for TBGA

Characteristic ¹	400 MHz	533 MHz	667 MHz	Unit
e300 core frequency (<i>core_clk</i>)	266–400	266–533	266–667	MHz
Coherent system bus frequency (<i>csb_clk</i>)	100–266	100–333	100–333	MHz
DDR1 memory bus frequency (MCK) ²	100–133	100–133	100–166.67	MHz
DDR2 memory bus frequency (MCK) ³	100–133	100–200	100–200	MHz
Local bus frequency (LCLK _n) ⁴	16.67–133	16.67–133	16.67–133	MHz
PCI input frequency (CLKIN or PCI_CLK)	25–66	25–66	25–66	MHz
Security core maximum internal operating frequency	133	133	166	MHz
USB_DR, USB_MPH maximum internal operating frequency	133	133	166	MHz

¹ The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen so that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies. The value of SCCR[ENCCM], SCCR[USBDRCM], and SCCR[USBMPHCM] must be programmed so that the maximum internal operating frequency of the Security core and USB modules does not exceed the respective values listed in this table.

² The DDR data rate is 2x the DDR memory bus frequency.

³ The DDR data rate is 2x the DDR memory bus frequency.

⁴ The local bus frequency is 1/2, 1/4, or 1/8 of the *lbiu_clk* frequency (depending on LCCR[CLKDIV]) which is in turn 1x or 2x the *csb_clk* frequency (depending on RCWL[LBIUCM]).

[Table 59](#) provides the operating frequencies for the MPC8347EA PBGA under recommended operating conditions.

Table 59. Operating Frequencies for PBGA

Parameter ¹	266 MHz	333 MHz	400 MHz	Unit
e300 core frequency (<i>core_clk</i>)	200–266	200–333	200–400	MHz
Coherent system bus frequency (<i>csb_clk</i>)	100–266			MHz
DDR1 memory bus frequency (MCK) ²	100–133			MHz
DDR2 memory bus frequency (MCK) ³	100–133			MHz
Local bus frequency (LCLK _n) ⁴	16.67–133			MHz
PCI input frequency (CLKIN or PCI_CLK)	25–66			MHz
Security core maximum internal operating frequency	133			MHz
USB_DR, USB_MPH maximum internal operating frequency	133			MHz

¹ The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen so that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies. The value of SCCR[ENCCM], SCCR[USBDRCM], and SCCR[USBMPHCM] must be programmed so that the maximum internal operating frequency of the Security core and USB modules does not exceed the respective values listed in this table.

² The DDR data rate is 2x the DDR memory bus frequency.

$OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N) \div 2$.

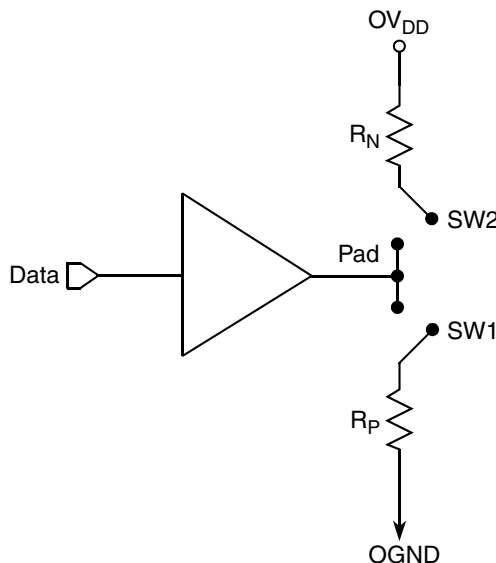


Figure 44. Driver Impedance Measurement

Two measurements give the value of this resistance and the strength of the driver current source. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term} . The measured voltage is $V_2 = (1 \div (1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1 \div V_2 - 1)$. The drive current is then $I_{source} = V_1 \div R_{source}$.

[Table 69](#) summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD} , nominal OV_{DD} , 105°C.

Table 69. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI Signals (Not Including PCI Output Clocks)	PCI Output Clocks (Including PCI_SYNC_OUT)	DDR DRAM	Symbol	Unit
R_N	42 Target	25 Target	42 Target	20 Target	Z_0	W
R_P	42 Target	25 Target	42 Target	20 Target	Z_0	W
Differential	NA	NA	NA	NA	Z_{DIFF}	W

Note: Nominal supply voltages. See [Table 1](#), $T_j = 105^\circ\text{C}$.

21.6 Configuration Pin Multiplexing

The MPC8347EA power-on configuration options can be set through external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see the customer-visible configuration pins). These pins are used as output only pins in normal operation.

parts including extended temperatures, refer to the device product summary page on our website listed on the back cover of this document or, contact your local Freescale sales office.

Table 70. Part Numbering Nomenclature

MPC	nnnn	e	t	pp	aa	a	r
Product Code	Part Identifier	Encryption Acceleration	Temperature ¹ Range	Package ²	Processor Frequency ³	Platform Frequency	Revision Level
MPC	8347	Blank = Not included E = included	Blank = 0 to 105°C C = -40 to 105°C	ZU = TBGA VV = PB free TBGA ZQ = PBGA VR = PB Free PBGA	e300 core speed AD = 266 AG = 400 AJ = 533 AL = 667	D = 266 F = 333 ⁴	B = 3.1

Notes:

1. For temperature range = C, processor frequency is limited to 400 (PBGA) with a platform frequency of 266 and up to 533 (TBGA) with a platform frequency of 333
2. See [Section 18, "Package and Pin Listings,"](#) for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.
4. ALF marked parts support DDR1 data rate up to 333 MHz (at 333 MHz CSB as the 'F' marking implies) and DDR2 data rate up to 400 MHz (at 200 MHz CSB). AJF marked parts support DDR1 and DDR2 data rate up to 333 MHz (at a CSB of 333 MHz).

[Table 71](#) shows the SVR settings by device and package type.

Table 71. SVR Settings

Device	Package	SVR (Rev. 3.0)
MPC8347EA	TBGA	8052_0030
MPC8347A	TBGA	8053_0030
MPC8347EA	PBGA	8054_0030
MPC8347A	PBGA	8055_0030