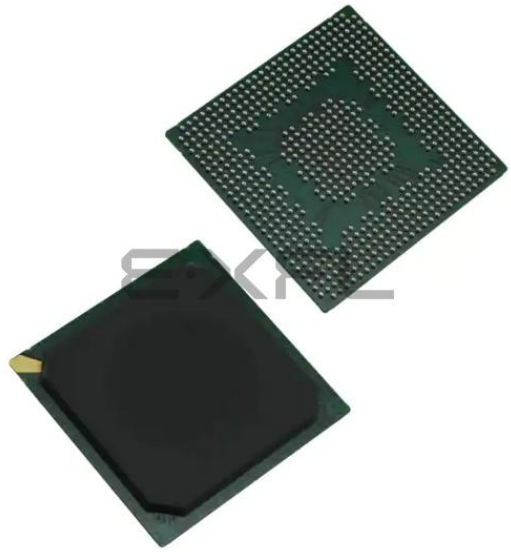

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8347ezqagd

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the device.

4.1 DC Electrical Characteristics

Table 6 provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the MPC8347EA.

Table 6. CLKIN DC Timing Specifications

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.7	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.4	V
CLKIN input current	$0 V \le V_{IN} \le OV_{DD}$	I_{IN}	—	±10	μA
PCI_SYNC_IN input current	$0 V \le V_{IN} \le 0.5 V$ or $OV_{DD} - 0.5 V \le V_{IN} \le OV_{DD}$	I_{IN}	—	±10	μA
PCI_SYNC_IN input current	$0.5 V \le V_{IN} \le OV_{DD} - 0.5 V$	I_{IN}	—	±50	μA

4.2 AC Electrical Characteristics

The primary clock source for the MPC8347EA can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Table 7 provides the clock input (CLKIN/PCI_CLK) AC timing specifications for the device.

Table 7. CLKIN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
CLKIN/PCI_CLK frequency	f_{CLKIN}	—	—	66	MHz	1, 6
CLKIN/PCI_CLK cycle time	t_{CLKIN}	15	—	—	ns	—
CLKIN/PCI_CLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.3	ns	2
CLKIN/PCI_CLK duty cycle	t_{KHK}/t_{CLKIN}	40	—	60	%	3
CLKIN/PCI_CLK jitter	—	—	—	±150	ps	4, 5

Notes:

1. **Caution:** The system, core, USB, security, and TSEC must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for CLKIN/PCI_CLK are measured at 0.4 and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The CLKIN/PCI_CLK driver's closed loop jitter bandwidth should be < 500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.
6. Spread spectrum clocking is allowed with 1% input frequency down-spread at maximum 50 KHz modulation rate regardless of input frequency.

8.1.1 TSEC DC Electrical Characteristics

GMII, MII, TBI, RGMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 23 and Table 24. The RGMII and RTBI signals in Table 24 are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 23. GMII/TBI and MII DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	LV_{DD}[2]	—		2.97	3.63	V
Output high voltage	V_{OH}	I_{OH} = –4.0 mA	LV_{DD} = Min	2.40	LV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 4.0 mA	LV_{DD} = Min	GND	0.50	V
Input high voltage	V_{IH}	—	—	2.0	LV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	—	–0.3	0.90	V
Input high current	I_{IH}	V_{IN}[1] = LV_{DD}		—	40	μA
Input low current	I_{IL}	V_{IN}[1] = GND		–600	—	μA

Notes:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.
2. GMII/MII pins not needed for RGMII or RTBI operation are powered by the OV_{DD} supply.

Table 24. RGMII/RTBI (When Operating at 2.5 V) DC Electrical Characteristics

Parameters	Symbol	Conditions		Min	Max	Unit
Supply voltage 2.5 V	LV_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	LV_{DD} = Min	2.00	LV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	LV_{DD} = Min	GND – 0.3	0.40	V
Input high voltage	V_{IH}	—	LV_{DD} = Min	1.7	LV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	LV_{DD} = Min	–0.3	0.70	V
Input high current	I_{IH}	V_{IN}[1] = LV_{DD}		—	10	μA
Input low current	I_{IL}	V_{IN}[1] = GND		–15	—	μA

Note:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

8.2 GMII, MII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

8.2.1 GMII Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

8.2.1.1 GMII Transmit AC Timing Specifications

Table 25 provides the GMII transmit AC timing specifications.

Table 25. GMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
GTX_CLK clock period	t_{GTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{GTXH}/t_{GTX}	43.75	—	56.25	%
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX}	0.5	—	5.0	ns
GTX_CLK clock rise time (20%–80%)	t_{GTXR}	—	—	1.0	ns
GTX_CLK clock fall time (80%–20%)	t_{GTXF}	—	—	1.0	ns

Notes:

1. The symbols for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 9 shows the GMII transmit AC timing diagram.

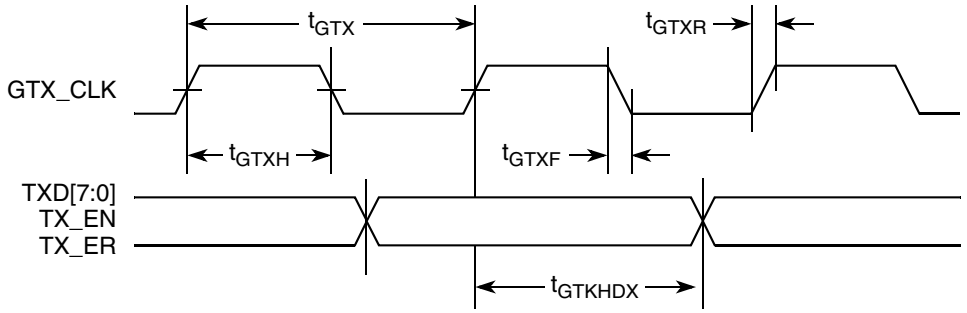

Figure 9. GMII Transmit AC Timing Diagram

8.2.1.2 GMII Receive AC Timing Specifications

Table 26 provides the GMII receive AC timing specifications.

Table 26. GMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
RX_CLK clock period	t_{GRX}	—	8.0	—	ns
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	40	—	60	%
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0.5	—	—	ns

8.2.3.1 TBI Transmit AC Timing Specifications

Table 29 provides the TBI transmit AC timing specifications.

Table 29. TBI Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
GTX_CLK clock period	t_{TTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{TTXH}/t_{TTX}	40	—	60	%
GTX_CLK to TBI data TXD[7:0], TX_ER, TX_EN delay	t_{TTKHDX}	1.0	—	5.0	ns
GTX_CLK clock rise (20%–80%)	t_{TTXR}	—	—	1.0	ns
GTX_CLK clock fall time (80%–20%)	t_{TTXF}	—	—	1.0	ns

Notes:

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 14 shows the TBI transmit AC timing diagram.

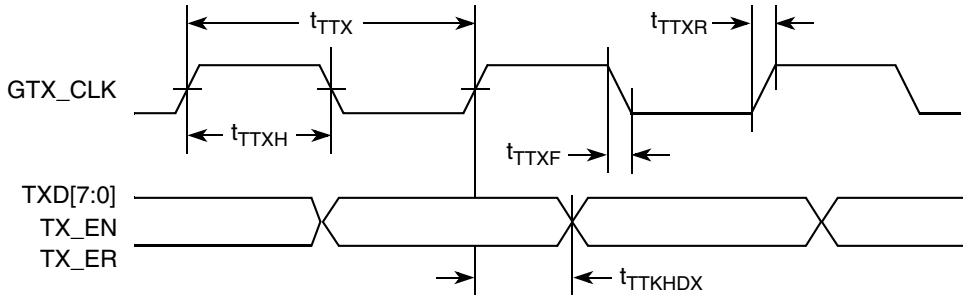

Figure 14. TBI Transmit AC Timing Diagram

8.2.3.2 TBI Receive AC Timing Specifications

Table 30 provides the TBI receive AC timing specifications.

Table 30. TBI Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
PMA_RX_CLK clock period	t_{TRX}		16.0		ns
PMA_RX_CLK skew	t_{SKTRX}	7.5	—	8.5	ns
RX_CLK duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%

Table 32. MII Management DC Electrical Characteristics Powered at 2.5 V (continued)

Parameter	Symbol	Conditions	Min	Max	Unit
Input high current	I_{IH}	V_{IN}[1] = LV_{DD}	—	10	μA
Input low current	I_{IL}	V_{IN} = LV_{DD}	–15	—	μA

Note:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

Table 33. MII Management DC Electrical Characteristics Powered at 3.3 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	LV_{DD}	—		2.97	3.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	LV_{DD} = Min	2.10	LV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	LV_{DD} = Min	GND	0.50	V
Input high voltage	V_{IH}	—		2.00	—	V
Input low voltage	V_{IL}	—		—	0.80	V
Input high current	I_{IH}	LV_{DD} = Max	V_{IN}[1] = 2.1 V	—	40	μA
Input low current	I_{IL}	LV_{DD} = Max	V_{IN} = 0.5 V	–600	—	μA

Note:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

8.3.2 MII Management AC Electrical Specifications

Table 34 provides the MII management AC timing specifications.

Table 34. MII Management AC Timing Specifications

At recommended operating conditions with LV_{DD} is 3.3 V ± 10% or 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	10	—	70	ns	3
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—

9 USB

This section provides the AC and DC electrical specifications for the USB interface of the MPC8347EA.

9.1 USB DC Electrical Characteristics

Table 35 provides the DC electrical characteristics for the USB interface.

Table 35. USB DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current	I_{IN}	—	±5	μA
High-level output voltage, I_{OH} = –100 μA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V

9.2 USB AC Electrical Specifications

Table 36 describes the general timing parameters of the USB interface of the MPC8347EA.

Table 36. USB General Timing Parameters (ULPI Mode Only)

Parameter	Symbol[1]	Min	Max	Unit	Notes
USB clock cycle time	t_{USCK}	15	—	ns	2–5
Input setup to USB clock—all inputs	t_{USIVKH}	4	—	ns	2–5
Input hold to USB clock—all inputs	t_{USIXKH}	1	—	ns	2–5
USB clock to output valid—all outputs	t_{USKHOV}	—	7	ns	2–5
Output hold from USB clock—all outputs	t_{USKHOX}	2	—	ns	2–5

Notes:

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes USB timing (US) for the USB clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to USB clock.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of the USB clock to 0.4 × OV_{DD} of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

Figure 18 and Figure 19 provide the AC test load and signals for the USB, respectively.

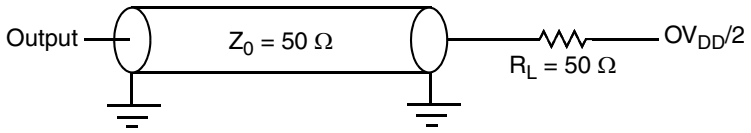

Figure 18. USB AC Test Load

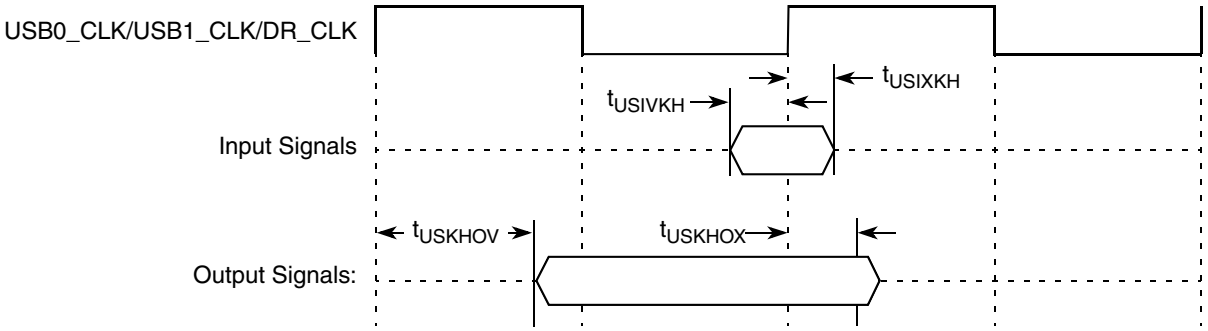

Figure 19. USB Signals

10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8347EA.

10.1 Local Bus DC Electrical Characteristics

Table 37 provides the DC electrical characteristics for the local bus interface.

Table 37. Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current	I_{IN}	—	±5	μA
High-level output voltage, I_{OH} = –100 μA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V

Figure 21 through Figure 26 show the local bus signals.

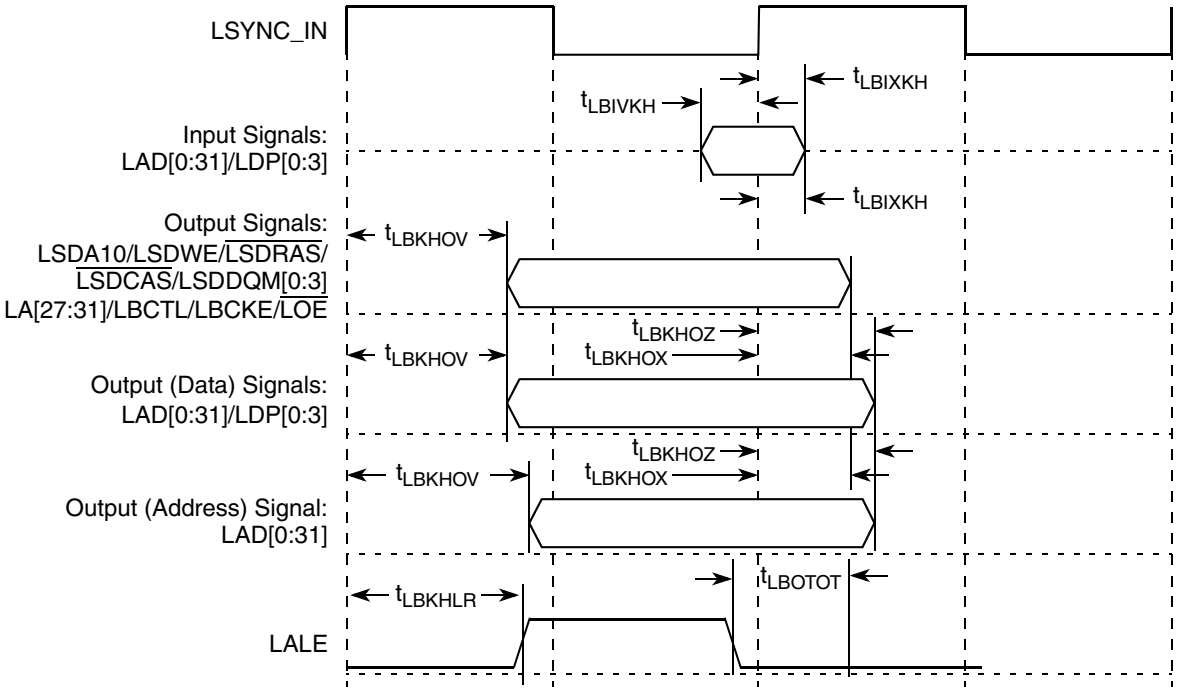

Figure 21. Local Bus Signals, Nonspecial Signals Only (DLL Enabled)

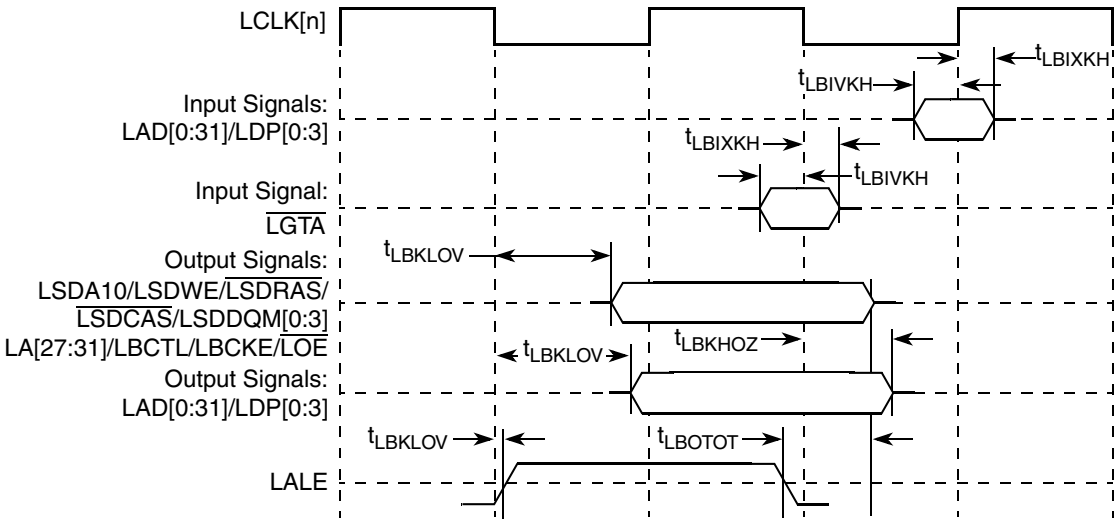

Figure 22. Local Bus Signals, Nonspecial Signals Only (DLL Bypass Mode)

Table 40. JTAG Interface DC Electrical Characteristics (continued)

Parameter	Symbol	Condition	Min	Max	Unit
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

11.2 JTAG AC Timing Specifications

This section describes the AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8347EA. Table 41 provides the JTAG AC timing specifications as defined in Figure 28 through Figure 31.

Table 41. JTAG AC Timing Specifications (Independent of CLKIN)[1]

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR}, t_{JTGF}	0	2	ns	—
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 4	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 10 10	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 2 2	 11 11	ns	5
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 2 2	 — —	ns	5

13 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8347EA.

13.1 PCI DC Electrical Characteristics

Table 44 provides the DC electrical characteristics for the PCI interface of the MPC8347EA.

Table 44. PCI DC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}$ (min) or	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL}$ (max)	–0.3	0.8	V
Input current	I_{IN}	V_{IN}[1]= 0 V or $V_{IN} = OV_{DD}$	—	±5	μA
High-level output voltage	V_{OH}	OV_{DD} = min, I_{OH} = –100 μA	OV_{DD} – 0.2	—	V
Low-level output voltage	V_{OL}	OV_{DD} = min, I_{OL} = 100 μA	—	0.2	V

Note:
1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1.

13.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8347EA. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the device is configured as a host or agent device. Table 45 provides the PCI AC timing specifications at 66 MHz.

Table 45. PCI AC Timing Specifications at 66 MHz[1]

Parameter	Symbol[2]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	6.0	ns	3
Output hold from clock	t_{PCKHOX}	1	—	ns	3
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	3, 4
Input setup to clock	t_{PCIVKH}	3.0	—	ns	3, 5

Figure 35 shows the PCI input AC timing diagram.

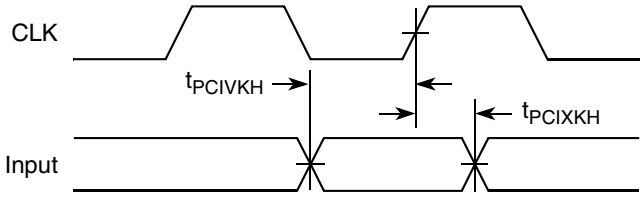

Figure 35. PCI Input AC Timing Diagram

Figure 36 shows the PCI output AC timing diagram.

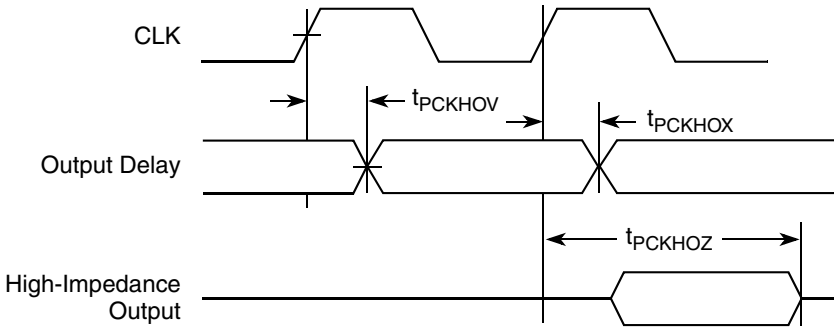

Figure 36. PCI Output AC Timing Diagram

14 Timers

This section describes the DC and AC electrical specifications for the timers.

14.1 Timer DC Electrical Characteristics

Table 47 provides the DC electrical characteristics for the MPC8347EA timer pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_CLK.

Table 47. Timer DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

18.3 Package Parameters for the MPC8347EA PBGA

The package parameters are as provided in the following list. The package type is 29 mm × 29 mm, 620 plastic ball grid array (PBGA).

Package outline	29 mm × 29 mm
Interconnects	620
Pitch	1.00 mm
Module height (maximum)	2.46 mm
Module height (typical)	2.23 mm
Module height (minimum)	2.00 mm
Solder balls	62 Sn/36 Pb/2 Ag (ZQ package) 96.5 Sn/3.5Ag (VR package)
Ball diameter (typical)	0.60 mm

Table 55. MPC8347EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MECC[0:4]/MSRCID[0:4]	W4, W3, Y3, AA6, T1	I/O	GV_{DD}	—
MECC[5]/MDVAL	U1	I/O	GV_{DD}	—
MECC[6:7]	Y1, Y6	I/O	GV_{DD}	—
MDM[0:8]	B1, F1, K1, R4, AD4, AJ1, AP3, AP7, Y4	O	GV_{DD}	—
MDQS[0:8]	B2, F5, J1, P2, AC1, AJ2, AN4, AL8, W2	I/O	GV_{DD}	—
MBA[0:1]	AD1, AA5	O	GV_{DD}	—
MA[0:14]	W1, U4, T3, R3, P1, M1, N1, L3, L1, K2, Y2, K3, J3, AP2, AN6	O	GV_{DD}	—
$\overline{\text{MWE}}$	AF1	O	GV_{DD}	—
$\overline{\text{MRAS}}$	AF4	O	GV_{DD}	—
$\overline{\text{MCAS}}$	AG3	O	GV_{DD}	—
$\overline{\text{MCS}}$[0:3]	AG2, AG1, AK1, AL4	O	GV_{DD}	—
MCKE[0:1]	H3, G1	O	GV_{DD}	3
MCK[0:5]	U2, F4, AM3, V3, F2, AN3	O	GV_{DD}	—
$\overline{\text{MCK}}$[0:5]	U3, E3, AN2, V4, E1, AM4	O	GV_{DD}	—
MODT[0:3]	AH3, AJ5, AH1, AJ4	O	GV_{DD}	—
MBA[2]	H4	O	GV_{DD}	—
MDIC0	AB1	I/O	—	10
MDIC1	AA1	I/O	—	10
Local Bus Controller Interface				
LAD[0:31]	AM13, AP13, AL14, AM14, AN14, AP14, AK15, AJ15, AM15, AN15, AP15, AM16, AL16, AN16, AP16, AL17, AM17, AP17, AK17, AP18, AL18, AM18, AN18, AP19, AN19, AM19, AP20, AK19, AN20, AL20, AP21, AN21	I/O	OV_{DD}	—
LDP[0]/$\overline{\text{CKSTOP\_OUT}}$	AM21	I/O	OV_{DD}	—
LDP[1]/$\overline{\text{CKSTOP\_IN}}$	AP22	I/O	OV_{DD}	—
LDP[2]/$\overline{\text{LCS}}$[4]	AN22	I/O	OV_{DD}	—
LDP[3]/$\overline{\text{LCS}}$[5]	AM22	I/O	OV_{DD}	—
LA[27:31]	AK21, AP23, AN23, AP24, AK22	O	OV_{DD}	—
$\overline{\text{LCS}}$[0:3]	AN24, AL23, AP25, AN25	O	OV_{DD}	—
$\overline{\text{LWE}}$[0:3]/LSDDQM[0:3]/$\overline{\text{LBS}}$[0:3]	AK23, AP26, AL24, AM25	O	OV_{DD}	—
LBCTL	AN26	O	OV_{DD}	—

Table 55. MPC8347EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC2_TXD[3:0]/GPIO1[17:20]	B5, A5, F8, B6	I/O	LV_{DD2}	—
TSEC2_TX_ER/GPIO1[24]	F14	I/O	OV_{DD}	—
TSEC2_TX_EN/GPIO1[12]	C5	I/O	LV_{DD2}	3
TSEC2_TX_CLK/GPIO1[30]	E14	I/O	OV_{DD}	—
DUART				
UART_SOUT[1:2]/MSRCID[0:1]/LSRCID[0:1]	AK27, AN29	O	OV_{DD}	—
UART_SIN[1:2]/MSRCID[2:3]/LSRCID[2:3]	AL28, AM29	I/O	OV_{DD}	—
$\overline{\text{UART\_CTS}}$[1]/MSRCID4/LSRCID4	AP30	I/O	OV_{DD}	—
$\overline{\text{UART\_CTS}}$[2]/MDVAL/ LDVAL	AN30	I/O	OV_{DD}	—
$\overline{\text{UART\_RTS}}$[1:2]	AP31, AM30	O	OV_{DD}	—
I^2C interface				
IIC1_SDA	AK29	I/O	OV_{DD}	2
IIC1_SCL	AP32	I/O	OV_{DD}	2
IIC2_SDA	AN31	I/O	OV_{DD}	2
IIC2_SCL	AM31	I/O	OV_{DD}	2
SPI				
SPIMOSI/$\overline{\text{LCS}}$[6]	AN32	I/O	OV_{DD}	—
SPIMISO/$\overline{\text{LCS}}$[7]	AP33	I/O	OV_{DD}	—
SPICLK	AK30	I/O	OV_{DD}	—
SPISEL	AL31	I	OV_{DD}	—
Clocks				
PCI_CLK_OUT[0:2]	AN9, AP9, AM10	O	OV_{DD}	—
PCI_CLK_OUT[3]/$\overline{\text{LCS}}$[6]	AN10	O	OV_{DD}	—
PCI_CLK_OUT[4]/$\overline{\text{LCS}}$[7]	AJ11	O	OV_{DD}	—
PCI_SYNC_IN/PCI_CLOCK	AK12	I	OV_{DD}	—
PCI_SYNC_OUT	AP11	O	OV_{DD}	3
RTC/PIT_CLOCK	AM32	I	OV_{DD}	—
CLKIN	AM9	I	OV_{DD}	—
JTAG				
TCK	E20	I	OV_{DD}	—
TDI	F20	I	OV_{DD}	4
TDO	B20	O	OV_{DD}	3
TMS	A20	I	OV_{DD}	4
$\overline{\text{TRST}}$	B19	I	OV_{DD}	4

Table 56. MPC8347EA (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MRAS	AF7	O	GV_{DD}	—
$\overline{\text{MCAS}}$	AG6	O	GV_{DD}	—
$\overline{\text{MCS}}$[0:3]	AE7, AH7, AH4, AF2	O	GV_{DD}	—
MCKE[0:1]	AG23, AH23	O	GV_{DD}	3
MCK[0:5]	AH15, AE24, AE2, AF14, AE23, AD3	O	GV_{DD}	—
$\overline{\text{MCK}}$[0:5]	AG15, AD23, AE3, AG14, AF24, AD2	O	GV_{DD}	—
MODT[0:3]	AG5, AD4, AH6, AF4	O	GV_{DD}	—
MBA[2]	AD22	O	GV_{DD}	—
MDIC0	AG11	I/O	—	9
MDIC1	AF12	I/O	—	9
Local Bus Controller Interface				
LAD[0:31]	T4, T5, T1, R2, R3, T2, R1, R4, P1, P2, P3, P4, N1, N4, N2, N3, M1, M2, M3, N5, M4, L1, L2, L3, K1, M5, K2, K3, J1, J2, L5, J3	I/O	OV_{DD}	—
LDP[0]/$\overline{\text{CKSTOP\_OUT}}$	H1	I/O	OV_{DD}	—
LDP[1]/$\overline{\text{CKSTOP\_IN}}$	K5	I/O	OV_{DD}	—
LDP[2]/$\overline{\text{LCS}}$[4]	H2	I/O	OV_{DD}	—
LDP[3]/$\overline{\text{LCS}}$[5]	G1	I/O	OV_{DD}	—
LA[27:31]	J4, H3, G2, F1, G3	O	OV_{DD}	—
$\overline{\text{LCS}}$[0:3]	J5, H4, F2, E1	O	OV_{DD}	—
$\overline{\text{LWE}}$[0:3]/LSDDQM[0:3]/$\overline{\text{LBS}}$[0:3]	F3, G4, D1, E2	O	OV_{DD}	—
LBCTL	H5	O	OV_{DD}	—
LALE	E3	O	OV_{DD}	—
LGPL0/LSDA10/cfg_reset_source0	F4	I/O	OV_{DD}	—
LGPL1/$\overline{\text{LSDWE}}$/cfg_reset_source1	D2	I/O	OV_{DD}	—
LGPL2/$\overline{\text{LSDRAS}}$/$\overline{\text{LOE}}$	C1	O	OV_{DD}	—
LGPL3/$\overline{\text{LSDCAS}}$/cfg_reset_source2	C2	I/O	OV_{DD}	—
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE	C3	I/O	OV_{DD}	12
LGPL5/cfg_clkin_div	B3	I/O	OV_{DD}	—
LCKE	E4	O	OV_{DD}	—
LCLK[0:2]	D4, A3, C4	O	OV_{DD}	—
LSYNC_OUT	U3	O	OV_{DD}	—
LSYNC_IN	Y2	I	OV_{DD}	—

19 Clocking

Figure 42 shows the internal distribution of the clocks.

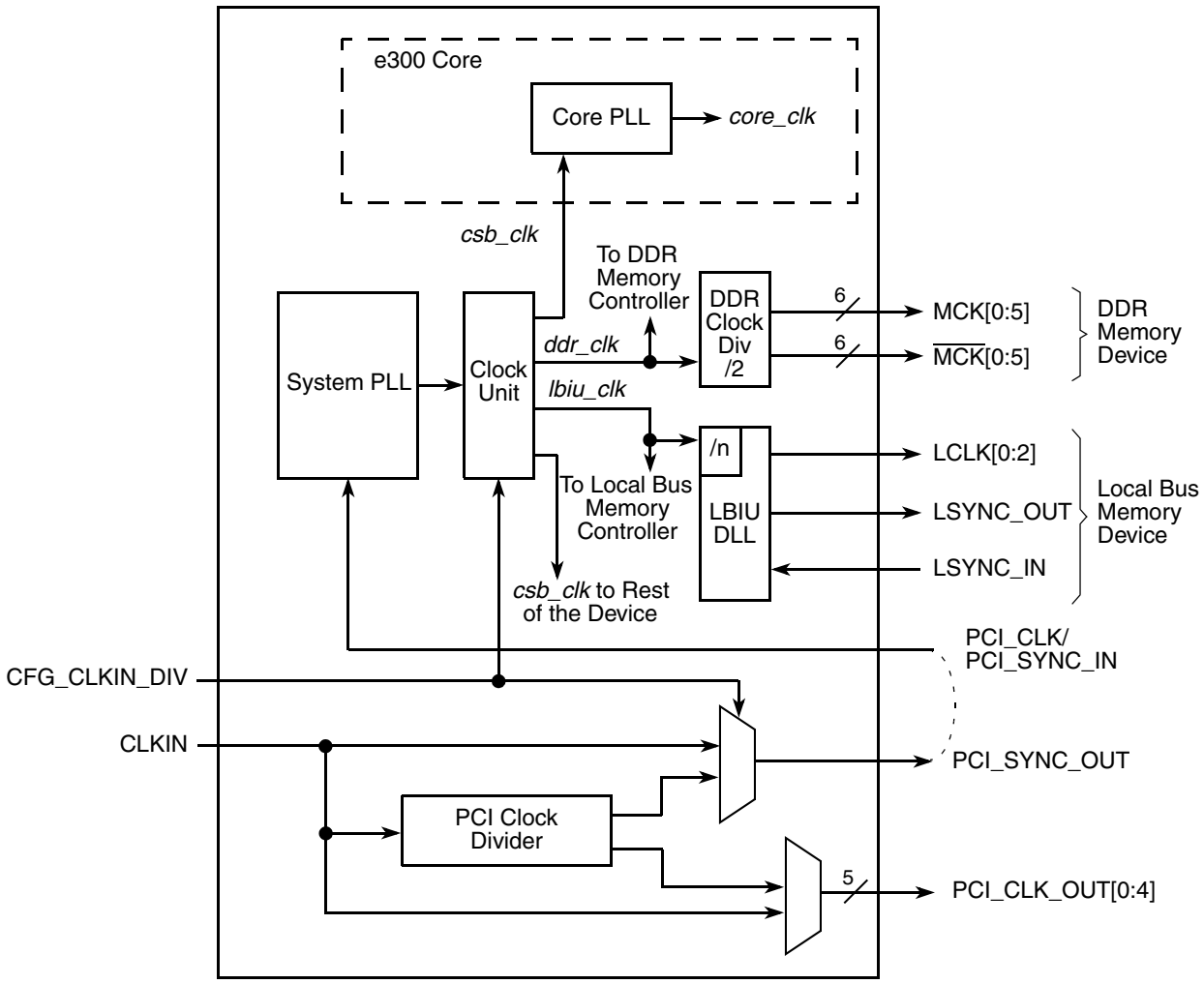

Figure 42. MPC8347EA Clock Subsystem

The primary clock source can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. When the MPC8347EA is configured as a PCI host device, CLKIN is its primary input clock. CLKIN feeds the PCI clock divider (÷2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The CFG_CLKIN_DIV configuration input selects whether CLKIN or CLKIN/2 is driven out on the PCI_SYNC_OUT signal. The OCCR[PCICD*n*] parameters select whether CLKIN or CLKIN/2 is driven out on the PCI_CLK_OUT*n* signals.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the MPC8347EA to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input clock and the CLKIN signal should be tied to GND.

VCO divider must be set properly so that the core VCO frequency is in the range of 800–1800 MHz.

Table 63. e300 Core PLL Configuration

RCWL[COREPLL]			*core_clk* : *csb_clk* Ratio	VCO Divider[1]
0–1	**2–5**	**6**		
nn	**0000**	n	PLL bypassed (PLL off, *csb_clk* clocks core directly)	PLL bypassed (PLL off, *csb_clk* clocks core directly)
00	**0001**	0	1:1	2
01	**0001**	0	1:1	4
10	**0001**	0	1:1	8
11	**0001**	0	1:1	8
00	**0001**	1	1.5:1	2
01	**0001**	1	1.5:1	4
10	**0001**	1	1.5:1	8
11	**0001**	1	1.5:1	8
00	**0010**	0	2:1	2
01	**0010**	0	2:1	4
10	**0010**	0	2:1	8
11	**0010**	0	2:1	8
00	**0010**	1	2.5:1	2
01	**0010**	1	2.5:1	4
10	**0010**	1	2.5:1	8
11	**0010**	1	2.5:1	8
00	**0011**	0	3:1	2
01	**0011**	0	3:1	4
10	**0011**	0	3:1	8
11	**0011**	0	3:1	8

1 Core VCO frequency = core frequency × VCO divider. The VCO divider must be set properly so that the core VCO frequency is in the range of 800–1800 MHz.

20.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature and a measure of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per the JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

20.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

Some application environments require a heat sink to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

The thermal performance of devices with heat sinks has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572

20.3 Heat Sink Attachment

When heat sinks are attached, an interface material is required, preferably thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces that can lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. The recommended maximum force on the top of the package is 10 lb force (4.5 kg force). Any adhesive attachment should attach to painted or plastic surfaces, and its performance should be verified under the application requirements.

20.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimize the size of the clearance to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

T_J = junction temperature (°C)

T_C = case temperature of the package (°C)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

P_D = power dissipation (W)

capacitive loads. This noise must be prevented from reaching other components in the MPC8347EA system, and the device itself requires a clean, tightly regulated source of power. Therefore, the system designer should place at least one decoupling capacitor at each V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pin of the device. These capacitors should receive their power from separate V_{DD}, OV_{DD}, GV_{DD}, LV_{DD}, and GND power planes in the PCB, with short traces to minimize inductance. Capacitors can be placed directly under the device using a standard escape pattern. Others can surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, distribute several bulk storage capacitors around the PCB, feeding the V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are 100–330 µF (AVX TPS tantalum or Sanyo OSCON).

21.4 Connection Recommendations

To ensure reliable operation, connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD}, GV_{DD}, or LV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, GV_{DD}, LV_{DD}, OV_{DD}, and GND pins of the MPC8347EA.

21.5 Output Buffer DC Impedance

The MPC8347EA drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 44). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals