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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	672-LBGA
Supplier Device Package	672-LBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8347ezuagdb

- Up to four physical banks (chip selects), each bank up to 1 Gbyte independently addressable
- DRAM chip configurations from 64 Mbits to 1 Gbit with ×8/×16 data ports
- Full error checking and correction (ECC) support
- Support for up to 16 simultaneous open pages (up to 32 pages for DDR2)
- Contiguous or discontiguous memory mapping
- Read-modify-write support
- Sleep-mode support for SDRAM self refresh
- Auto refresh
- On-the-fly power management using CKE
- Registered DIMM support
- 2.5-V SSTL2 compatible I/O for DDR1, 1.8-V SSTL2 compatible I/O for DDR2

- Dual three-speed (10/100/1000) Ethernet controllers (TSECs)
  - Dual controllers designed to comply with IEEE 802.3™, 802.3u™, 820.3x™, 802.3z™, 802.3ac™ standards
  - Ethernet physical interfaces:
    - 1000 Mbps IEEE Std. 802.3 GMII/RGMII, IEEE Std. 802.3z TBI/RTBI, full-duplex
    - 10/100 Mbps IEEE Std. 802.3 MII full- and half-duplex
  - Buffer descriptors are backward-compatible with MPC8260 and MPC860T 10/100 programming models
  - 9.6-Kbyte jumbo frame support
  - RMON statistics support
  - Internal 2-Kbyte transmit and 2-Kbyte receive FIFOs per TSEC module
  - MII management interface for control and status
  - Programmable CRC generation and checking
- PCI interface
  - Designed to comply with *PCI Specification Revision 2.3*
  - Data bus width:
    - 32-bit data PCI interface operating at up to 66 MHz
  - PCI 3.3-V compatible
  - PCI host bridge capabilities
  - PCI agent mode on PCI interface
  - PCI-to-memory and memory-to-PCI streaming
  - Memory prefetching of PCI read accesses and support for delayed read transactions
  - Posting of processor-to-PCI and PCI-to-memory writes
  - On-chip arbitration supporting five masters on PCI
  - Accesses to all PCI address spaces
  - Parity supported
  - Selectable hardware-enforced coherency

4.3 TSEC Gigabit Reference Clock Timing

Table 8 provides the TSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications.

Table 8. EC_GTX_CLK125 AC Timing Specifications

At recommended operating conditions with LV_{DD} = 2.5 ± 0.125 mV/ 3.3 V ± 165 mV

Parameter	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	t_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK125 rise and fall time LV_{DD} = 2.5 V LV_{DD} = 3.3 V	t_{G125R}/t_{G125F}	—	—	 0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	 45 47	—	 55 53	%	2
EC_GTX_CLK125 jitter	—	—	—	±150	ps	2

Notes:

1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for LV_{DD} = 2.5 V and from 0.6 and 2.7 V for LV_{DD} = 3.3 V.
2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. The EC_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 8.2.4, “RGMII and RTBI AC Timing Specifications for the duty cycle for 10Base-T and 100Base-T reference clock.

5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8347EA.

5.1 RESET DC Electrical Characteristics

Table 9 provides the DC electrical characteristics for the RESET pins of the MPC8347EA.

Table 9. RESET Pins DC Electrical Characteristics[1]

Parameter	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage[2]	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V

Table 9. RESET Pins DC Electrical Characteristics[1] (continued)

Parameter	Symbol	Condition	Min	Max	Unit
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Notes:
1. This table applies for pins $\overline{\text{PORESET}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, and $\overline{\text{QUIESCE}}$.
2. $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are open drain pins, thus V_{OH} is not relevant for those pins.

5.2 RESET AC Electrical Characteristics

Table 10 provides the reset initialization AC timing specifications of the MPC8347EA.

Table 10. RESET Initialization Timing Specifications

Parameter	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$ or $\overline{\text{SRESET}}$ (input) to activate reset flow	32	—	$t_{PCI\_SYNC\_IN}$	1
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to CLKIN when the MPC8347EA is in PCI host mode	32	—	t_{CLKIN}	2
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to PCI_SYNC_IN when the MPC8347EA is in PCI agent mode	32	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{\text{HRESET}}$/$\overline{\text{SRESET}}$ assertion (output)	512	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{\text{HRESET}}$ negation to $\overline{\text{SRESET}}$ negation (output)	16	—	$t_{PCI\_SYNC\_IN}$	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the MPC8347EA is in PCI host mode	4	—	t_{CLKIN}	2
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the MPC8347EA is in PCI agent mode	4	—	$t_{PCI\_SYNC\_IN}$	1
Input hold time for POR configuration signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	—
Time for the MPC8347EA to turn off POR configuration signals with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the MPC8347EA to turn on POR configuration signals with respect to the negation of $\overline{\text{HRESET}}$	1	—	$t_{PCI\_SYNC\_IN}$	1, 3

Notes:
1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. In PCI host mode, the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual*.
2. t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is valid only in PCI host mode. See the *MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual*.
3. POR configuration signals consist of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

Table 11 lists the PLL and DLL lock times.

Table 11. PLL and DLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	μs	—
DLL lock times	7680	122,880	csb_clk cycles	1, 2

Notes:
1. DLL lock times are a function of the ratio between the output clock and the coherency system bus clock (csb_clk). A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.
2. The csb_clk is determined by the CLKIN and system PLL ratio. See Section 19, "Clocking."

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8347EA. Note that DDR SDRAM is GV_{DD}(typ) = 2.5 V and DDR2 SDRAM is GV_{DD}(typ) = 1.8 V. The AC electrical specifications are the same for DDR and DRR2 SDRAM.

NOTE

The information in this document is accurate for revision 3.0 silicon and later. For information on revision 1.1 silicon and earlier versions see the *MPC8347E PowerQUICC II Pro Integrated Host Processor Hardware Specifications*. See Section 22.1, "Part Numbers Fully Addressed by This Document," for silicon revision level determination.

6.1 DDR and DDR2 SDRAM DC Electrical Characteristics

Table 12 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8347EA when GV_{DD}(typ) = 1.8 V.

Table 12. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.71	1.89	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.125	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.125	V	—
Output leakage current	I_{OZ}	–9.9	9.9	μA	4
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA	—

Table 27. MII Transmit AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
TX_CLK data clock rise (20%–80%)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall (80%–20%)	t_{MTXF}	1.0	—	4.0	ns

Note:

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). In general, the clock reference symbol is based on two to three letters representing the clock of a particular function. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 11 shows the MII transmit AC timing diagram.

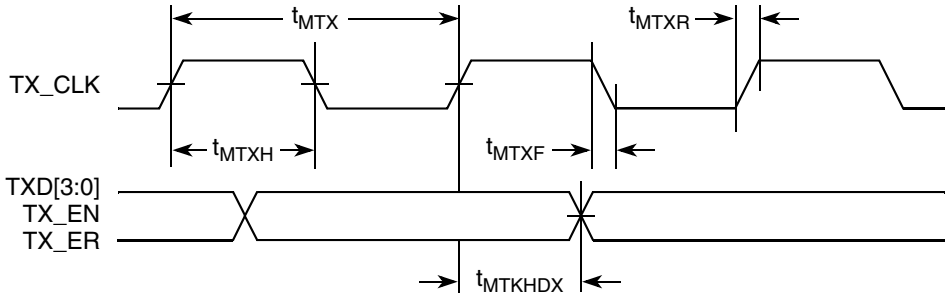


Figure 11. MII Transmit AC Timing Diagram

8.2.2.2 MII Receive AC Timing Specifications

Table 28 provides the MII receive AC timing specifications.

Table 28. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns

Table 28. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
RX_CLK clock rise (20%–80%)	t_{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time (80%–20%)	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 12 provides the AC test load for TSEC.

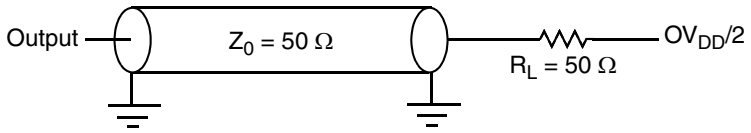


Figure 12. TSEC AC Test Load

Figure 13 shows the MII receive AC timing diagram.

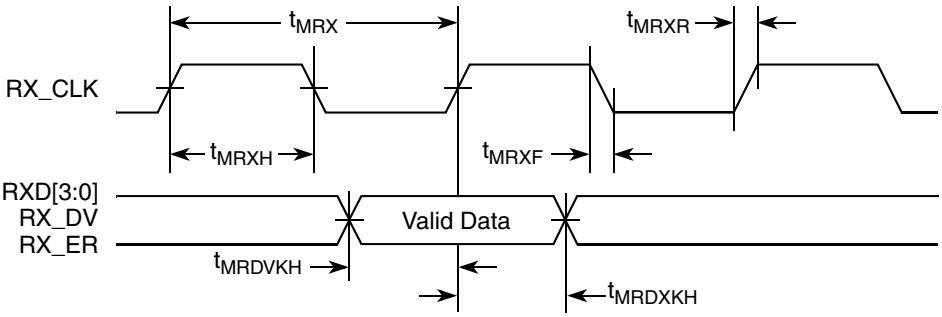


Figure 13. MII Receive AC Timing Diagram

8.2.3 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.3.1 TBI Transmit AC Timing Specifications

Table 29 provides the TBI transmit AC timing specifications.

Table 29. TBI Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
GTX_CLK clock period	t_{TTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{TTXH}/t_{TTX}	40	—	60	%
GTX_CLK to TBI data TXD[7:0], TX_ER, TX_EN delay	t_{TTKHDX}	1.0	—	5.0	ns
GTX_CLK clock rise (20%–80%)	t_{TTXR}	—	—	1.0	ns
GTX_CLK clock fall time (80%–20%)	t_{TTXF}	—	—	1.0	ns

Notes:

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 14 shows the TBI transmit AC timing diagram.

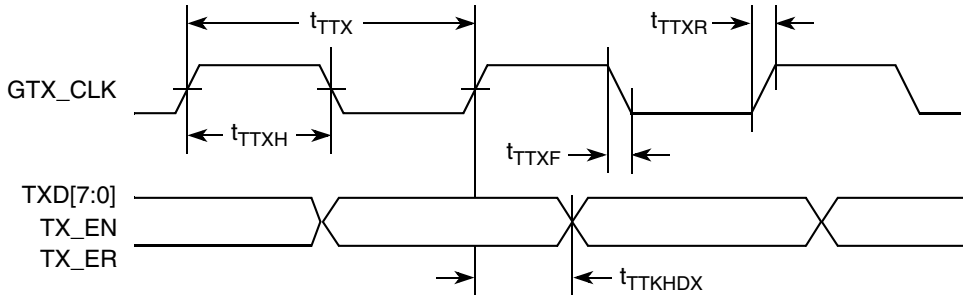


Figure 14. TBI Transmit AC Timing Diagram

8.2.3.2 TBI Receive AC Timing Specifications

Table 30 provides the TBI receive AC timing specifications.

Table 30. TBI Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
PMA_RX_CLK clock period	t_{TRX}		16.0		ns
PMA_RX_CLK skew	t_{SKTRX}	7.5	—	8.5	ns
RX_CLK duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%

8.2.4 RGMII and RTBI AC Timing Specifications

Table 31 presents the RGMII and RTBI AC timing specifications.

Table 31. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}	–0.5	—	0.5	ns
Data to clock input skew (at receiver)[2]	t_{SKRGT}	1.0	—	2.8	ns
Clock cycle duration[3]	t_{RGT}	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T[4, 5]	t_{RGTH}/t_{RGT}	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX[3, 5]	t_{RGTH}/t_{RGT}	40	50	60	%
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns
Fall time (80%–20%)	t_{RGTF}	—	—	0.75	ns

Notes:

1. In general, the clock reference symbol for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Also, the notation for rise (R) and fall (F) times follows the clock symbol. For symbols representing skews, the subscript is SK followed by the clock being skewed (RGT).
2. This implies that PC board design requires clocks to be routed so that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned.
5. Duty cycle reference is $LV_{DD}/2$.

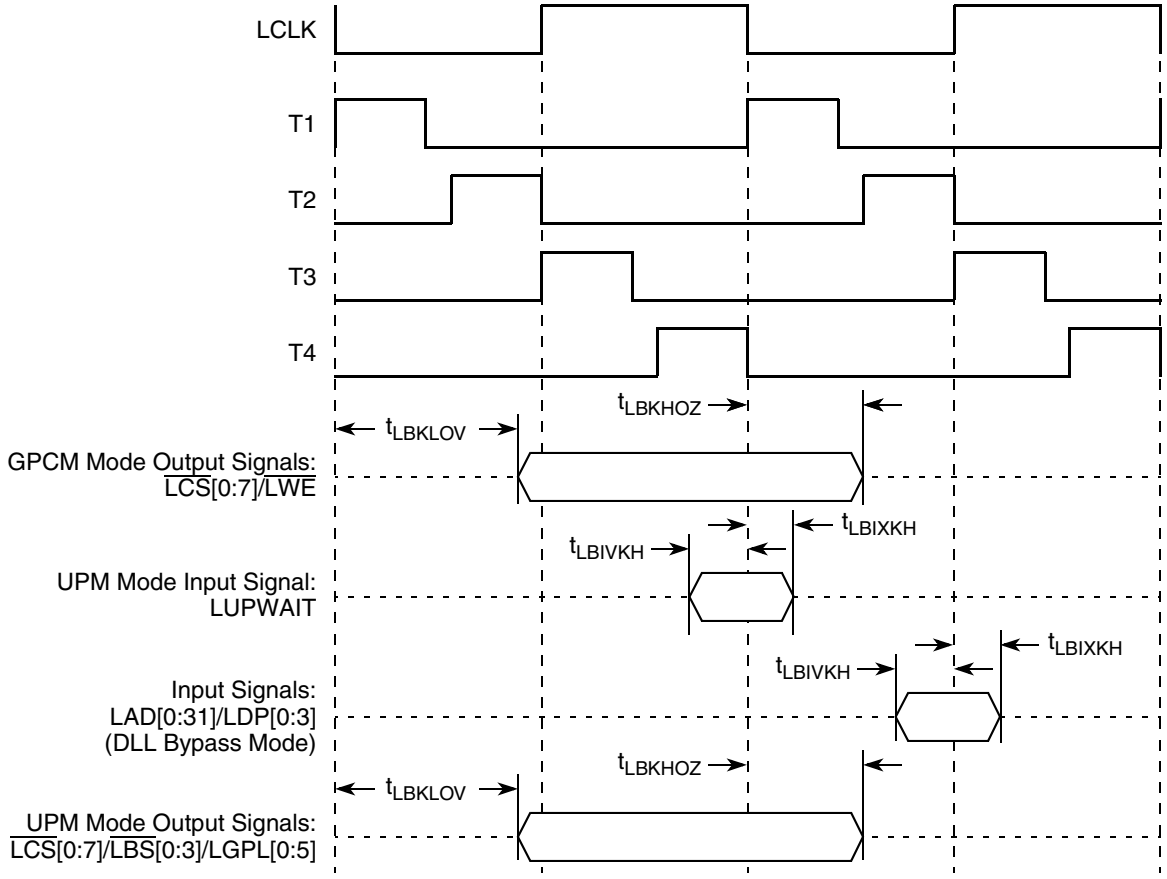


Figure 25. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (DLL Bypass Mode)

Figure 30 provides the boundary-scan timing diagram.

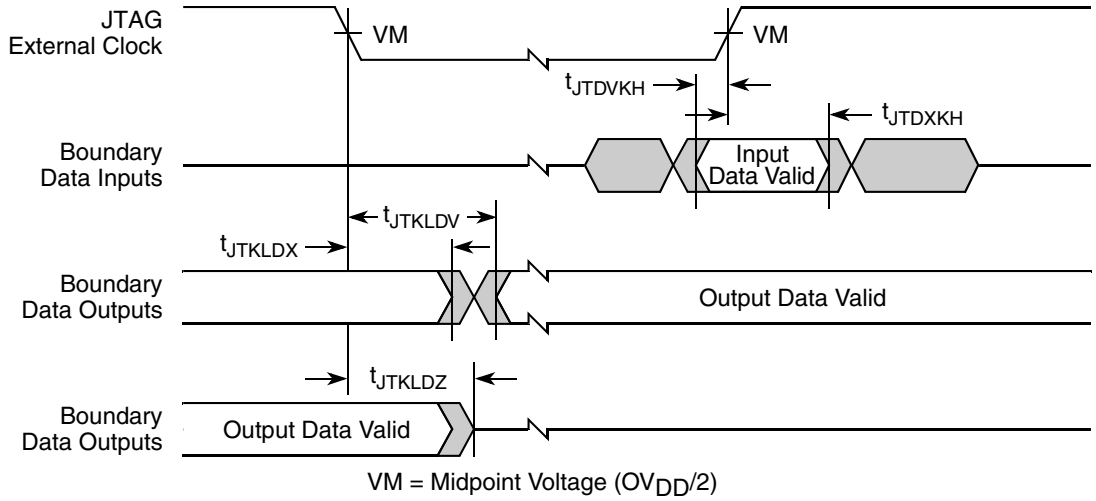


Figure 30. Boundary-Scan Timing Diagram

Figure 31 provides the test access port timing diagram.

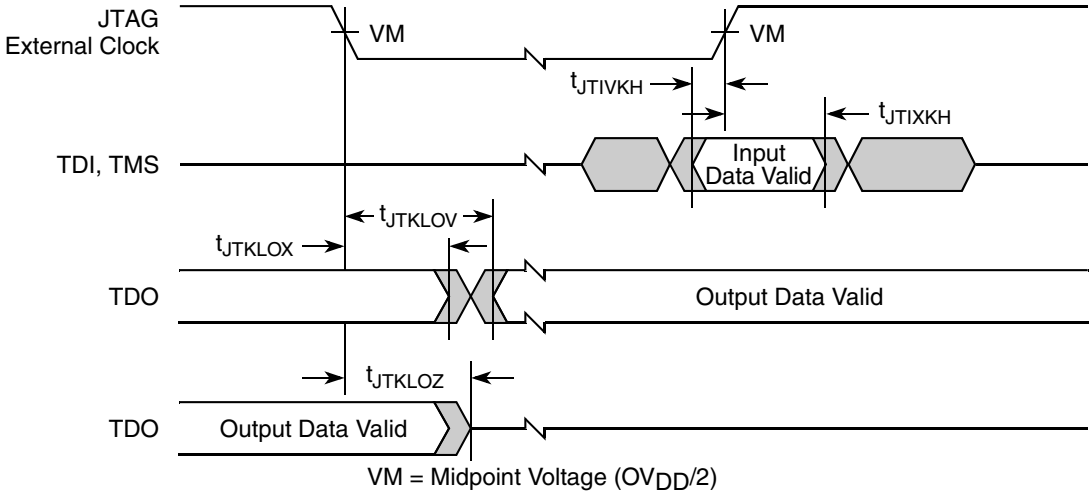
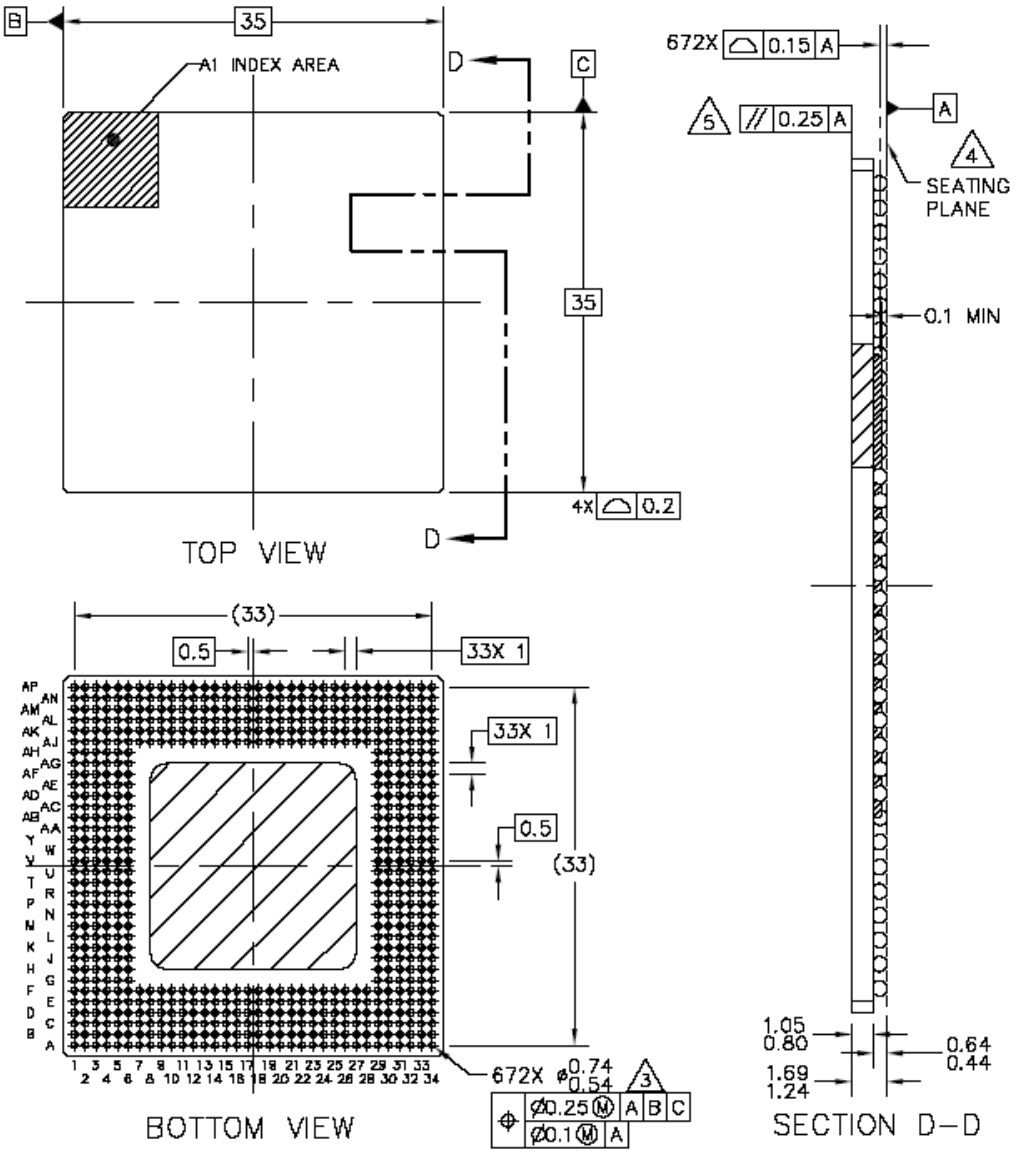


Figure 31. Test Access Port Timing Diagram

Pitch	1.00 mm
Module height (typical)	1.46 mm
Solder balls	62 Sn/36 Pb/2 Ag (ZU package) 96.5 Sn/3.5Ag (VV package)
Ball diameter (typical)	0.64 mm

18.2 Mechanical Dimensions for the MPC8347EA TBGA

Figure 40 shows the mechanical dimensions and bottom surface nomenclature for the MPC8347EA, 672-TBGA package.



Notes:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement must exclude any effect of mark on top surface of package.

Figure 40. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC8347EA TBGA

18.5 Pinout Listings

Table 55 provides the pinout listing for the MPC8347EA, 672 TBGA package.

Table 55. MPC8347EA (TBGA) Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI				
PCI_INTA/IRQ_OUT	B34	O	OV_{DD}	2
PCI_RESET_OUT	C33	O	OV_{DD}	—
PCI_AD[31:0]	G30, G32, G34, H31, H32, H33, H34, J29, J32, J33, L30, K31, K33, K34, L33, L34, P34, R29, R30, R33, R34, T31, T32, T33, U31, U34, V31, V32, V33, V34, W33, W34	I/O	OV_{DD}	—
PCI_C/BE[3:0]	J30, M31, P33, T34	I/O	OV_{DD}	—
PCI_PAR	P32	I/O	OV_{DD}	—
PCI_FRAME	M32	I/O	OV_{DD}	5
PCI_TRDY	N29	I/O	OV_{DD}	5
PCI_IRDY	M34	I/O	OV_{DD}	5
PCI_STOP	N31	I/O	OV_{DD}	5
PCI_DEVSEL	N30	I/O	OV_{DD}	5
PCI_IDSEL	J31	I	OV_{DD}	—
PCI_SERR	N34	I/O	OV_{DD}	5
PCI_PERR	N33	I/O	OV_{DD}	5
PCI_REQ[0]	D32	I/O	OV_{DD}	—
PCI_REQ[1]/CPCI1_HS_ES	D34	I	OV_{DD}	—
PCI_REQ[2:4]	E34, F32, G29	I	OV_{DD}	—
PCI_GNT0	C34	I/O	OV_{DD}	—
PCI_GNT1/CPCI1_HS_LED	D33	O	OV_{DD}	—
PCI_GNT2/CPCI1_HS_ENUM	E33	O	OV_{DD}	—
PCI_GNT[3:4]	F31, F33	O	OV_{DD}	—
M66EN	A19	I	OV_{DD}	—
DDR SDRAM Memory Interface				
MDQ[0:63]	D5, A3, C3, D3, C4, B3, C2, D4, D2, E5, G2, H6, E4, F3, G4, G3, H1, J2, L6, M6, H2, K6, L2, M4, N2, P4, R2, T4, P6, P3, R1, T2, AB5, AA3, AD6, AE4, AB4, AC2, AD3, AE6, AE3, AG4, AK5, AK4, AE2, AG6, AK3, AK2, AL2, AL1, AM5, AP5, AM2, AN1, AP4, AN5, AJ7, AN7, AM8, AJ9, AP6, AL7, AL9, AN8	I/O	GV_{DD}	—

Table 55. MPC8347EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LALE	AK24	O	OV_{DD}	—
LGPL0/LSDA10/cfg_reset_source0	AP27	I/O	OV_{DD}	—
LGPL1/$\overline{\text{LSDWE}}$/cfg_reset_source1	AL25	I/O	OV_{DD}	—
LGPL2/$\overline{\text{LSDRAS}}$/$\overline{\text{LOE}}$	AJ24	O	OV_{DD}	—
LGPL3/$\overline{\text{LSDCAS}}$/cfg_reset_source2	AN27	I/O	OV_{DD}	—
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE	AP28	I/O	OV_{DD}	13
LGPL5/cfg_clkin_div	AL26	I/O	OV_{DD}	—
LCKE	AM27	O	OV_{DD}	—
LCLK[0:2]	AN28, AK26, AP29	O	OV_{DD}	—
LSYNC_OUT	AM12	O	OV_{DD}	—
LSYNC_IN	AJ10	I	OV_{DD}	—
General Purpose I/O Timers				
GPIO1[0]/$\overline{\text{DMA\_DREQ0}}$/GTM1_TIN1/ GTM2_TIN2	F24	I/O	OV_{DD}	—
GPIO1[1]/$\overline{\text{DMA\_DACK0}}$/$\overline{\text{GTM1\_TGATE1}}$/ $\overline{\text{GTM2\_TGATE2}}$	E24	I/O	OV_{DD}	—
GPIO1[2]/$\overline{\text{DMA\_DDONE0}}$/$\overline{\text{GTM1\_TOUT1}}$	B25	I/O	OV_{DD}	—
GPIO1[3]/$\overline{\text{DMA\_DREQ1}}$/GTM1_TIN2/ GTM2_TIN1	D24	I/O	OV_{DD}	—
GPIO1[4]/$\overline{\text{DMA\_DACK1}}$/$\overline{\text{GTM1\_TGATE2}}$/ $\overline{\text{GTM2\_TGATE1}}$	A25	I/O	OV_{DD}	—
GPIO1[5]/$\overline{\text{DMA\_DDONE1}}$/$\overline{\text{GTM1\_TOUT2}}$/ $\overline{\text{GTM2\_TOUT1}}$	B24	I/O	OV_{DD}	—
GPIO1[6]/$\overline{\text{DMA\_DREQ2}}$/GTM1_TIN3/ GTM2_TIN4	A24	I/O	OV_{DD}	—
GPIO1[7]/$\overline{\text{DMA\_DACK2}}$/$\overline{\text{GTM1\_TGATE3}}$/ $\overline{\text{GTM2\_TGATE4}}$	D23	I/O	OV_{DD}	—
GPIO1[8]/$\overline{\text{DMA\_DDONE2}}$/$\overline{\text{GTM1\_TOUT3}}$	B23	I/O	OV_{DD}	—
GPIO1[9]/$\overline{\text{DMA\_DREQ3}}$/GTM1_TIN4/ GTM2_TIN3	A23	I/O	OV_{DD}	—
GPIO1[10]/$\overline{\text{DMA\_DACK3}}$/$\overline{\text{GTM1\_TGATE4}}$/ $\overline{\text{GTM2\_TGATE3}}$	F22	I/O	OV_{DD}	—
GPIO1[11]/$\overline{\text{DMA\_DDONE3}}$/$\overline{\text{GTM1\_TOUT4}}$/ $\overline{\text{GTM2\_TOUT3}}$	E22	I/O	OV_{DD}	—
USB Port 1				
MPH1_D0_ENABLEN/DR_D0_ENABLEN	A26	I/O	OV_{DD}	—
MPH1_D1_SER_TXD/DR_D1_SER_TXD	B26	I/O	OV_{DD}	—
MPH1_D2_VMO_SE0/DR_D2_VMO_SE0	D25	I/O	OV_{DD}	—

Table 55. MPC8347EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MPH1_D3_SPEED/DR_D3_SPEED	A27	I/O	OV_{DD}	—
MPH1_D4_DP/DR_D4_DP	B27	I/O	OV_{DD}	—
MPH1_D5_DM/DR_D5_DM	C27	I/O	OV_{DD}	—
MPH1_D6_SER_RCV/DR_D6_SER_RCV	D26	I/O	OV_{DD}	—
MPH1_D7_DRVVBUS/DR_D7_DRVVBUS	E26	I/O	OV_{DD}	—
MPH1_NXT/DR_SESS_VLD_NXT	D27	I	OV_{DD}	—
MPH1_DIR_DPPULLUP/ DR_XCVR_SEL_DPPULLUP	A28	I/O	OV_{DD}	—
MPH1_STP_SUSPEND/ DR_STP_SUSPEND	F26	O	OV_{DD}	—
MPH1_PWRFAULT/ DR_RX_ERROR_PWRFAULT	E27	I	OV_{DD}	—
MPH1_PCTL0/DR_TX_VALID_PCTL0	A29	O	OV_{DD}	—
MPH1_PCTL1/DR_TX_VALIDH_PCTL1	D28	O	OV_{DD}	—
MPH1_CLK/DR_CLK	B29	I	OV_{DD}	—
USB Port 0				
MPH0_D0_ENABLEN/DR_D8_CHGVBUS	C29	I/O	OV_{DD}	—
MPH0_D1_SER_TXD/DR_D9_DCHGVBUS	A30	I/O	OV_{DD}	—
MPH0_D2_VMO_SE0/DR_D10_DPPD	E28	I/O	OV_{DD}	—
MPH0_D3_SPEED/DR_D11_DMMD	B30	I/O	OV_{DD}	—
MPH0_D4_DP/DR_D12_VBUS_VLD	C30	I/O	OV_{DD}	—
MPH0_D5_DM/DR_D13_SESS_END	A31	I/O	OV_{DD}	—
MPH0_D6_SER_RCV/DR_D14	B31	I/O	OV_{DD}	—
MPH0_D7_DRVVBUS/DR_D15_IDPULLUP	C31	I/O	OV_{DD}	—
MPH0_NXT/DR_RX_ACTIVE_ID	B32	I	OV_{DD}	—
MPH0_DIR_DPPULLUP/DR_RESET	A32	I/O	OV_{DD}	—
MPH0_STP_SUSPEND/DR_TX_READY	A33	I/O	OV_{DD}	—
MPH0_PWRFAULT/DR_RX_VALIDH	C32	I	OV_{DD}	—
MPH0_PCTL0/DR_LINE_STATE0	D31	I/O	OV_{DD}	—
MPH0_PCTL1/DR_LINE_STATE1	E30	I/O	OV_{DD}	—
MPH0_CLK/DR_RX_VALID	B33	I	OV_{DD}	—
Programmable Interrupt Controller				
$\overline{\text{MCP\_OUT}}$	AN33	O	OV_{DD}	2
$\overline{\text{IRQ}}$0/$\overline{\text{MCP_IN}}$/GPIO2[12]	C19	I/O	OV_{DD}	—
$\overline{\text{IRQ}}$[1:5]/GPIO2[13:17]	C22, A22, D21, C21, B21	I/O	OV_{DD}	—

Table 56. MPC8347EA (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MRAS	AF7	O	GV_{DD}	—
$\overline{\text{MCAS}}$	AG6	O	GV_{DD}	—
$\overline{\text{MCS}}$[0:3]	AE7, AH7, AH4, AF2	O	GV_{DD}	—
MCKE[0:1]	AG23, AH23	O	GV_{DD}	3
MCK[0:5]	AH15, AE24, AE2, AF14, AE23, AD3	O	GV_{DD}	—
$\overline{\text{MCK}}$[0:5]	AG15, AD23, AE3, AG14, AF24, AD2	O	GV_{DD}	—
MODT[0:3]	AG5, AD4, AH6, AF4	O	GV_{DD}	—
MBA[2]	AD22	O	GV_{DD}	—
MDIC0	AG11	I/O	—	9
MDIC1	AF12	I/O	—	9
Local Bus Controller Interface				
LAD[0:31]	T4, T5, T1, R2, R3, T2, R1, R4, P1, P2, P3, P4, N1, N4, N2, N3, M1, M2, M3, N5, M4, L1, L2, L3, K1, M5, K2, K3, J1, J2, L5, J3	I/O	OV_{DD}	—
LDP[0]/$\overline{\text{CKSTOP\_OUT}}$	H1	I/O	OV_{DD}	—
LDP[1]/$\overline{\text{CKSTOP\_IN}}$	K5	I/O	OV_{DD}	—
LDP[2]/$\overline{\text{LCS}}$[4]	H2	I/O	OV_{DD}	—
LDP[3]/$\overline{\text{LCS}}$[5]	G1	I/O	OV_{DD}	—
LA[27:31]	J4, H3, G2, F1, G3	O	OV_{DD}	—
$\overline{\text{LCS}}$[0:3]	J5, H4, F2, E1	O	OV_{DD}	—
$\overline{\text{LWE}}$[0:3]/LSDDQM[0:3]/$\overline{\text{LBS}}$[0:3]	F3, G4, D1, E2	O	OV_{DD}	—
LBCTL	H5	O	OV_{DD}	—
LALE	E3	O	OV_{DD}	—
LGPL0/LSDA10/cfg_reset_source0	F4	I/O	OV_{DD}	—
LGPL1/$\overline{\text{LSDWE}}$/cfg_reset_source1	D2	I/O	OV_{DD}	—
LGPL2/$\overline{\text{LSDRAS}}$/$\overline{\text{LOE}}$	C1	O	OV_{DD}	—
LGPL3/$\overline{\text{LSDCAS}}$/cfg_reset_source2	C2	I/O	OV_{DD}	—
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE	C3	I/O	OV_{DD}	12
LGPL5/cfg_clkin_div	B3	I/O	OV_{DD}	—
LCKE	E4	O	OV_{DD}	—
LCLK[0:2]	D4, A3, C4	O	OV_{DD}	—
LSYNC_OUT	U3	O	OV_{DD}	—
LSYNC_IN	Y2	I	OV_{DD}	—

Table 56. MPC8347EA (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MPH1_PCTL0/DR_TX_VALID_PCTL0	A26	O	OV_{DD}	—
MPH1_PCTL1/DR_TX_VALIDH_PCTL1	B25	O	OV_{DD}	—
MPH1_CLK/DR_CLK	A25	I	OV_{DD}	—
USB Port 0				
MPH0_D0_ENABLEN/DR_D8_CHGVBUS	D24	I/O	OV_{DD}	—
MPH0_D1_SER_TXD/DR_D9_DCHGVBUS	C24	I/O	OV_{DD}	—
MPH0_D2_VMO_SE0/DR_D10_DPPD	B24	I/O	OV_{DD}	—
MPH0_D3_SPEED/DR_D11_DMMD	A24	I/O	OV_{DD}	—
MPH0_D4_DP/DR_D12_VBUS_VLD	D23	I/O	OV_{DD}	—
MPH0_D5_DM/DR_D13_SESS_END	C23	I/O	OV_{DD}	—
MPH0_D6_SER_RCV/DR_D14	B23	I/O	OV_{DD}	—
MPH0_D7_DRVVBUS/DR_D15_IDPULLUP	A23	I/O	OV_{DD}	—
MPH0_NXT/DR_RX_ACTIVE_ID	D22	I	OV_{DD}	—
MPH0_DIR_DPPULLUP/DR_RESET	C22	I/O	OV_{DD}	—
MPH0_STP_SUSPEND/DR_TX_READY	B22	I/O	OV_{DD}	—
MPH0_PWRFAULT/DR_RX_VALIDH	A22	I	OV_{DD}	—
MPH0_PCTL0/DR_LINE_STATE0	E21	I/O	OV_{DD}	—
MPH0_PCTL1/DR_LINE_STATE1	D21	I/O	OV_{DD}	—
MPH0_CLK/DR_RX_VALID	C21	I	OV_{DD}	—
Programmable Interrupt Controller				
$\overline{\text{MCP\_OUT}}$	E8	O	OV_{DD}	2
$\overline{\text{IRQ}}$0/$\overline{\text{MCP_IN}}$/GPIO2[12]	J28	I/O	OV_{DD}	—
$\overline{\text{IRQ}}$[1:5]/GPIO2[13:17]	K25, J25, H26, L24, G27	I/O	OV_{DD}	—
$\overline{\text{IRQ}}$[6]/GPIO2[18]/CKSTOP_OUT	G28	I/O	OV_{DD}	—
$\overline{\text{IRQ}}$[7]/GPIO2[19]/CKSTOP_IN	J26	I/O	OV_{DD}	—
Ethernet Management Interface				
EC_MDC	Y24	O	LV_{DD1}	—
EC_MDIO	Y25	I/O	LV_{DD1}	11
Gigabit Reference Clock				
EC_GTX_CLK125	Y26	I	LV_{DD1}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_COL/GPIO2[20]	M26	I/O	OV_{DD}	—
TSEC1_CRS/GPIO2[21]	U25	I/O	LV_{DD1}	—
TSEC1_GTX_CLK	V24	O	LV_{DD1}	3

Table 65. Package Thermal Characteristics for TBGA (continued)

Characteristic	Symbol	Value	Unit	Notes
Junction-to-package natural convection on top	Ψ_{JT}	1	°C/W	6

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal, 1 m/s is approximately equal to 200 linear feet per minute (LFM).
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 66 provides the package thermal characteristics for the 620 29 × 29 mm PBGA of the MPC8347EA.

Table 66. Package Thermal Characteristics for PBGA

Parameter	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection on single-layer board (1s)	$R_{\theta JA}$	21	°C/W	1, 2
Junction-to-ambient natural convection on four-layer board (2s2p)	$R_{\theta JMA}$	15	°C/W	1, 3
Junction-to-ambient (at 200 ft/min) on single-layer board (1s)	$R_{\theta JMA}$	17	°C/W	1, 3
Junction-to-ambient (at 200 ft/min) on four-layer board (2s2p)	$R_{\theta JMA}$	12	°C/W	1, 3
Junction-to-board thermal	$R_{\theta JB}$	6	°C/W	4
Junction-to-case thermal	$R_{\theta JC}$	5	°C/W	5
Junction-to-package natural convection on top	Ψ_{JT}	5	°C/W	6

Notes
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

20.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$ where $P_{I/O}$ is the power dissipation of the I/O drivers. See Table 5 for I/O power dissipation values.

20.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)
T_A = ambient temperature for the package (°C)
$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Generally, the value obtained on a single-layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

20.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)
T_A = ambient temperature for the package (°C)
$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

Table 72. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
8	2/2009	• Added footnote 6 to Table 7. • In Section 9.2, "USB AC Electrical Specifications," clarified that AC table is for ULPI only. • In Table 39, corrected t_{LBKHOV} parameter to t_{LBKLOV} (output data is driven on falling edge of clock in DLL bypass mode). Similarly, made the same correction to Figure 22, Figure 24, and Figure 25 for output signals. • Added footnote 10 and 11 to Table 55 and Table 56. • In Section 21.1, "System Clocking," removed "(AVDD1)" and "(AVDD2") from bulleted list. • In Section 21.2, "PLL Power Supply Filtering," in the second paragraph, changed "provide five independent filter circuits," and "the five AVDD pins" to provide four independent filter circuits," and "the four AVDD pins." • In Table 58, corrected the max csb_clk to 266 MHz. • In Table 64, added PLL configurations 903, 923, A03, A23, and 503 for 533 MHz • Added footnote 4 to Table 70. • In Table 70, updated note 1 to say the following: "For temperature range = C, processor frequency is limited to 533 (TBGA) and 400 (PBGA) with a platform frequency of 266."
7	4/2007	• In Table 3, "Output Drive Capability," changed the values in the Output Impedance column and added USB to the seventh row. • In Table 4, "Operating Frequencies for TBGA," added column for 400 MHz. • In Section 21.7, "Pull-Up Resistor Requirements,"deleted last two paragraphs and after first paragraph, added a new paragraph. • Deleted Section 21.8, "JTAG Configuration Signals," and Figure 43, "JTAG Interface Connection."
6	3/2007	• Page 1, updated first paragraph to reflect PowerQUICC II Pro information. • In Table 18, "DDR and DDR2 SDRAM Input AC Timing Specifications," added note 2 to t_{CISKEW} and deleted original note 3; renumbered the remaining notes. • In Figure 43, "JTAG Interface Connection," updated with new figure. • In Table 57, "Operating Frequencies for TBGA," in the 'Coherent system bus frequency (*csb_clk*)' row, changed the value in the 533 MHz column to 100-333. • In Table 63, "Suggested PLL Configurations," under the subhead, '33 MHz CLKIN/PCI_CLK Options,' added row A03 between Ref. No. 724 and 804. Under the subhead '66 MHz CLKIN/PCI_CLK Options,' added row 503 between Ref. No. 305 and 404. For Ref. No. 306, changed the CORE PLL value to 0000110. • In Section 23, "Ordering Information," replaced first paragraph and added a note. • In Section 23.1, "Part Numbers Fully Addressed by this Document," replaced first paragraph.
5	1/2007	• In Table 1, "Absolute Maximum Ratings," added (1.36 max for 667-MHz core frequency). • In Table 2, "Recommended Operating Conditions," added a row showing nominal core supply voltage of 1.3 V for 667-MHz parts. • In Table 4, "MPC8347EA Power Dissipation," added two footnotes to 667-MHz row showing nominal core supply voltage of 1.3 V for 667-MHz parts. • In Table 54, "MPC8347EA (TBGA) Pinout Listing," updated V_{DD} row to show nominal core supply voltage of 1.3 V for 667-MHz parts.
4	12/2006	Table 19, "DDR and DDR2 SDRAM Output AC Timing Specifications," modified T_{ddkhds} for 333 MHz from 900 ps to 775 ps.
3	11/2006	• Updated note in introduction. • In the features list in Section 1, "Overview," updated DDR data rate to show 266 MHz for PBGA parts for all silicon revisions, and 400 MHz for DDR2 for TBGA parts for silicon Rev. 2 and 3. • In Table 5, "MPC8347EA Typical I/O Power Dissipation," added GV_{DD} 1.8-V values for DDR2; added table footnote to designate rates that apply only to the TBGA package. • In Section 23, "Ordering Information," replicated note from document introduction.