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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	672-LBGA
Supplier Device Package	672-LBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8347ezuajfb

- Address translation units for address mapping between host and peripheral
- Dual address cycle for target
- Internal configuration registers accessible from PCI
- Security engine is optimized to handle all the algorithms associated with IPSec, SSL/TLS, SRTP, IEEE Std. 802.11i®, iSCSI, and IKE processing. The security engine contains four crypto-channels, a controller, and a set of crypto execution units (EUs):
 - Public key execution unit (PKEU) :
 - RSA and Diffie-Hellman algorithms
 - Programmable field size up to 2048 bits
 - Elliptic curve cryptography
 - F2m and F(p) modes
 - Programmable field size up to 511 bits
 - Data encryption standard (DES) execution unit (DEU)
 - DES and 3DES algorithms
 - Two key (K1, K2) or three key (K1, K2, K3) for 3DES
 - ECB and CBC modes for both DES and 3DES
 - Advanced encryption standard unit (AESU)
 - Implements the Rijndael symmetric-key cipher
 - Key lengths of 128, 192, and 256 bits
 - ECB, CBC, CCM, and counter (CTR) modes
 - XOR parity generation accelerator for RAID applications
 - ARC four execution unit (AFEU)
 - Stream cipher compatible with the RC4 algorithm
 - 40- to 128-bit programmable key
 - Message digest execution unit (MDEU)
 - SHA with 160-, 224-, or 256-bit message digest
 - MD5 with 128-bit message digest
 - HMAC with either algorithm
 - Random number generator (RNG)
 - Four crypto-channels, each supporting multi-command descriptor chains
 - Static and/or dynamic assignment of crypto-execution units through an integrated controller
 - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
- Universal serial bus (USB) dual role controller
 - USB on-the-go mode with both device and host functionality
 - Complies with USB specification Rev. 2.0
 - Can operate as a stand-alone USB device
 - One upstream facing port
 - Six programmable USB endpoints

4.3 TSEC Gigabit Reference Clock Timing

Table 8 provides the TSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications.

Table 8. EC_GTX_CLK125 AC Timing Specifications

At recommended operating conditions with $V_{DD} = 2.5 \pm 0.125$ mV/ 3.3 ± 0.165 mV

Parameter	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	t_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK125 rise and fall time $V_{DD} = 2.5$ V $V_{DD} = 3.3$ V	t_{G125R}/t_{G125F}	—	—	0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125L}	45 47	—	55 53	%	2
EC_GTX_CLK125 jitter	—	—	—	± 150	ps	2

Notes:

1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for $V_{DD} = 2.5$ V and from 0.6 and 2.7 V for $V_{DD} = 3.3$ V.
2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. The EC_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 8.2.4, "RGMII and RTBI AC Timing Specifications" for the duty cycle for 10Base-T and 100Base-T reference clock.

5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8347EA.

5.1 RESET DC Electrical Characteristics

Table 9 provides the DC electrical characteristics for the RESET pins of the MPC8347EA.

Table 9. RESET Pins DC Electrical Characteristics¹

Parameter	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	—	—	± 5	μA
Output high voltage ²	V_{OH}	$I_{OH} = -8.0$ mA	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0$ mA	—	0.5	V

Table 32. MII Management DC Electrical Characteristics Powered at 2.5 V (continued)

Parameter	Symbol	Conditions	Min	Max	Unit
Input high current	I_{IH}	$V_{IN}^1 = LV_{DD}$	—	10	μA
Input low current	I_{IL}	$V_{IN} = LV_{DD}$	–15	—	μA

Note:

1. The symbol V_{IN} , in this case, represents the LV_{IN} symbol referenced in [Table 1](#) and [Table 2](#).

Table 33. MII Management DC Electrical Characteristics Powered at 3.3 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	LV_{DD}	—		2.97	3.63	V
Output high voltage	V_{OH}	$I_{OH} = -1.0 \text{ mA}$	$LV_{DD} = \text{Min}$	2.10	$LV_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 1.0 \text{ mA}$	$LV_{DD} = \text{Min}$	GND	0.50	V
Input high voltage	V_{IH}	—		2.00	—	V
Input low voltage	V_{IL}	—		—	0.80	V
Input high current	I_{IH}	$LV_{DD} = \text{Max}$	$V_{IN}^1 = 2.1 \text{ V}$	—	40	μA
Input low current	I_{IL}	$LV_{DD} = \text{Max}$	$V_{IN} = 0.5 \text{ V}$	–600	—	μA

Note:

1. The symbol V_{IN} , in this case, represents the LV_{IN} symbol referenced in [Table 1](#) and [Table 2](#).

8.3.2 MII Management AC Electrical Specifications

[Table 34](#) provides the MII management AC timing specifications.

Table 34. MII Management AC Timing Specifications

At recommended operating conditions with LV_{DD} is 3.3 V $\pm$ 10% or 2.5 V $\pm$ 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	10	—	70	ns	3
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—

10.2 Local Bus AC Electrical Specification

Table 38 and Table 39 describe the general timing parameters of the local bus interface of the MPC8347EA.

Table 38. Local Bus General Timing Parameters—DLL On

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	—	ns	2
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	1.5	—	ns	3, 4
LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	2.2	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	1.0	—	ns	3, 4
LUPWAIT Input hold from local bus clock	$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
Local bus clock to LALE rise	t_{LBKHLR}	—	4.5	ns	—
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	4.5	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	4.5	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	4.5	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	1	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	1	—	ns	3
Local bus clock to output high impedance for LAD/LDP	t_{LBKHOZ}	—	3.8	ns	8

Notes:

1. The symbols for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to the rising edge of LSYNC_IN.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is not set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is set and when the load on the LALE output pin equals the load on the LAD output pins.
8. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

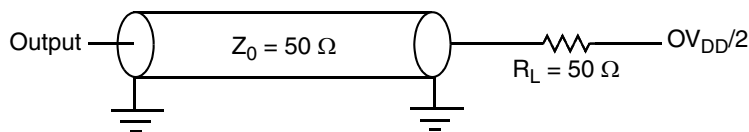
Table 39. Local Bus General Timing Parameters—DLL Bypass⁹

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	15	—	ns	2
Input setup to local bus clock	t_{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock	t_{LBIXKH}	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
Local bus clock to output valid	t_{LBKLOV}	—	3	ns	3
Local bus clock to output high impedance for LAD/LDP	t_{LBKHOZ}	—	4	ns	8

Notes:

1. The symbols for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to the falling edge of LCLK0 (for all outputs and for $\overline{LGTA}$ and LUPWAIT inputs) or the rising edge of LCLK0 (for all other inputs).
3. All signals are measured from $OV_{DD}/2$ of the rising/falling edge of LCLK0 to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is not set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is not set and when the load on the LALE output pin equals to the load on the LAD output pins.
8. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
9. DLL bypass mode is not recommended for use at frequencies above 66 MHz.

Figure 20 provides the AC test load for the local bus.


Figure 20. Local Bus C Test Load

12 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8347EA.

12.1 I²C DC Electrical Characteristics

Table 42 provides the DC electrical characteristics for the I²C interface of the MPC8347EA.

Table 42. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V _{IH}	0.7 × OV _{DD}	OV _{DD} + 0.3	V	—
Input low voltage level	V _{IL}	−0.3	0.3 × OV _{DD}	V	—
Low level output voltage	V _{OL}	0	0.2 × OV _{DD}	V	1
Output fall time from V _{IH} (min) to V _{IL} (max) with a bus capacitance from 10 to 400 pF	t _{I2CLKV}	20 + 0.1 × C _B	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t _{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between 0.1 × OV _{DD} and 0.9 × OV _{DD} (max))	I _I	−10	10	μA	4
Capacitance for each I/O pin	C _I	—	10	pF	—

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. Refer to the *MPC8349EA Integrated Host Processor Family Reference Manual*, for information on the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.

12.2 I²C AC Electrical Specifications

Table 43 provides the AC timing parameters for the I²C interface of the MPC8347EA. Note that all values refer to V_{IH}(min) and V_{IL}(max) levels (see Table 42).

Table 43. I²C AC Electrical Specifications

Parameter	Symbol ¹	Min	Max	Unit
SCL clock frequency	f _{I2C}	0	400	kHz
Low period of the SCL clock	t _{I2CL}	1.3	—	μs
High period of the SCL clock	t _{I2CH}	0.6	—	μs
Setup time for a repeated START condition	t _{I2SVKH}	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t _{I2SXKL}	0.6	—	μs
Data setup time	t _{I2DVKH}	100	—	ns
Data hold time:CBUS compatible masters I ² C bus devices	t _{I2DXKL}	— 0 ²	— 0.9 ³	μs

Table 43. I²C AC Electrical Specifications (continued)

Parameter	Symbol ¹	Min	Max	Unit
Fall time of both SDA and SCL signals ⁵	t_{I2CF}	—	300	ns
Setup time for STOP condition	t_{I2PVKH}	0.6	—	μ s
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μ s
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V

Notes:

1. The symbols for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) goes invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. The device provides a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH(min)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKH} must be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.
- 5.)The device does not follow the "I²C-BUS Specifications" version 2.1 regarding the t_{I2CF} AC parameter.

Figure 32 provides the AC test load for the I²C.

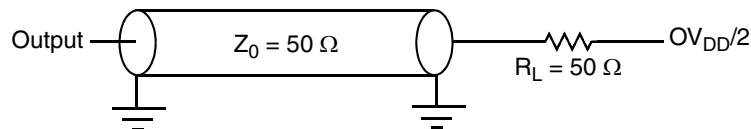
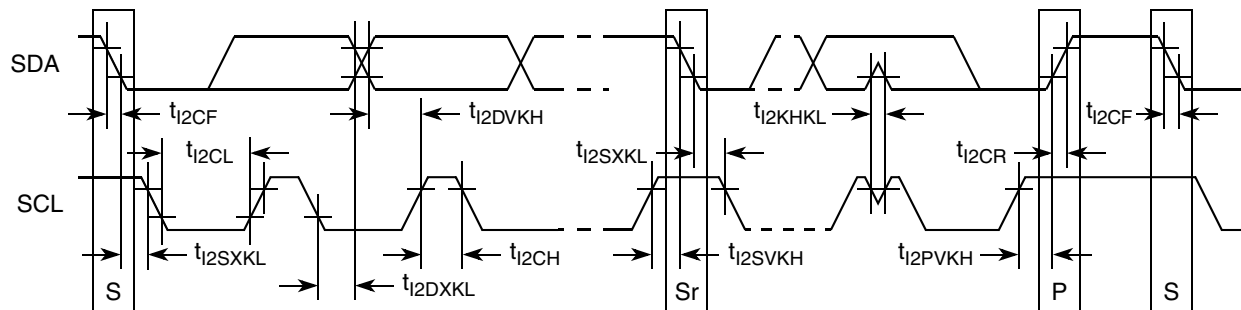

Figure 32. I²C AC Test Load

Figure 33 shows the AC timing diagram for the I²C bus.


Figure 33. I²C Bus AC Timing Diagram

14.2 Timer AC Timing Specifications

Table 48 provides the timer input and output AC timing specifications.

Table 48. Timers Input AC Timing Specifications¹

Parameter	Symbol ²	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:

1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

15 GPIO

This section describes the DC and AC electrical specifications for the GPIO.

15.1 GPIO DC Electrical Characteristics

Table 49 provides the DC electrical characteristics for the MPC8347EA GPIO.

Table 49. GPIO DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	−0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	$I_{OH} = -8.0$ mA	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0$ mA	—	0.5	V
Output low voltage	V_{OL}	$I_{OL} = 3.2$ mA	—	0.4	V

15.2 GPIO AC Timing Specifications

Table 50 provides the GPIO input and output AC timing specifications.

Table 50. GPIO Input AC Timing Specifications¹

Parameter	Symbol ²	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:

1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by external synchronous logic. GPIO inputs must be valid for at least t_{PIWID} ns to ensure proper operation.

Figure 38 and Figure 39 represent the AC timings from Table 54. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 38 shows the SPI timings in slave mode (external clock).

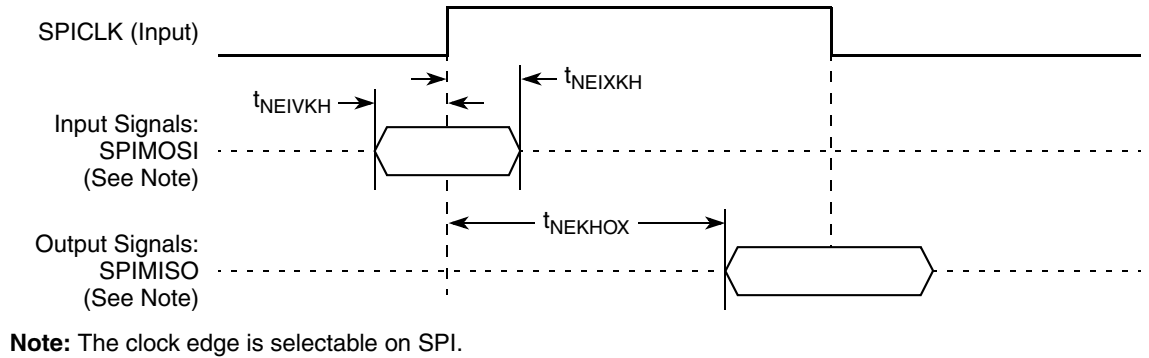


Figure 38. SPI AC Timing in Slave Mode (External Clock) Diagram

Figure 39 shows the SPI timings in master mode (internal clock).

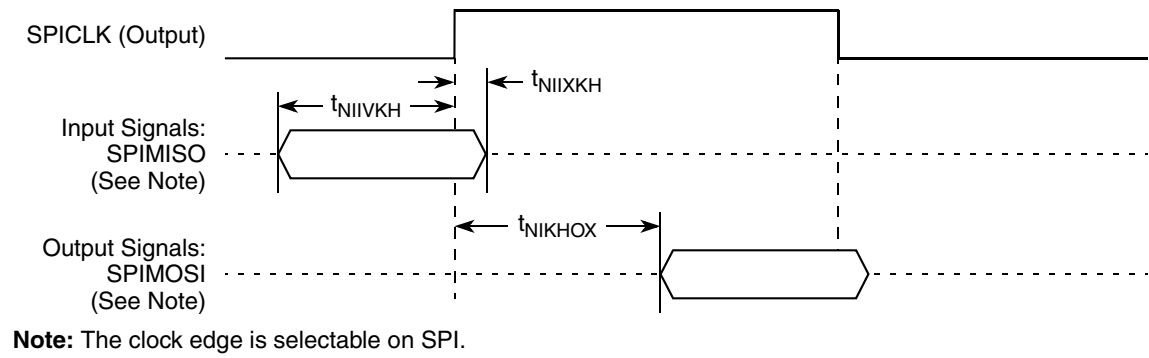


Figure 39. SPI AC Timing in Master Mode (Internal Clock) Diagram

18 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8347EA is available in two packages—a tape ball grid array (TBGA) and a plastic ball grid array (PBGA). See Section 18.1, “Package Parameters for the MPC8347EA TBGA,” Section 18.2, “Mechanical Dimensions for the MPC8347EA TBGA,” Section 18.3, “Package Parameters for the MPC8347EA PBGA,” and Section 18.4, “Mechanical Dimensions for the MPC8347EA PBGA.”

18.1 Package Parameters for the MPC8347EA TBGA

The package parameters are provided in the following list. The package type is 35 mm × 35 mm, 672 tape ball grid array (TBGA).

Package outline	35 mm × 35 mm
Interconnects	672

18.3 Package Parameters for the MPC8347EA PBGA

The package parameters are as provided in the following list. The package type is 29 mm × 29 mm, 620 plastic ball grid array (PBGA).

Package outline	29 mm × 29 mm
Interconnects	620
Pitch	1.00 mm
Module height (maximum)	2.46 mm
Module height (typical)	2.23 mm
Module height (minimum)	2.00 mm
Solder balls	62 Sn/36 Pb/2 Ag (ZQ package) 96.5 Sn/3.5Ag (VR package)
Ball diameter (typical)	0.60 mm

Table 55. MPC8347EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MECC[0:4]/MSRCID[0:4]	W4, W3, Y3, AA6, T1	I/O	GV _{DD}	—
MECC[5]/MDVAL	U1	I/O	GV _{DD}	—
MECC[6:7]	Y1, Y6	I/O	GV _{DD}	—
MDM[0:8]	B1, F1, K1, R4, AD4, AJ1, AP3, AP7, Y4	O	GV _{DD}	—
MDQS[0:8]	B2, F5, J1, P2, AC1, AJ2, AN4, AL8, W2	I/O	GV _{DD}	—
MBA[0:1]	AD1, AA5	O	GV _{DD}	—
MA[0:14]	W1, U4, T3, R3, P1, M1, N1, L3, L1, K2, Y2, K3, J3, AP2, AN6	O	GV _{DD}	—
$\overline{\text{MWE}}$	AF1	O	GV _{DD}	—
$\overline{\text{MRAS}}$	AF4	O	GV _{DD}	—
$\overline{\text{MCAS}}$	AG3	O	GV _{DD}	—
$\overline{\text{MCS}}[0:3]$	AG2, AG1, AK1, AL4	O	GV _{DD}	—
MCKE[0:1]	H3, G1	O	GV _{DD}	3
MCK[0:5]	U2, F4, AM3, V3, F2, AN3	O	GV _{DD}	—
$\overline{\text{MCK}}[0:5]$	U3, E3, AN2, V4, E1, AM4	O	GV _{DD}	—
MODT[0:3]	AH3, AJ5, AH1, AJ4	O	GV _{DD}	—
MBA[2]	H4	O	GV _{DD}	—
MDIC0	AB1	I/O	—	10
MDIC1	AA1	I/O	—	10
Local Bus Controller Interface				
LAD[0:31]	AM13, AP13, AL14, AM14, AN14, AP14, AK15, AJ15, AM15, AN15, AP15, AM16, AL16, AN16, AP16, AL17, AM17, AP17, AK17, AP18, AL18, AM18, AN18, AP19, AN19, AM19, AP20, AK19, AN20, AL20, AP21, AN21	I/O	OV _{DD}	—
LDP[0]/ $\overline{\text{CKSTOP_OUT}}$	AM21	I/O	OV _{DD}	—
LDP[1]/ $\overline{\text{CKSTOP_IN}}$	AP22	I/O	OV _{DD}	—
LDP[2]/ $\overline{\text{LCS}}[4]$	AN22	I/O	OV _{DD}	—
LDP[3]/ $\overline{\text{LCS}}[5]$	AM22	I/O	OV _{DD}	—
LA[27:31]	AK21, AP23, AN23, AP24, AK22	O	OV _{DD}	—
$\overline{\text{LCS}}[0:3]$	AN24, AL23, AP25, AN25	O	OV _{DD}	—
$\overline{\text{LWE}}[0:3]/\text{LSDDQM}[0:3]/\overline{\text{LBS}}[0:3]$	AK23, AP26, AL24, AM25	O	OV _{DD}	—
LBCTL	AN26	O	OV _{DD}	—

Table 55. MPC8347EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC2_TXD[3:0]/GPIO1[17:20]	B5, A5, F8, B6	I/O	LV _{DD2}	—
TSEC2_TX_ER/GPIO1[24]	F14	I/O	OV _{DD}	—
TSEC2_TX_EN/GPIO1[12]	C5	I/O	LV _{DD2}	3
TSEC2_TX_CLK/GPIO1[30]	E14	I/O	OV _{DD}	—
UART				
UART_SOUT[1:2]/MSRCID[0:1]/LSRCID[0:1]	AK27, AN29	O	OV _{DD}	—
UART_SIN[1:2]/MSRCID[2:3]/LSRCID[2:3]	AL28, AM29	I/O	OV _{DD}	—
UART_CTS[1]/MSRCID4/LSRCID4	AP30	I/O	OV _{DD}	—
UART_CTS[2]/MDVAL/ LDVAL	AN30	I/O	OV _{DD}	—
UART_RTS[1:2]	AP31, AM30	O	OV _{DD}	—
I²C interface				
IIC1_SDA	AK29	I/O	OV _{DD}	2
IIC1_SCL	AP32	I/O	OV _{DD}	2
IIC2_SDA	AN31	I/O	OV _{DD}	2
IIC2_SCL	AM31	I/O	OV _{DD}	2
SPI				
SPIMOSI/ $\overline{\text{LCS}}$ [6]	AN32	I/O	OV _{DD}	—
SPIMISO/ $\overline{\text{LCS}}$ [7]	AP33	I/O	OV _{DD}	—
SPICLK	AK30	I/O	OV _{DD}	—
SPISEL	AL31	I	OV _{DD}	—
Clocks				
PCI_CLK_OUT[0:2]	AN9, AP9, AM10	O	OV _{DD}	—
PCI_CLK_OUT[3]/ $\overline{\text{LCS}}$ [6]	AN10	O	OV _{DD}	—
PCI_CLK_OUT[4]/ $\overline{\text{LCS}}$ [7]	AJ11	O	OV _{DD}	—
PCI_SYNC_IN/PCI_CLOCK	AK12	I	OV _{DD}	—
PCI_SYNC_OUT	AP11	O	OV _{DD}	3
RTC/PIT_CLOCK	AM32	I	OV _{DD}	—
CLKIN	AM9	I	OV _{DD}	—
JTAG				
TCK	E20	I	OV _{DD}	—
TDI	F20	I	OV _{DD}	4
TDO	B20	O	OV _{DD}	3
TMS	A20	I	OV _{DD}	4
$\overline{\text{TRST}}$	B19	I	OV _{DD}	4

Table 56. MPC8347EA (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
General Purpose I/O Timers				
GPIO1[0]/DMA_DREQ0/GTM1_TIN1/ GTM2_TIN2	D27	I/O	OV _{DD}	—
GPIO1[1]/DMA_DACK0/GTM1_TGATE1/ GTM2_TGATE2	E26	I/O	OV _{DD}	—
GPIO1[2]/DMA_DDONE0/GTM1_TOUT1	D28	I/O	OV _{DD}	—
GPIO1[3]/DMA_DREQ1/GTM1_TIN2/ GTM2_TIN1	G25	I/O	OV _{DD}	—
GPIO1[4]/DMA_DACK1/GTM1_TGATE2/ GTM2_TGATE1	J24	I/O	OV _{DD}	—
GPIO1[5]/DMA_DDONE1/GTM1_TOUT2/ GTM2_TOUT1	F26	I/O	OV _{DD}	—
GPIO1[6]/DMA_DREQ2/GTM1_TIN3/ GTM2_TIN4	E27	I/O	OV _{DD}	—
GPIO1[7]/DMA_DACK2/GTM1_TGATE3/ GTM2_TGATE4	E28	I/O	OV _{DD}	—
GPIO1[8]/DMA_DDONE2/GTM1_TOUT3	H25	I/O	OV _{DD}	—
GPIO1[9]/DMA_DREQ3/GTM1_TIN4/ GTM2_TIN3	F27	I/O	OV _{DD}	—
GPIO1[10]/DMA_DACK3/ GTM1_TGATE4/GTM2_TGATE3	K24	I/O	OV _{DD}	—
GPIO1[11]/DMA_DDONE3/ GTM1_TOUT4/GTM2_TOUT3	G26	I/O	OV _{DD}	—
USB Port 1				
MPH1_D0_ENABLEN/DR_D0_ENABLEN	C28	I/O	OV _{DD}	—
MPH1_D1_SER_TXD/DR_D1_SER_TXD	F25	I/O	OV _{DD}	—
MPH1_D2_VMO_SE0/DR_D2_VMO_SE0	B28	I/O	OV _{DD}	—
MPH1_D3_SPEED/DR_D3_SPEED	C27	I/O	OV _{DD}	—
MPH1_D4_DP/DR_D4_DP	D26	I/O	OV _{DD}	—
MPH1_D5_DM/DR_D5_DM	E25	I/O	OV _{DD}	—
MPH1_D6_SER_RCV/DR_D6_SER_RCV	C26	I/O	OV _{DD}	—
MPH1_D7_DRVVBUS/DR_D7_DRVVBUS	D25	I/O	OV _{DD}	—
MPH1_NXT/DR_SESS_VLD_NXT	B26	I	OV _{DD}	—
MPH1_DIR_DPPULLUP/ DR_XCVR_SEL_DPPULLUP	E24	I/O	OV _{DD}	—
MPH1_STP_SUSPEND/ DR_STP_SUSPEND	A27	O	OV _{DD}	—
MPH1_PWRFAULT/ DR_RX_ERROR_PWRFAULT	C25	I	OV _{DD}	—

Table 56. MPC8347EA (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC1_RX_CLK	U26	I	LV _{DD1}	—
TSEC1_RX_DV	U24	I	LV _{DD1}	—
TSEC1_RX_ER/GPIO2[26]	L28	I/O	OV _{DD}	—
TSEC1_RXD[7:4]/GPIO2[22:25]	M27, M28, N26, N27	I/O	OV _{DD}	—
TSEC1_RXD[3:0]	W26, W24, Y28, Y27	I	LV _{DD1}	—
TSEC1_TX_CLK	N25	I	OV _{DD}	—
TSEC1_TXD[7:4]/GPIO2[27:30]	N28, P25, P26, P27	I/O	OV _{DD}	—
TSEC1_TXD[3:0]	V28, V27, V26, W28	O	LV _{DD1}	10
TSEC1_TX_EN	W27	O	LV _{DD1}	—
TSEC1_TX_ER/GPIO2[31]	N24	I/O	OV _{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_COL/GPIO1[21]	P28	I/O	OV _{DD}	—
TSEC2_CRS/GPIO1[22]	AC28	I/O	LV _{DD2}	—
TSEC2_GTX_CLK	AC27	O	LV _{DD2}	—
TSEC2_RX_CLK	AB25	I	LV _{DD2}	—
TSEC2_RX_DV/GPIO1[23]	AC26	I/O	LV _{DD2}	—
TSEC2_RXD[7:4]/GPIO1[26:29]	R28, T24, T25, T26	I/O	OV _{DD}	—
TSEC2_RXD[3:0]/GPIO1[13:16]	AA25, AA26, AA27, AA28	I/O	LV _{DD2}	—
TSEC2_RX_ER/GPIO1[25]	R25	I/O	OV _{DD}	—
TSEC2_TXD[7]/GPIO1[31]	T27	I/O	OV _{DD}	—
TSEC2_TXD[6]/DR_XCVR_TERM_SEL	T28	O	OV _{DD}	—
TSEC2_TXD[5]/DR_UTMI_OPMODE1	U28	O	OV _{DD}	—
TSEC2_TXD[4]/DR_UTMI_OPMODE0	U27	O	OV _{DD}	—
TSEC2_TXD[3:0]/GPIO1[17:20]	AB26, AB27, AA24, AB28	I/O	LV _{DD2}	—
TSEC2_TX_ER/GPIO1[24]	R27	I/O	OV _{DD}	—
TSEC2_TX_EN/GPIO1[12]	AD28	I/O	LV _{DD2}	3
TSEC2_TX_CLK/GPIO1[30]	R26	I/O	OV _{DD}	—
DUART				
UART_SOUT[1:2]/MSRCID[0:1]/LSRCID[0:1]	B4, A4	O	OV _{DD}	—
UART_SIN[1:2]/MSRCID[2:3]/LSRCID[2:3]	D5, C5	I/O	OV _{DD}	—
UART_CTS[1]/MSRCID4/LSRCID4	B5	I/O	OV _{DD}	—
UART_CTS[2]/MDVAL/LDVAL	A5	I/O	OV _{DD}	—
UART_RTS[1:2]	D6, C6	O	OV _{DD}	—

Table 56. MPC8347EA (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LV _{DD1}	U20, W25	Power for three-speed Ethernet #1 and for Ethernet management interface I/O (2.5 V, 3.3 V)	LV _{DD1}	—
LV _{DD2}	V20, Y23	Power for three-speed Ethernet #2 I/O (2.5 V, 3.3 V)	LV _{DD2}	—
V _{DD}	J11, J12, J15, K10, K11, K12, K13, K14, K15, K16, K17, K18, K19, L10, L11, L18, L19, M10, M19, N10, N19, P9, P10, P19, R10, R19, R20, T10, T19, U10, U19, V10, V11, V18, V19, W11, W12, W13, W14, W15, W16, W17, W18	Power for core (1.2 V)	V _{DD}	—
OV _{DD}	B27, D3, D11, D19, E15, E23, F5, F8, F11, F14, F17, F20, G24, H23, H24, J6, J14, J17, J18, K4, L9, L20, L23, L25, M6, M9, M20, P5, P20, P23, R6, R9, R24, U23, V4, V6	PCI, 10/100 Ethernet, and other standard (3.3 V)	OV _{DD}	—
MVREF1	AF19	I	DDR reference voltage	—
MVREF2	AE10	I	DDR reference voltage	—
No Connection				
NC	V1, V2, V5	—	—	—

Notes:

1. This pin is an open-drain signal. A weak pull-up resistor (1 k Ω) should be placed on this pin to OV_{DD}.
2. This pin is an open-drain signal. A weak pull-up resistor (2–10 k Ω) should be placed on this pin to OV_{DD}.
3. During reset, this output is actively driven rather than three-stated.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull-up if the chip is in PCI host mode. Follow the PCI specifications.
6. This pin must always be tied to GND.
7. This pin must always be left not connected.
8. Thermal sensitive resistor.
9. It is recommended that MDIC0 be tied to GRD using an 18 Ω resistor and MDIC1 be tied to DDR power using an 18 Ω resistor.
10. TSEC1_TXD[3] is required an external pull-up resistor. For proper functionality of the device, this pin must be pulled up or actively driven high during a hard reset. No external pull-down resistors are allowed to be attached to this net.
11. A weak pull-up resistor (2–10 k Ω) should be placed on this pin to LV_{DD1}.
12. For systems that boot from local bus (GPCM)-controlled NOR flash, a pullup on LGPL4 is required.

and Table 62 show the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

Table 61. CSB Frequency Options for Host Mode

CFG_CLKIN_DIV at Reset ¹	SPMF	<i>csb_clk</i> : Input Clock Ratio ²	Input Clock Frequency (MHz) ²			
			16.67	25	33.33	66.67
			<i>csb_clk</i> Frequency (MHz)			
Low	0010	2 : 1				133
Low	0011	3 : 1			100	200
Low	0100	4 : 1			133	266
Low	0101	5 : 1			166	333
Low	0110	6 : 1	100	150	200	
Low	0111	7 : 1	116	175	233	
Low	1000	8 : 1	133	200	266	
Low	1001	9 : 1	150	225	300	
Low	1010	10 : 1	166	250	333	
Low	1011	11 : 1	183	275		
Low	1100	12 : 1	200	300		
Low	1101	13 : 1	216	325		
Low	1110	14 : 1	233			
Low	1111	15 : 1	250			
Low	0000	16 : 1	266			
High	0010	2 : 1				133
High	0011	3 : 1			100	200
High	0100	4 : 1			133	266
High	0101	5 : 1			166	333
High	0110	6 : 1			200	
High	0111	7 : 1			233	
High	1000	8 : 1				

¹ CFG_CLKIN_DIV selects the ratio between CLKIN and PCI_SYNC_OUT.

² CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

DDR2 memory may be used at 133 MHz provided that the memory components are specified for operation at this frequency.

Table 65. Package Thermal Characteristics for TBGA (continued)

Characteristic	Symbol	Value	Unit	Notes
Junction-to-package natural convection on top	Ψ_{JT}	1	°C/W	6

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal, 1 m/s is approximately equal to 200 linear feet per minute (LFM).
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 66 provides the package thermal characteristics for the 620 29 × 29 mm PBGA of the MPC8347EA.

Table 66. Package Thermal Characteristics for PBGA

Parameter	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection on single-layer board (1s)	$R_{\theta JA}$	21	°C/W	1, 2
Junction-to-ambient natural convection on four-layer board (2s2p)	$R_{\theta JMA}$	15	°C/W	1, 3
Junction-to-ambient (at 200 ft/min) on single-layer board (1s)	$R_{\theta JMA}$	17	°C/W	1, 3
Junction-to-ambient (at 200 ft/min) on four-layer board (2s2p)	$R_{\theta JMA}$	12	°C/W	1, 3
Junction-to-board thermal	$R_{\theta JB}$	6	°C/W	4
Junction-to-case thermal	$R_{\theta JC}$	5	°C/W	5
Junction-to-package natural convection on top	Ψ_{JT}	5	°C/W	6

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

20.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$ where $P_{I/O}$ is the power dissipation of the I/O drivers. See [Table 5](#) for I/O power dissipation values.

Table 67 and Table 68 show heat sink thermal resistance for TBGA and PBGA of the MPC8347EA.

Table 67. Heat Sink and Thermal Resistance of MPC8347EA (TBGA)

Heat Sink Assuming Thermal Grease	Air Flow	35 × 35 mm TBGA
		Thermal Resistance
AAVID 30 × 30 × 9.4 mm pin fin	Natural convection	10
AAVID 30 × 30 × 9.4 mm pin fin	1 m/s	6.5
AAVID 30 × 30 × 9.4 mm pin fin	2 m/s	5.6
AAVID 31 × 35 × 23 mm pin fin	Natural convection	8.4
AAVID 31 × 35 × 23 mm pin fin	1 m/s	4.7
AAVID 31 × 35 × 23 mm pin fin	2 m/s	4
Wakefield, 53 × 53 × 25 mm pin fin	Natural convection	5.7
Wakefield, 53 × 53 × 25 mm pin fin	1 m/s	3.5
Wakefield, 53 × 53 × 25 mm pin fin	2 m/s	2.7
MEI, 75 × 85 × 12 no adjacent board, extrusion	Natural convection	6.7
MEI, 75 × 85 × 12 no adjacent board, extrusion	1 m/s	4.1
MEI, 75 × 85 × 12 no adjacent board, extrusion	2 m/s	2.8
MEI, 75 × 85 × 12 mm, adjacent board, 40 mm side bypass	1 m/s	3.1

Table 68. Heat Sink and Thermal Resistance of MPC8347EA (PBGA)

Heat Sink Assuming Thermal Grease	Air Flow	29 × 29 mm PBGA
		Thermal Resistance
AAVID 30 × 30 × 9.4 mm pin fin	Natural convection	13.5
AAVID 30 × 30 × 9.4 mm pin fin	1 m/s	9.6
AAVID 30 × 30 × 9.4 mm pin fin	2 m/s	8.8
AAVID 31 × 35 × 23 mm pin fin	Natural convection	11.3
AAVID 31 × 35 × 23 mm pin fin	1 m/s	8.1
AAVID 31 × 35 × 23 mm pin fin	2 m/s	7.5
Wakefield, 53 × 53 × 25 mm pin fin	Natural convection	9.1
Wakefield, 53 × 53 × 25 mm pin fin	1 m/s	7.1
Wakefield, 53 × 53 × 25 mm pin fin	2 m/s	6.5
MEI, 75 × 85 × 12 no adjacent board, extrusion	Natural convection	10.1
MEI, 75 × 85 × 12 no adjacent board, extrusion	1 m/s	7.7
MEI, 75 × 85 × 12 no adjacent board, extrusion	2 m/s	6.6
MEI, 75 × 85 × 12 mm, adjacent board, 40 mm side bypass	1 m/s	6.9

21 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8347EA.

21.1 System Clocking

The MPC8347EA includes two PLLs:

1. The platform PLL generates the platform clock from the externally supplied CLKIN input. The frequency ratio between the platform and CLKIN is selected using the platform PLL ratio configuration bits as described in [Section 19.1, “System PLL Configuration.”](#)
2. The e300 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in [Section 19.2, “Core PLL Configuration.”](#)

21.2 PLL Power Supply Filtering

Each PLL gets power through independent power supply pins (AV_{DD1} , AV_{DD2} , respectively). The AV_{DD} level should always equal to V_{DD} , and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme.

There are a number of ways to provide power reliably to the PLLs, but the recommended solution is to provide four independent filter circuits as illustrated in [Figure 43](#), one to each of the four AV_{DD} pins. Independent filters to each PLL reduce the opportunity to cause noise injection from one PLL to the other.

The circuit filters noise in the PLL resonant frequency range from 500 kHz to 10 MHz. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

To minimize noise coupled from nearby circuits, each circuit should be placed as closely as possible to the specific AV_{DD} pin being supplied. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

[Figure 43](#) shows the PLL power supply filter circuit.

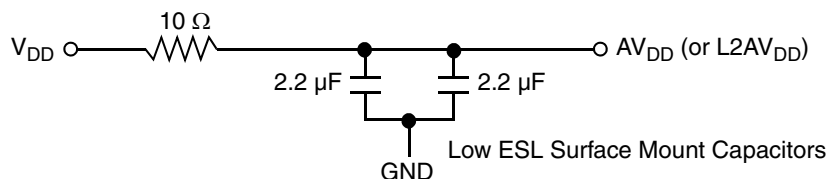


Figure 43. PLL Power Supply Filter Circuit

21.3 Decoupling Recommendations

Due to large address and data buses and high operating frequencies, the MPC8347EA can generate transient power surges and high frequency noise in its power supply, especially while driving large

Table 72. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
8	2/2009	- Added footnote 6 to Table 7. - In Section 9.2, "USB AC Electrical Specifications," clarified that AC table is for ULPI only. - In Table 39, corrected t_{LBKHOV} parameter to t_{LBKLOV} (output data is driven on falling edge of clock in DLL bypass mode). Similarly, made the same correction to Figure 22, Figure 24, and Figure 25 for output signals. - Added footnote 10 and 11 to Table 55 and Table 56. - In Section 21.1, "System Clocking," removed "(AVDD1)" and "(AVDD2)" from bulleted list. - In Section 21.2, "PLL Power Supply Filtering," in the second paragraph, changed "provide five independent filter circuits," and "the five AVDD pins" to provide four independent filter circuits," and "the four AVDD pins." - In Table 58, corrected the max csb_clk to 266 MHz. - In Table 64, added PLL configurations 903, 923, A03, A23, and 503 for 533 MHz - Added footnote 4 to Table 70. - In Table 70, updated note 1 to say the following: "For temperature range = C, processor frequency is limited to 533 (TBGA) and 400 (PBGA) with a platform frequency of 266."
7	4/2007	- In Table 3, "Output Drive Capability," changed the values in the Output Impedance column and added USB to the seventh row. - In Table 4, "Operating Frequencies for TBGA," added column for 400 MHz. - In Section 21.7, "Pull-Up Resistor Requirements," deleted last two paragraphs and after first paragraph, added a new paragraph. - Deleted Section 21.8, "JTAG Configuration Signals," and Figure 43, "JTAG Interface Connection."
6	3/2007	- Page 1, updated first paragraph to reflect PowerQUICC II Pro information. - In Table 18, "DDR and DDR2 SDRAM Input AC Timing Specifications," added note 2 to t_{CISKEW} and deleted original note 3; renumbered the remaining notes. - In Figure 43, "JTAG Interface Connection," updated with new figure. - In Table 57, "Operating Frequencies for TBGA," in the 'Coherent system bus frequency (<i>csb_clk</i>)' row, changed the value in the 533 MHz column to 100-333. - In Table 63, "Suggested PLL Configurations," under the subhead, '33 MHz CLKIN/PCI_CLK Options,' added row A03 between Ref. No. 724 and 804. Under the subhead '66 MHz CLKIN/PCI_CLK Options,' added row 503 between Ref. No. 305 and 404. For Ref. No. 306, changed the CORE PLL value to 0000110. - In Section 23, "Ordering Information," replaced first paragraph and added a note. - In Section 23.1, "Part Numbers Fully Addressed by this Document," replaced first paragraph.
5	1/2007	- In Table 1, "Absolute Maximum Ratings," added (1.36 max for 667-MHz core frequency). - In Table 2, "Recommended Operating Conditions," added a row showing nominal core supply voltage of 1.3 V for 667-MHz parts. - In Table 4, "MPC8347EA Power Dissipation," added two footnotes to 667-MHz row showing nominal core supply voltage of 1.3 V for 667-MHz parts. - In Table 54, "MPC8347EA (TBGA) Pinout Listing," updated V_{DD} row to show nominal core supply voltage of 1.3 V for 667-MHz parts.
4	12/2006	Table 19, "DDR and DDR2 SDRAM Output AC Timing Specifications," modified T_{ddkhd} for 333 MHz from 900 ps to 775 ps.
3	11/2006	- Updated note in introduction. - In the features list in Section 1, "Overview," updated DDR data rate to show 266 MHz for PBGA parts for all silicon revisions, and 400 MHz for DDR2 for TBGA parts for silicon Rev. 2 and 3. - In Table 5, "MPC8347EA Typical I/O Power Dissipation," added GV_{DD} 1.8-V values for DDR2; added table footnote to designate rates that apply only to the TBGA package. - In Section 23, "Ordering Information," replicated note from document introduction.