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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	672-LBGA
Supplier Device Package	672-LBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8347ezualfb

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



NOTE

The information in this document is accurate for revision 3.x silicon and later (in other words, for orderable part numbers ending in A or B). For information on revision 1.1 silicon and earlier versions, see the *MPC8347E PowerQUICC II Pro Integrated Host Processor Hardware Specifications*.

See Section 22.1, "Part Numbers Fully Addressed by This Document," for silicon revision level determination.

1 Overview

This section provides a high-level overview of the device features. Figure 1 shows the major functional units within the MPC8347EA.



Figure 1. MPC8347EA Block Diagram

Major features of the device are as follows:

- Embedded PowerPC e300 processor core; operates at up to 667 MHz
 - High-performance, superscalar processor core
 - Floating-point, integer, load/store, system register, and branch processing units
 - 32-Kbyte instruction cache, 32-Kbyte data cache
 - Lockable portion of L1 cache
 - Dynamic power management
 - Software-compatible with the other Freescale processor families that implement Power Architecture technology
- Double data rate, DDR1/DDR2 SDRAM memory controller
 - Programmable timing supporting DDR1 and DDR2 SDRAM
 - 32- or 64-bit data interface, up to 400 MHz data rate for TBGA, 266 MHz for PBGA



Overview

- Up to four physical banks (chip selects), each bank up to 1 Gbyte independently addressable
- DRAM chip configurations from 64 Mbits to 1 Gbit with $\times 8/\times 16$ data ports
- Full error checking and correction (ECC) support
- Support for up to 16 simultaneous open pages (up to 32 pages for DDR2)
- Contiguous or discontiguous memory mapping
- Read-modify-write support
- Sleep-mode support for SDRAM self refresh
- Auto refresh
- On-the-fly power management using CKE
- Registered DIMM support
- 2.5-V SSTL2 compatible I/O for DDR1, 1.8-V SSTL2 compatible I/O for DDR2
- Dual three-speed (10/100/1000) Ethernet controllers (TSECs)
 - Dual controllers designed to comply with IEEE 802.3TM, 802.3uTM, 820.3xTM, 802.3zTM, 802.3acTM standards
 - Ethernet physical interfaces:
 - 1000 Mbps IEEE Std. 802.3 GMII/RGMII, IEEE Std. 802.3z TBI/RTBI, full-duplex
 - 10/100 Mbps IEEE Std. 802.3 MII full- and half-duplex
 - Buffer descriptors are backward-compatible with MPC8260 and MPC860T 10/100 programming models
 - 9.6-Kbyte jumbo frame support
 - RMON statistics support
 - Internal 2-Kbyte transmit and 2-Kbyte receive FIFOs per TSEC module
 - MII management interface for control and status
 - Programmable CRC generation and checking
- PCI interface
 - Designed to comply with PCI Specification Revision 2.3
 - Data bus width:
 - 32-bit data PCI interface operating at up to 66 MHz
 - PCI 3.3-V compatible
 - PCI host bridge capabilities
 - PCI agent mode on PCI interface
 - PCI-to-memory and memory-to-PCI streaming
 - Memory prefetching of PCI read accesses and support for delayed read transactions
 - Posting of processor-to-PCI and PCI-to-memory writes
 - On-chip arbitration supporting five masters on PCI
 - Accesses to all PCI address spaces
 - Parity supported
 - Selectable hardware-enforced coherency



Overview

- Address translation units for address mapping between host and peripheral
- Dual address cycle for target
- Internal configuration registers accessible from PCI
- Security engine is optimized to handle all the algorithms associated with IPSec, SSL/TLS, SRTP, IEEE Std. 802.11i[®], iSCSI, and IKE processing. The security engine contains four crypto-channels, a controller, and a set of crypto execution units (EUs):
 - Public key execution unit (PKEU) :
 - RSA and Diffie-Hellman algorithms
 - Programmable field size up to 2048 bits
 - Elliptic curve cryptography
 - F2m and F(p) modes
 - Programmable field size up to 511 bits
 - Data encryption standard (DES) execution unit (DEU)
 - DES and 3DES algorithms
 - Two key (K1, K2) or three key (K1, K2, K3) for 3DES
 - ECB and CBC modes for both DES and 3DES
 - Advanced encryption standard unit (AESU)
 - Implements the Rijndael symmetric-key cipher
 - Key lengths of 128, 192, and 256 bits
 - ECB, CBC, CCM, and counter (CTR) modes
 - XOR parity generation accelerator for RAID applications
 - ARC four execution unit (AFEU)
 - Stream cipher compatible with the RC4 algorithm
 - 40- to 128-bit programmable key
 - Message digest execution unit (MDEU)
 - SHA with 160-, 224-, or 256-bit message digest
 - MD5 with 128-bit message digest
 - HMAC with either algorithm
 - Random number generator (RNG)
 - Four crypto-channels, each supporting multi-command descriptor chains
 - Static and/or dynamic assignment of crypto-execution units through an integrated controller
 - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
- Universal serial bus (USB) dual role controller
 - USB on-the-go mode with both device and host functionality
 - Complies with USB specification Rev. 2.0
 - Can operate as a stand-alone USB device
 - One upstream facing port
 - Six programmable USB endpoints

Power Characteristics

	Core Frequency (MHz)	CSB Frequency (MHz)	Typical at T _J = 65	Typical ^{2,3}	Maximum ⁴	Unit
TBGA	333	333	2.0	3.0	3.2	W
		166	1.8	2.8	2.9	W
	400	266	2.1	3.0	3.3	W
		133	1.9	2.9	3.1	W
	450	300	2.3	3.2	3.5	W
		150	2.1	3.0	3.2	W
	500	333	2.4	3.3	3.6	W
		166	2.2	3.1	3.4	W
	533	266	2.4	3.3	3.6	W
		133	2.2	3.1	3.4	W
	667 ^{5,6}	333	3.5	4.6	5	W

 Table 4. MPC8347EA Power Dissipation¹ (continued)

¹ The values do not include I/O supply power (OV_{DD}, LV_{DD}, GV_{DD}) or AV_{DD}. For I/O power values, see Table 5.

² Typical power is based on a voltage of $V_{DD} = 1.2$ V, a junction temperature of $T_J = 105$ °C, and a Dhrystone benchmark application.

³ Thermal solutions may need to design to a value higher than typical power based on the end application, T_A target, and I/O power.

⁴ Maximum power is based on a voltage of V_{DD} = 1.2 V, worst case process, a junction temperature of T_J = 105°C, and an artificial smoke test.

⁵ Typical power is based on a voltage of V_{DD} = 1.3 V, a junction temperature of T_J = 105°C, and a Dhrystone benchmark application.

⁶ Maximum power is based on a voltage of V_{DD} = 1.3 V, worst case process, a junction temperature of T_J = 105°C, and an artificial smoke test.



4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the device.

4.1 DC Electrical Characteristics

Table 6 provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the MPC8347EA.

Parameter	Condition	Symbol	Min	Мах	Unit
Input high voltage	_	V _{IH}	2.7	OV _{DD} + 0.3	V
Input low voltage	_	V _{IL}	-0.3	0.4	V
CLKIN input current	$0~V \leq V_{IN} \leq OV_{DD}$	I _{IN}	—	±10	μA
PCI_SYNC_IN input current	$\begin{array}{c} 0 \ V \leq V_{IN} \leq 0.5 \ V \ or \\ OV_{DD} - 0.5 \ V \leq V_{IN} \leq OV_{DD} \end{array}$	I _{IN}	_	±10	μA
PCI_SYNC_IN input current	$0.5~V \leq \! V_{IN} \leq OV_{DD} - 0.5~V$	I _{IN}	—	±50	μA

Table 6. CLKIN DC Timing Specifications

4.2 AC Electrical Characteristics

The primary clock source for the MPC8347EA can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Table 7 provides the clock input (CLKIN/PCI_CLK) AC timing specifications for the device.

Table 7. CLKIN AC	Timing	Specifications
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Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
CLKIN/PCI_CLK frequency	f _{CLKIN}	_	_	66	MHz	1, 6
CLKIN/PCI_CLK cycle time	t _{CLKIN}	15	_	_	ns	—
CLKIN/PCI_CLK rise and fall time	t _{KH} , t _{KL}	0.6	1.0	2.3	ns	2
CLKIN/PCI_CLK duty cycle	t _{KHK} /t _{CLKIN}	40	_	60	%	3
CLKIN/PCI_CLK jitter	_	_	—	±150	ps	4, 5

Notes:

1. Caution: The system, core, USB, security, and TSEC must not exceed their respective maximum or minimum operating frequencies.

- 2. Rise and fall times for CLKIN/PCI_CLK are measured at 0.4 and 2.7 V.
- 3. Timing is guaranteed by design and characterization.
- 4. This represents the total input jitter—short term and long term—and is guaranteed by design.
- 5. The CLKIN/PCI_CLK driver's closed loop jitter bandwidth should be < 500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.
- 6. Spread spectrum clocking is allowed with 1% input frequency down-spread at maximum 50 KHz modulation rate regardless of input frequency.



RESET Initialization

4.3 TSEC Gigabit Reference Clock Timing

Table 8 provides the TSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications.

Table 8. EC_GTX_CLK125 AC Timing Specifications

At recommended operating conditions with LV $_{DD}$ = 2.5 \pm 0.125 mV/ 3.3 V \pm 165 mV

Parameter	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	t _{G125}	—	125	_	MHz	_
EC_GTX_CLK125 cycle time	t _{G125}	—	8		ns	
EC_GTX_CLK125 rise and fall time $LV_{DD} = 2.5 V$ $LV_{DD} = 3.3 V$	t _{G125R} /t _{G125F}			0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t _{G125H} /t _{G125}	45 47	_	55 53	%	2
EC_GTX_CLK125 jitter	_	—	—	±150	ps	2

Notes:

1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for LV_{DD} = 2.5 V and from 0.6 and 2.7 V for LV_{DD} = 3.3 V.

2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. The EC_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 8.2.4, "RGMII and RTBI AC Timing Specifications for the duty cycle for 10Base-T and 100Base-T reference clock.

5 **RESET Initialization**

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8347EA.

5.1 **RESET DC Electrical Characteristics**

Table 9 provides the DC electrical characteristics for the RESET pins of the MPC8347EA.

Parameter	Symbol	Condition	Min	Мах	Unit
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	—	_	±5	μA
Output high voltage ²	V _{OH}	I _{OH} = -8.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0 mA	—	0.5	V

Table 9. RESET Pins DC Electrical Characteristics¹



Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol ¹	Min	Max	Unit	Notes
266 MHz		1100	_		
200 MHz		1200	—		
MDQS preamble start	t _{DDKHMP}	$-0.5\times t_{MCK}-0.6$	$-0.5\times t_{MCK}+0.6$	ns	6
MDQS epilogue end	t _{DDKHME}	-0.6	0.6	ns	6

Notes:

- The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output goes invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are set up (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
 </sub>
- 2. All MCK/ \overline{MCK} referenced measurements are made from the crossing of the two signals ±0.1 V.
- 3. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK, MCS, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.
- 4. t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register and is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters are set to the same adjustment value. See the MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual for the timing modifications enabled by use of these bits.
- 5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside the data eye at the pins of the microprocessor.
- 6. All outputs are referenced to the rising edge of MCK(n) at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

Figure 6 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).



Figure 6. Timing Diagram for t_{DDKHMH}



Figure 7 shows the DDR SDRAM output timing diagram.



Figure 8 provides the AC test load for the DDR bus.



Figure 8. DDR AC Test Load

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8347EA.

7.1 DUART DC Electrical Characteristics

Table 21 provides the DC electrical characteristics for the DUART interface of the MPC8347EA.

Table 21. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Мах	Unit
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
Input current (0.8 V \leq V _{IN} \leq 2 V)	I _{IN}	_	±5	μA



Parameter	Symbol	Min	Мах	Unit
High-level output voltage, $I_{OH} = -100 \ \mu A$	V _{OH}	OV _{DD} - 0.2	_	V
Low-level output voltage, $I_{OL} = 100 \ \mu A$	V _{OL}	—	0.2	V

Table 21. DUART DC Electrical Characteristics (continued)

7.2 DUART AC Electrical Specifications

Table 22 provides the AC timing parameters for the DUART interface of the MPC8347EA.

Table 22. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16		2

Notes:

1. Actual attainable baud rate will be limited by the latency of interrupt processing.

2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

8 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speeds (10/100/1000 Mbps) and MII management.

8.1 Three-Speed Ethernet Controller (TSEC)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to gigabit media independent interface (GMII), the media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), and reduced ten-bit interface (RTBI) signals except management data input/output (MDIO) and management data clock (MDC). The MII, GMII, and TBI interfaces are defined for 3.3 V, and the RGMII and RTBI interfaces are defined for 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard *Reduced Pin-Count Interface for Gigabit Ethernet Physical Layer Device Specification*, Version 1.2a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in Section 8.3, "Ethernet Management Interface Electrical Characteristics."



8.2.3.1 TBI Transmit AC Timing Specifications

Table 29 provides the TBI transmit AC timing specifications.

Table 29. TBI Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
GTX_CLK clock period	t _{TTX}	—	8.0	—	ns
GTX_CLK duty cycle	t _{TTXH} /t _{TTX}	40	—	60	%
GTX_CLK to TBI data TXD[7:0], TX_ER, TX_EN delay	t _{TTKHDX}	1.0	—	5.0	ns
GTX_CLK clock rise (20%–80%)	t _{TTXR}	—	—	1.0	ns
GTX_CLK clock fall time (80%–20%)	t _{TTXF}	—	—	1.0	ns

Notes:

1. The symbols for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (X) or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}

Figure 14 shows the TBI transmit AC timing diagram.



Figure 14. TBI Transmit AC Timing Diagram

8.2.3.2 TBI Receive AC Timing Specifications

Table 30 provides the TBI receive AC timing specifications.

Table 30. TBI Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
PMA_RX_CLK clock period	t _{TRX}		16.0		ns
PMA_RX_CLK skew	t _{SKTRX}	7.5	—	8.5	ns
RX_CLK duty cycle	t _{TRXH} /t _{TRX}	40	_	60	%



8.2.4 RGMII and RTBI AC Timing Specifications

Table 31 presents the RGMII and RTBI AC timing specifications.

Table 31. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
Data to clock output skew (at transmitter)	t _{SKRGT}	-0.5	—	0.5	ns
Data to clock input skew (at receiver) ²	t _{SKRGT}	1.0	—	2.8	ns
Clock cycle duration ³	t _{RGT}	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T ^{4, 5}	t _{RGTH} /t _{RGT}	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX ^{3, 5}	t _{RGTH} /t _{RGT}	40	50	60	%
Rise time (20%–80%)	t _{RGTR}	—	—	0.75	ns
Fall time (80%–20%)	t _{RGTF}	—	—	0.75	ns

Notes:

1. In general, the clock reference symbol for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Also, the notation for rise (R) and fall (F) times follows the clock symbol. For symbols representing skews, the subscript is SK followed by the clock being skewed (RGT).

2. This implies that PC board design requires clocks to be routed so that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.

3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns \pm 40 ns and 40 ns \pm 4 ns, respectively.

4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned.

5. Duty cycle reference is $LV_{DD}/2$.



Table 32. MII Management DC Electrical Characteristics Powe	ered at 2.5 V (continued)
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Parameter	Symbol	Conditions	Min	Мах	Unit
Input high current	I _{IH}	$V_{IN}^{1} = LV_{DD}$	—	10	μA
Input low current	IIL	$V_{IN} = LV_{DD}$	-15	—	μA

Note:

1. The symbol V_{IN} , in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

Parameter	Symbol	Conditions		Min	Мах	Unit
Supply voltage (3.3 V)	LV _{DD}	—		2.97	3.63	V
Output high voltage	V _{OH}	I _{OH} = -1.0 mA	$LV_{DD} = Min$	2.10	LV _{DD} + 0.3	V
Output low voltage	V _{OL}	I _{OL} = 1.0 mA	$LV_{DD} = Min$	GND	0.50	V
Input high voltage	V _{IH}	—		2.00	_	V
Input low voltage	V _{IL}	—		—	0.80	V
Input high current	I _{IH}	LV _{DD} = Max	$V_{IN}^{1} = 2.1 V$	—	40	μA
Input low current	۱ _{IL}	LV _{DD} = Max	V _{IN} = 0.5 V	-600	_	μA

Note:

1. The symbol V_{IN} , in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

8.3.2 MII Management AC Electrical Specifications

Table 34 provides the MII management AC timing specifications.

Table 34. MII Management AC Timing Specifications

At recommended operating conditions with LV_{DD} is 3.3 V ± 10% or 2.5 V ± 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit	Notes
MDC frequency	f _{MDC}	—	2.5	—	MHz	2
MDC period	t _{MDC}	—	400	—	ns	—
MDC clock pulse width high	t _{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t _{MDKHDX}	10	—	70	ns	3
MDIO to MDC setup time	t _{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t _{MDDXKH}	0	—	—	ns	—
MDC rise time	t _{MDCR}			10	ns	_



Figure 30 provides the boundary-scan timing diagram.



Figure 30. Boundary-Scan Timing Diagram









14.2 Timer AC Timing Specifications

Table 48 provides the timer input and output AC timing specifications.

Table 48. Timers Input AC Timing Specifications¹

Parameter	Symbol ²	Min	Unit
Timers inputs—minimum pulse width	t _{TIWID}	20	ns

Notes:

1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.

2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

15 GPIO

This section describes the DC and AC electrical specifications for the GPIO.

15.1 GPIO DC Electrical Characteristics

Table 49 provides the DC electrical characteristics for the MPC8347EA GPIO.

Table 49.	GPIO	DC	Electrical	Characteristic	cs
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PArameter	Symbol	Condition	Min	Мах	Unit
Input high voltage	V _{IH}	_	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	—	_	±5	μA
Output high voltage	V _{OH}	I _{OH} = -8.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0 mA	_	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	—	0.4	V

15.2 GPIO AC Timing Specifications

Table 50 provides the GPIO input and output AC timing specifications.

Table 50. GPIO Input AC Timing Specifications¹

Parameter	Symbol ²	Min	Unit
GPIO inputs—minimum pulse width	t _{PIWID}	20	ns

Notes:

1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.

 GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by external synchronous logic. GPIO inputs must be valid for at least t_{PIWID} ns to ensure proper operation.



Package and Pin Listings

Figure 38 and Figure 39 represent the AC timings from Table 54. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 38 shows the SPI timings in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 38. SPI AC Timing in Slave Mode (External Clock) Diagram

Figure 39 shows the SPI timings in master mode (internal clock).



Note: The clock edge is selectable on SPI.



18 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8347EA is available in two packages—a tape ball grid array (TBGA) and a plastic ball grid array (PBGA). See Section 18.1, "Package Parameters for the MPC8347EA TBGA," Section 18.2, "Mechanical Dimensions for the MPC8347EA TBGA," Section 18.3, "Package Parameters for the MPC8347EA PBGA," and Section 18.4, "Mechanical Dimensions for the MPC8347EA PBGA."

18.1 Package Parameters for the MPC8347EA TBGA

The package parameters are provided in the following list. The package type is $35 \text{ mm} \times 35 \text{ mm}$, 672 tape ball grid array (TBGA).

Package outline	$35 \text{ mm} \times 35 \text{ mm}$
Interconnects	672



Package and Pin Listings

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GV _{DD}	A2, E2, G5, G6, J5, K4, K5, L4, N4, P5, R6, T6, U5, V1, W5, Y5, AA4, AB3, AC4, AD5, AF3, AG5, AH2, AH5, AH6, AJ6, AK6, AK8, AK9, AL6	Power for DDR DRAM I/O voltage (2.5 V)	GV _{DD}	
LV _{DD} 1	C9, D11	Power for three-speed Ethernet #1 and for Ethernet management interface I/O (2.5 V, 3.3 V)	LV _{DD} 1	_
LV _{DD} 2	C6, D9	Power for three-speed Ethernet #2 I/O (2.5 V, 3.3 V)	LV _{DD} 2	
V _{DD}	E19, E29, F7, F9, F11,F13, F15, F17, F18, F21, F23, F25, F29, H29, J6, K29, M29, N6, P29, T29, U30, V6, V29, W29, AB29, AC5, AD29, AF6, AF29, AH29, AJ8, AJ12, AJ14, AJ16, AJ18, AJ20, AJ21, AJ23, AJ25, AJ26, AJ27, AJ28, AJ29, AK10	Power for core (1.2 V nominal, 1.3 V for 667 MHz)	V _{DD}	_
OV _{DD}	B22, B28, C16, C17, C24, C26, D13, D15, D19, D29, E31, F28, G33, H30, L29, L32, N32, P31, R31, U32, W31, Y29, AA29, AC30, AE31, AF30, AG29, AJ17, AJ30, AK11, AL15, AL19, AL21, AL29, AL30, AM20, AM23, AM24, AM26, AM28, AN11, AN13	PCI, 10/100 Ethernet, and other standard (3.3 V)	OV _{DD}	_
MVREF1	M3	I	DDR reference voltage	_
MVREF2	AD2	I	DDR reference voltage	_

Table 55. MPC8347EA (TBGA) Pinout Listing (continued)



19 Clocking

Figure 42 shows the internal distribution of the clocks.



Figure 42. MPC8347EA Clock Subsystem

The primary clock source can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. When the MPC8347EA is configured as a PCI host device, CLKIN is its primary input clock. CLKIN feeds the PCI clock divider (÷2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The CFG_CLKIN_DIV configuration input selects whether CLKIN or CLKIN/2 is driven out on the PCI_SYNC_OUT signal. The OCCR[PCICD*n*] parameters select whether CLKIN or CLKIN/2 is driven out on the PCI_CLK_OUT signals.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the MPC8347EA to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input clock and the CLKIN signal should be tied to GND.



Addressed by This Document," for part ordering details and contact your Freescale Sales Representative or authorized distributor for more information.

Characteristic ¹	400 MHz	533 MHz	667 MHz	Unit
e300 core frequency (<i>core_clk</i>)	266–400	266–533	266–667	MHz
Coherent system bus frequency (<i>csb_clk</i>)	100–266	100–333	100–333	MHz
DDR1 memory bus frequency (MCK) ²	100–133	100–133	100–166.67	MHz
DDR2 memory bus frequency (MCK) ³	100–133	100–200	100–200	MHz
Local bus frequency (LCLKn) ⁴	16.67–133	16.67–133	16.67–133	MHz
PCI input frequency (CLKIN or PCI_CLK)	25–66	25–66	25–66	MHz
Security core maximum internal operating frequency	133	133	166	MHz
USB_DR, USB_MPH maximum internal operating frequency	133	133	166	MHz

Table 58. Operating Frequencies for TBGA

¹ The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen so that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies. The value of SCCR[ENCCM], SCCR[USBDRCM], and SCCR[USBMPHCM] must be programmed so that the maximum internal operating frequency of the Security core and USB modules does not exceed the respective values listed in this table.

² The DDR data rate is 2x the DDR memory bus frequency.

³ The DDR data rate is 2x the DDR memory bus frequency.

⁴ The local bus frequency is 1/2, 1/4, or 1/8 of the *lbiu_clk* frequency (depending on LCCR[CLKDIV]) which is in turn 1x or 2x the *csb_clk* frequency (depending on RCWL[LBIUCM]).

Table 59 provides the operating frequencies for the MPC8347EA PBGA under recommended operating conditions.

Table 59.	Operating	Frequencies	for PBGA

Parameter ¹	266 MHz	333 MHz	400 MHz	Unit
e300 core frequency (<i>core_clk</i>)	200–266	200–333	200–400	MHz
Coherent system bus frequency (<i>csb_clk</i>)	100–266			MHz
DDR1 memory bus frequency (MCK) ²	100–133		MHz	
DDR2 memory bus frequency (MCK) ³	100–133			MHz
Local bus frequency (LCLK <i>n</i>) ⁴	16.67–133		MHz	
PCI input frequency (CLKIN or PCI_CLK)	25–66		MHz	
Security core maximum internal operating frequency	133		MHz	
USB_DR, USB_MPH maximum internal operating frequency	133		MHz	

¹ The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen so that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies. The value of SCCR[ENCCM], SCCR[USBDRCM], and SCCR[USBMPHCM] must be programmed so that the maximum internal operating frequency of the Security core and USB modules does not exceed the respective values listed in this table.

² The DDR data rate is 2× the DDR memory bus frequency.



Thermal

Table 67 and Table 68 show heat sink thermal resistance for TBGA and PBGA of the MPC8347EA.

Heat Sink Accuming Theymal Crasse	Air Flow	35 × 35 mm TBGA	
neal Sink Assuming Thermal Grease		Thermal Resistance	
AAVID $30 \times 30 \times 9.4$ mm pin fin	Natural convection	10	
AAVID $30 \times 30 \times 9.4$ mm pin fin	1 m/s	6.5	
AAVID $30 \times 30 \times 9.4$ mm pin fin	2 m/s	5.6	
AAVID 31 \times 35 \times 23 mm pin fin	Natural convection	8.4	
AAVID 31 \times 35 \times 23 mm pin fin	1 m/s	4.7	
AAVID 31 \times 35 \times 23 mm pin fin	2 m/s	4	
Wakefield, $53 \times 53 \times 25$ mm pin fin	Natural convection	5.7	
Wakefield, $53 \times 53 \times 25$ mm pin fin	1 m/s	3.5	
Wakefield, $53 \times 53 \times 25$ mm pin fin	2 m/s	2.7	
MEI, $75 \times 85 \times 12$ no adjacent board, extrusion	Natural convection	6.7	
MEI, 75 \times 85 \times 12 no adjacent board, extrusion	1 m/s	4.1	
MEI, $75 \times 85 \times 12$ no adjacent board, extrusion	2 m/s	2.8	
MEI, 75 \times 85 \times 12 mm, adjacent board, 40 mm side bypass	1 m/s	3.1	

 Table 67. Heat Sink and Thermal Resistance of MPC8347EA (TBGA)

Table 68. Heat Sink and Thermal Resistance of MPC8347EA (PBGA)

Hoot Sink Accuming Thermal Graces	Air Elow	29 × 29 mm PBGA	
neat Sink Assuming Thermal Grease		Thermal Resistance	
AAVID $30 \times 30 \times 9.4$ mm pin fin	Natural convection	13.5	
AAVID $30 \times 30 \times 9.4$ mm pin fin	1 m/s	9.6	
AAVID $30 \times 30 \times 9.4$ mm pin fin	2 m/s	8.8	
AAVID 31 \times 35 \times 23 mm pin fin	Natural convection	11.3	
AAVID 31 \times 35 \times 23 mm pin fin	1 m/s	8.1	
AAVID 31 \times 35 \times 23 mm pin fin	2 m/s	7.5	
Wakefield, $53 \times 53 \times 25$ mm pin fin	Natural convection	9.1	
Wakefield, $53 \times 53 \times 25$ mm pin fin	1 m/s	7.1	
Wakefield, $53 \times 53 \times 25$ mm pin fin	2 m/s	6.5	
MEI, $75 \times 85 \times 12$ no adjacent board, extrusion	Natural convection	10.1	
MEI, $75 \times 85 \times 12$ no adjacent board, extrusion	1 m/s	7.7	
MEI, $75 \times 85 \times 12$ no adjacent board, extrusion	2 m/s	6.6	
MEI, $75 \times 85 \times 12$ mm, adjacent board, 40 mm side bypass	1 m/s	6.9	



Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com

The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com 888-642-7674

800-347-4572

20.3 Heat Sink Attachment

When heat sinks are attached, an interface material is required, preferably thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces that can lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. The recommended maximum force on the top of the package is 10 lb force (4.5 kg force). Any adhesive attachment should attach to painted or plastic surfaces, and its performance should be verified under the application requirements.

20.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimize the size of the clearance to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

 T_J = junction temperature (°C) T_C = case temperature of the package (°C) $R_{\partial JC}$ = junction-to-case thermal resistance (°C/W) P_D = power dissipation (W)