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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	-
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	672-LBGA
Supplier Device Package	672-LBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8347vvalfb

- Address translation units for address mapping between host and peripheral
- Dual address cycle for target
- Internal configuration registers accessible from PCI

- Security engine is optimized to handle all the algorithms associated with IPSec, SSL/TLS, SRTP, IEEE Std. 802.11i®, iSCSI, and IKE processing. The security engine contains four crypto-channels, a controller, and a set of crypto execution units (EUs):
  - Public key execution unit (PKEU) :
    - RSA and Diffie-Hellman algorithms
    - Programmable field size up to 2048 bits
    - Elliptic curve cryptography
    - F2m and F(p) modes
    - Programmable field size up to 511 bits
  - Data encryption standard (DES) execution unit (DEU)
    - DES and 3DES algorithms
    - Two key (K1, K2) or three key (K1, K2, K3) for 3DES
    - ECB and CBC modes for both DES and 3DES
  - Advanced encryption standard unit (AESU)
    - Implements the Rijndael symmetric-key cipher
    - Key lengths of 128, 192, and 256 bits
    - ECB, CBC, CCM, and counter (CTR) modes
  - XOR parity generation accelerator for RAID applications
  - ARC four execution unit (AFEU)
    - Stream cipher compatible with the RC4 algorithm
    - 40- to 128-bit programmable key
  - Message digest execution unit (MDEU)
    - SHA with 160-, 224-, or 256-bit message digest
    - MD5 with 128-bit message digest
    - HMAC with either algorithm
  - Random number generator (RNG)
  - Four crypto-channels, each supporting multi-command descriptor chains
    - Static and/or dynamic assignment of crypto-execution units through an integrated controller
    - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
- Universal serial bus (USB) dual role controller
  - USB on-the-go mode with both device and host functionality
  - Complies with USB specification Rev. 2.0
  - Can operate as a stand-alone USB device
    - One upstream facing port
    - Six programmable USB endpoints

  - Can operate as a stand-alone USB host controller
    - USB root hub with one downstream-facing port
    - Enhanced host controller interface (EHCI) compatible
    - High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
  - External PHY with UTMI, serial and UTMI+ low-pin interface (ULPI)
- Universal serial bus (USB) multi-port host controller
  - Can operate as a stand-alone USB host controller
    - USB root hub with one or two downstream-facing ports
    - Enhanced host controller interface (EHCI) compatible
    - Complies with *USB Specification Rev. 2.0*
  - High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
  - Direct connection to a high-speed device without an external hub
  - External PHY with serial and low-pin count (ULPI) interfaces
- Local bus controller (LBC)
  - Multiplexed 32-bit address and data operating at up to 133 MHz
  - Eight chip selects for eight external slaves
  - Up to eight-beat burst transfers
  - 32-, 16-, and 8-bit port sizes controlled by an on-chip memory controller
  - Three protocol engines on a per chip select basis:
    - General-purpose chip select machine (GPCM)
    - Three user-programmable machines (UPMs)
    - Dedicated single data rate SDRAM controller
  - Parity support
  - Default boot ROM chip select with configurable bus width (8-, 16-, or 32-bit)
- Programmable interrupt controller (PIC)
  - Functional and programming compatibility with the MPC8260 interrupt controller
  - Support for 8 external and 35 internal discrete interrupt sources
  - Support for 1 external (optional) and 7 internal machine checkstop interrupt sources
  - Programmable highest priority request
  - Four groups of interrupts with programmable priority
  - External and internal interrupts directed to host processor
  - Redirects interrupts to external $\overline{\text{INTA}}$ pin in core disable mode.
  - Unique vector number for each interrupt source
- Dual industry-standard I^2C interfaces
  - Two-wire interface
  - Multiple master support
  - Master or slave I^2C mode support

2.1.2 Power Supply Voltage Specification

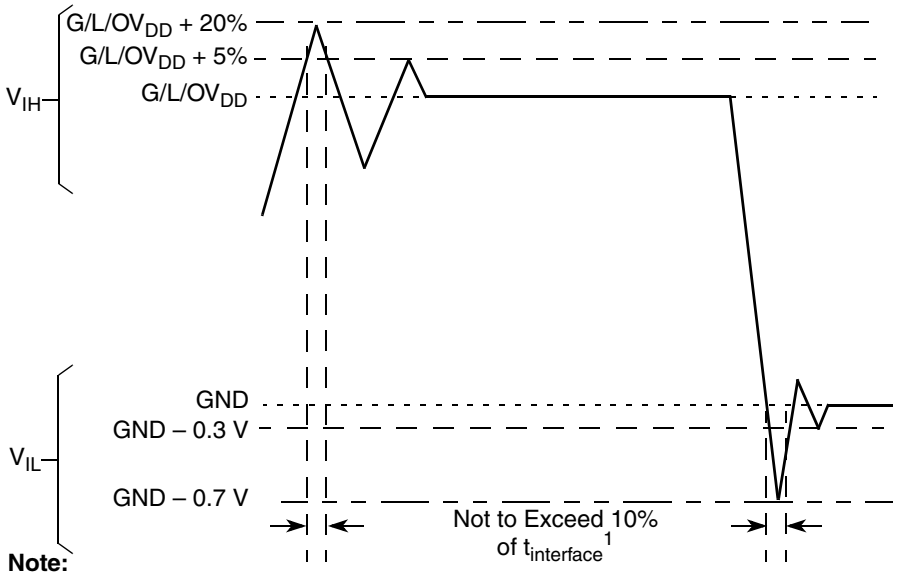
Table 2 provides the recommended operating conditions for the MPC8347EA. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Parameter	Symbol	Recommended Value	Unit	Notes
Core supply voltage for 667-MHz core frequency	V_{DD}	1.3 V ± 60 mV	V	1
Core supply voltage	V_{DD}	1.2 V ± 60 mV	V	1
PLL supply voltage for 667-MHz core frequency	AV_{DD}	1.3 V ± 60 mV	V	1
PLL supply voltage	AV_{DD}	1.2 V ± 60 mV	V	1
DDR and DDR2 DRAM I/O voltage	GV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	—
Three-speed Ethernet I/O supply voltage	LV_{DD1}	3.3 V ± 330 mV 2.5 V ± 125 mV	V	—
Three-speed Ethernet I/O supply voltage	LV_{DD2}	3.3 V ± 330 mV 2.5 V ± 125 mV	V	—
PCI, local bus, DUART, system control and power management, I^2C, and JTAG I/O voltage	OV_{DD}	3.3 V ± 330 mV	V	—

Note:
1 GV_{DD}, LV_{DD}, OV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8347EA.



Note:
1. $t_{interface}$ refers to the clock period associated with the bus clock interface.

Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}$

Figure 3 shows the undershoot and overshoot voltage of the PCI interface of the MPC8347EA for the 3.3-V signals, respectively.

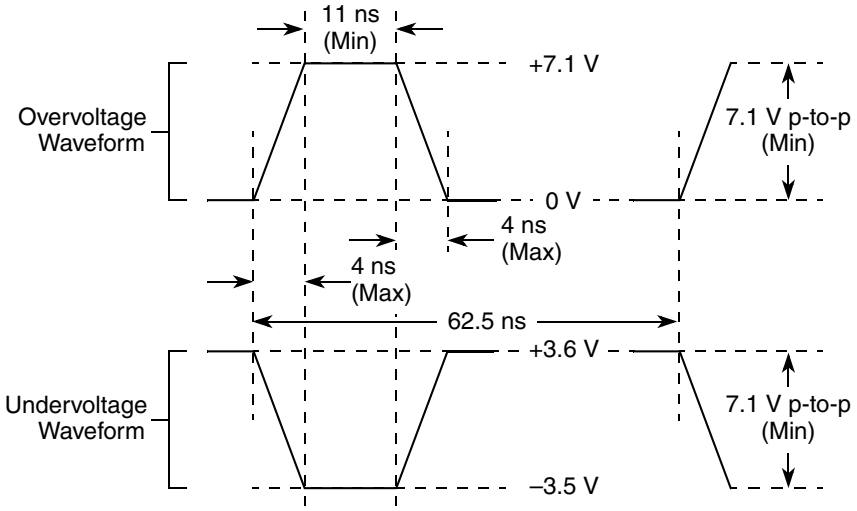


Figure 3. Maximum AC Waveforms on PCI Interface for 3.3-V Signaling

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	40	OV_{DD} = 3.3 V
PCI signals (not including PCI output clocks)	25	
PCI output clocks (including PCI_SYNC_OUT)	40	
DDR signal	18	GV_{DD} = 2.5 V
DDR2 signal	18 36 (half-strength mode)	GV_{DD} = 1.8 V
TSEC/10/100 signals	40	LV_{DD} = 2.5/3.3 V
DUART, system control, I^2C, JTAG, USB	40	OV_{DD} = 3.3 V
GPIO signals	40	OV_{DD} = 3.3 V, LV_{DD} = 2.5/3.3 V

2.2 Power Sequencing

This section details the power sequencing considerations for the MPC8347EA.

2.2.1 Power-Up Sequencing

MPC8347EAdoes not require the core supply voltage (V_{DD} and AV_{DD}) and I/O supply voltages (GV_{DD}, LV_{DD}, and OV_{DD}) to be applied in any particular order. During the power ramp up, before the power

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol [1]	Min	Max	Unit	Notes
266 MHz		1100	—		
200 MHz		1200	—		
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6
MDQS epilogue end	t_{DDKHME}	–0.6	0.6	ns	6

Notes:

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output goes invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are set up (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.
4. t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register and is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters are set to the same adjustment value. See the *MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual* for the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK(n) at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

Figure 6 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

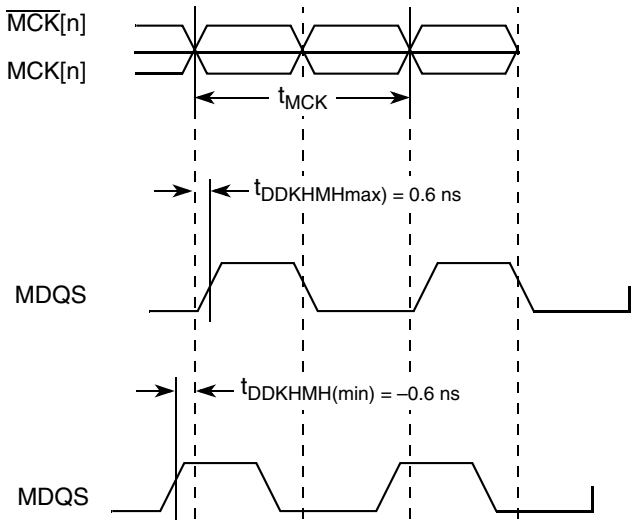


Figure 6. Timing Diagram for t_{DDKHMH}

8.1.1 TSEC DC Electrical Characteristics

GMII, MII, TBI, RGMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 23 and Table 24. The RGMII and RTBI signals in Table 24 are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 23. GMII/TBI and MII DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	LV_{DD}[2]	—		2.97	3.63	V
Output high voltage	V_{OH}	I_{OH} = –4.0 mA	LV_{DD} = Min	2.40	LV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 4.0 mA	LV_{DD} = Min	GND	0.50	V
Input high voltage	V_{IH}	—	—	2.0	LV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	—	–0.3	0.90	V
Input high current	I_{IH}	V_{IN}[1] = LV_{DD}		—	40	μA
Input low current	I_{IL}	V_{IN}[1] = GND		–600	—	μA

Notes:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.
2. GMII/MII pins not needed for RGMII or RTBI operation are powered by the OV_{DD} supply.

Table 24. RGMII/RTBI (When Operating at 2.5 V) DC Electrical Characteristics

Parameters	Symbol	Conditions		Min	Max	Unit
Supply voltage 2.5 V	LV_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	LV_{DD} = Min	2.00	LV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	LV_{DD} = Min	GND – 0.3	0.40	V
Input high voltage	V_{IH}	—	LV_{DD} = Min	1.7	LV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	LV_{DD} = Min	–0.3	0.70	V
Input high current	I_{IH}	V_{IN}[1] = LV_{DD}		—	10	μA
Input low current	I_{IL}	V_{IN}[1] = GND		–15	—	μA

Note:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

8.2 GMII, MII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

8.2.1 GMII Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

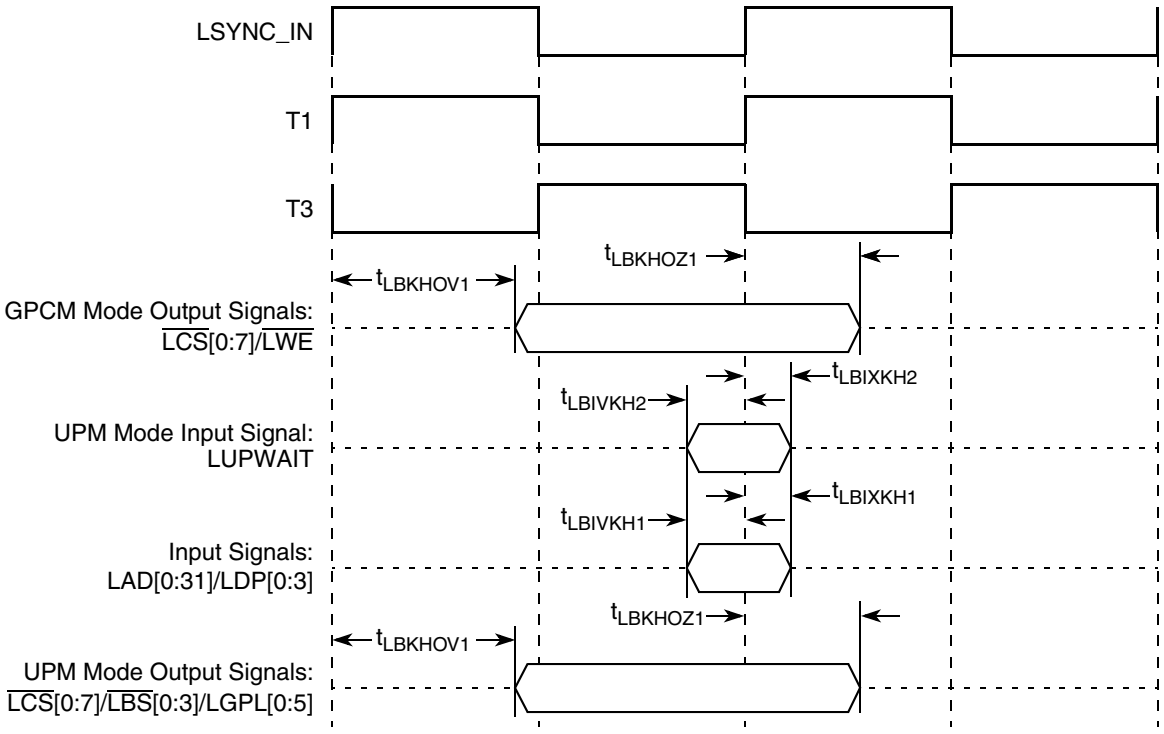


Figure 23. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Enabled)

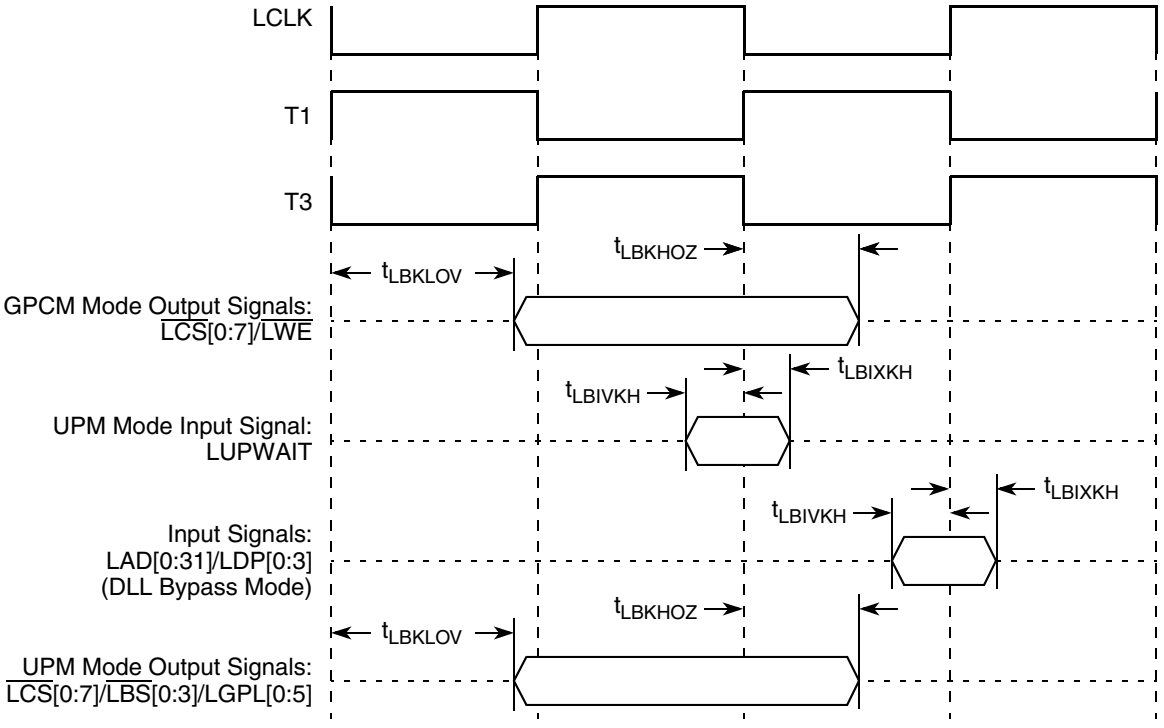


Figure 24. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Bypass Mode)

Figure 30 provides the boundary-scan timing diagram.

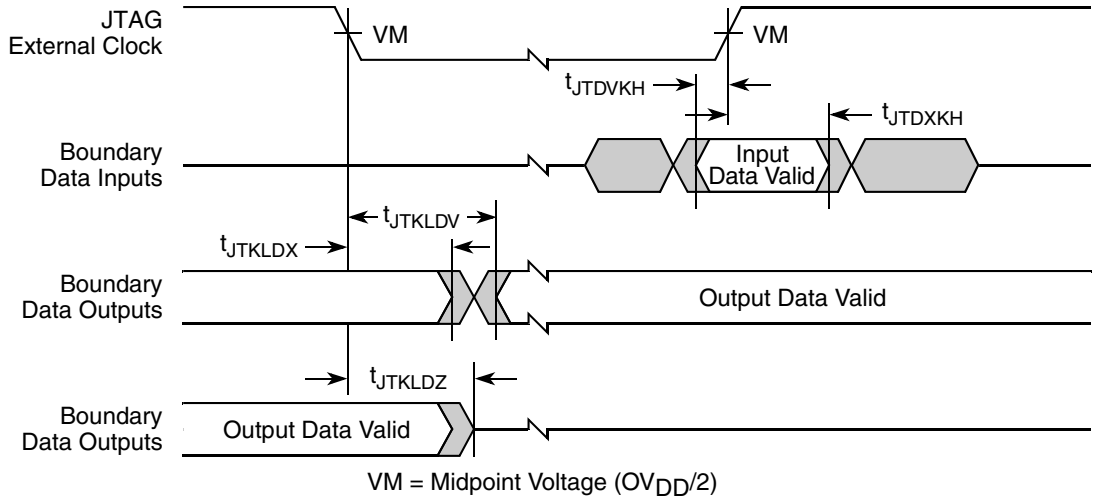


Figure 30. Boundary-Scan Timing Diagram

Figure 31 provides the test access port timing diagram.

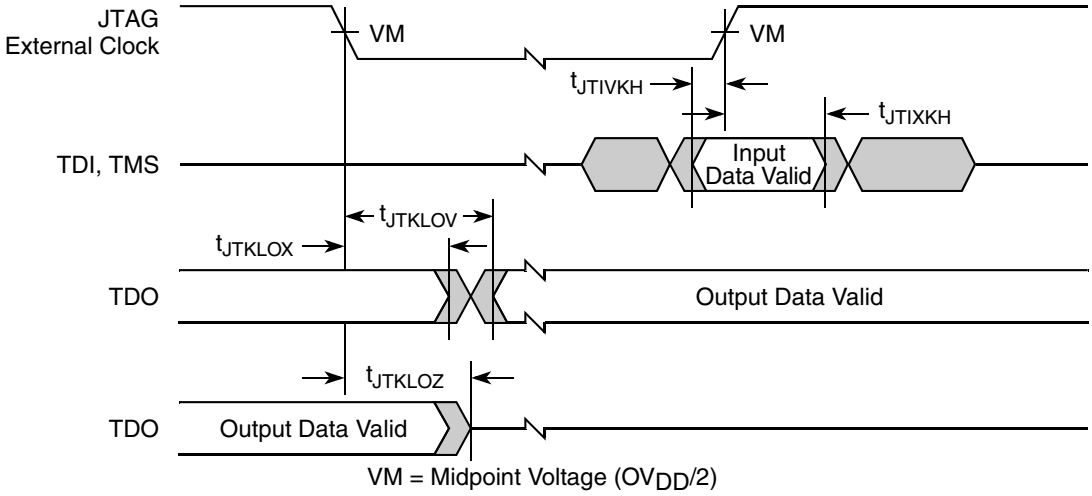


Figure 31. Test Access Port Timing Diagram

13 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8347EA.

13.1 PCI DC Electrical Characteristics

Table 44 provides the DC electrical characteristics for the PCI interface of the MPC8347EA.

Table 44. PCI DC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}$ (min) or	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL}$ (max)	–0.3	0.8	V
Input current	I_{IN}	V_{IN}[1]= 0 V or $V_{IN} = OV_{DD}$	—	±5	μA
High-level output voltage	V_{OH}	OV_{DD} = min, I_{OH} = –100 μA	OV_{DD} – 0.2	—	V
Low-level output voltage	V_{OL}	OV_{DD} = min, I_{OL} = 100 μA	—	0.2	V

Note:
1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1.

13.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8347EA. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the device is configured as a host or agent device. Table 45 provides the PCI AC timing specifications at 66 MHz.

Table 45. PCI AC Timing Specifications at 66 MHz[1]

Parameter	Symbol[2]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	6.0	ns	3
Output hold from clock	t_{PCKHOX}	1	—	ns	3
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	3, 4
Input setup to clock	t_{PCIVKH}	3.0	—	ns	3, 5

16 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins.

16.1 IPIC DC Electrical Characteristics

Table 51 provides the DC electrical characteristics for the external interrupt pins.

Table 51. IPIC DC Electrical Characteristics[1]

Parameter	Symbol	Condition	Min	Max	Unit	Notes
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	—	–0.3	0.8	V	—
Input current	I_{IN}	—	—	±5	μA	—
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V	2
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V	2

Notes:
1. This table applies for pins $\overline{\text{IRQ}}$[0:7], $\overline{\text{IRQ\_OUT}}$, and $\overline{\text{MCP\_OUT}}$.
2. $\overline{\text{IRQ\_OUT}}$ and $\overline{\text{MCP\_OUT}}$ are open-drain pins; thus V_{OH} is not relevant for those pins.

16.2 IPIC AC Timing Specifications

Table 52 provides the IPIC input and output AC timing specifications.

Table 52. IPIC Input AC Timing Specifications[1]

Parameter	Symbol[2]	Min	Unit
IPIC inputs—minimum pulse width	t_{PICWID}	20	ns

Notes:
1. Input specifications are measured at the 50 percent level of the IPIC input signals. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by external synchronous logic. IPIC inputs must be valid for at least t_{PICWID} ns to ensure proper operation in edge triggered mode.

17 SPI

This section describes the SPI DC and AC electrical specifications.

17.1 SPI DC Electrical Characteristics

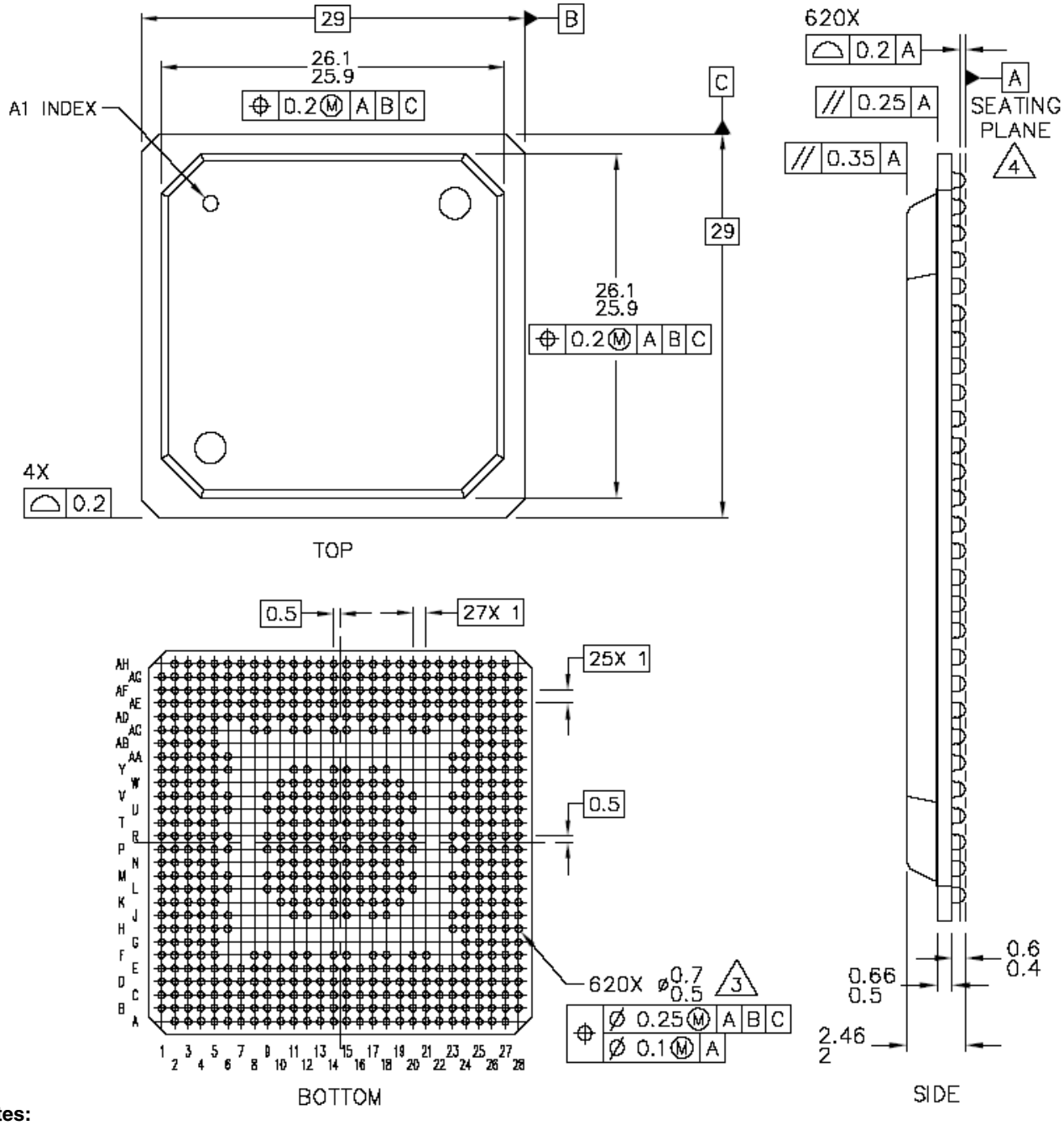
Table 53 provides the SPI DC electrical characteristics.

Table 53. SPI DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V

18.4 Mechanical Dimensions for the MPC8347EA PBGA

Figure 41 shows the mechanical dimensions and bottom surface nomenclature for the MPC8347EA, 620-PBGA package.



Notes:

1. All dimensions are in millimeters.
2. Dimensioning and tolerancing per ASME Y14. 5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

Figure 41. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC8347EA PBGA

Table 55. MPC8347EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MECC[0:4]/MSRCID[0:4]	W4, W3, Y3, AA6, T1	I/O	GV_{DD}	—
MECC[5]/MDVAL	U1	I/O	GV_{DD}	—
MECC[6:7]	Y1, Y6	I/O	GV_{DD}	—
MDM[0:8]	B1, F1, K1, R4, AD4, AJ1, AP3, AP7, Y4	O	GV_{DD}	—
MDQS[0:8]	B2, F5, J1, P2, AC1, AJ2, AN4, AL8, W2	I/O	GV_{DD}	—
MBA[0:1]	AD1, AA5	O	GV_{DD}	—
MA[0:14]	W1, U4, T3, R3, P1, M1, N1, L3, L1, K2, Y2, K3, J3, AP2, AN6	O	GV_{DD}	—
$\overline{\text{MWE}}$	AF1	O	GV_{DD}	—
$\overline{\text{MRAS}}$	AF4	O	GV_{DD}	—
$\overline{\text{MCAS}}$	AG3	O	GV_{DD}	—
$\overline{\text{MCS}}$[0:3]	AG2, AG1, AK1, AL4	O	GV_{DD}	—
MCKE[0:1]	H3, G1	O	GV_{DD}	3
MCK[0:5]	U2, F4, AM3, V3, F2, AN3	O	GV_{DD}	—
$\overline{\text{MCK}}$[0:5]	U3, E3, AN2, V4, E1, AM4	O	GV_{DD}	—
MODT[0:3]	AH3, AJ5, AH1, AJ4	O	GV_{DD}	—
MBA[2]	H4	O	GV_{DD}	—
MDIC0	AB1	I/O	—	10
MDIC1	AA1	I/O	—	10
Local Bus Controller Interface				
LAD[0:31]	AM13, AP13, AL14, AM14, AN14, AP14, AK15, AJ15, AM15, AN15, AP15, AM16, AL16, AN16, AP16, AL17, AM17, AP17, AK17, AP18, AL18, AM18, AN18, AP19, AN19, AM19, AP20, AK19, AN20, AL20, AP21, AN21	I/O	OV_{DD}	—
LDP[0]/$\overline{\text{CKSTOP\_OUT}}$	AM21	I/O	OV_{DD}	—
LDP[1]/$\overline{\text{CKSTOP\_IN}}$	AP22	I/O	OV_{DD}	—
LDP[2]/$\overline{\text{LCS}}$[4]	AN22	I/O	OV_{DD}	—
LDP[3]/$\overline{\text{LCS}}$[5]	AM22	I/O	OV_{DD}	—
LA[27:31]	AK21, AP23, AN23, AP24, AK22	O	OV_{DD}	—
$\overline{\text{LCS}}$[0:3]	AN24, AL23, AP25, AN25	O	OV_{DD}	—
$\overline{\text{LWE}}$[0:3]/LSDDQM[0:3]/$\overline{\text{LBS}}$[0:3]	AK23, AP26, AL24, AM25	O	OV_{DD}	—
LBCTL	AN26	O	OV_{DD}	—

Table 56. MPC8347EA (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MPH1_PCTL0/DR_TX_VALID_PCTL0	A26	O	OV_{DD}	—
MPH1_PCTL1/DR_TX_VALIDH_PCTL1	B25	O	OV_{DD}	—
MPH1_CLK/DR_CLK	A25	I	OV_{DD}	—
USB Port 0				
MPH0_D0_ENABLEN/DR_D8_CHGVBUS	D24	I/O	OV_{DD}	—
MPH0_D1_SER_TXD/DR_D9_DCHGVBUS	C24	I/O	OV_{DD}	—
MPH0_D2_VMO_SE0/DR_D10_DPPD	B24	I/O	OV_{DD}	—
MPH0_D3_SPEED/DR_D11_DMMD	A24	I/O	OV_{DD}	—
MPH0_D4_DP/DR_D12_VBUS_VLD	D23	I/O	OV_{DD}	—
MPH0_D5_DM/DR_D13_SESS_END	C23	I/O	OV_{DD}	—
MPH0_D6_SER_RCV/DR_D14	B23	I/O	OV_{DD}	—
MPH0_D7_DRVVBUS/DR_D15_IDPULLUP	A23	I/O	OV_{DD}	—
MPH0_NXT/DR_RX_ACTIVE_ID	D22	I	OV_{DD}	—
MPH0_DIR_DPPULLUP/DR_RESET	C22	I/O	OV_{DD}	—
MPH0_STP_SUSPEND/DR_TX_READY	B22	I/O	OV_{DD}	—
MPH0_PWRFAULT/DR_RX_VALIDH	A22	I	OV_{DD}	—
MPH0_PCTL0/DR_LINE_STATE0	E21	I/O	OV_{DD}	—
MPH0_PCTL1/DR_LINE_STATE1	D21	I/O	OV_{DD}	—
MPH0_CLK/DR_RX_VALID	C21	I	OV_{DD}	—
Programmable Interrupt Controller				
$\overline{\text{MCP\_OUT}}$	E8	O	OV_{DD}	2
$\overline{\text{IRQ}}$0/$\overline{\text{MCP_IN}}$/GPIO2[12]	J28	I/O	OV_{DD}	—
$\overline{\text{IRQ}}$[1:5]/GPIO2[13:17]	K25, J25, H26, L24, G27	I/O	OV_{DD}	—
$\overline{\text{IRQ}}$[6]/GPIO2[18]/CKSTOP_OUT	G28	I/O	OV_{DD}	—
$\overline{\text{IRQ}}$[7]/GPIO2[19]/CKSTOP_IN	J26	I/O	OV_{DD}	—
Ethernet Management Interface				
EC_MDC	Y24	O	LV_{DD1}	—
EC_MDIO	Y25	I/O	LV_{DD1}	11
Gigabit Reference Clock				
EC_GTX_CLK125	Y26	I	LV_{DD1}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_COL/GPIO2[20]	M26	I/O	OV_{DD}	—
TSEC1_CRS/GPIO2[21]	U25	I/O	LV_{DD1}	—
TSEC1_GTX_CLK	V24	O	LV_{DD1}	3

Table 56. MPC8347EA (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$LV_{DD}1$	U20, W25	Power for three-speed Ethernet #1 and for Ethernet management interface I/O (2.5 V, 3.3 V)	$LV_{DD}1$	—
$LV_{DD}2$	V20, Y23	Power for three-speed Ethernet #2 I/O (2.5 V, 3.3 V)	$LV_{DD}2$	—
V_{DD}	J11, J12, J15, K10, K11, K12, K13, K14, K15, K16, K17, K18, K19, L10, L11, L18, L19, M10, M19, N10, N19, P9, P10, P19, R10, R19, R20, T10, T19, U10, U19, V10, V11, V18, V19, W11, W12, W13, W14, W15, W16, W17, W18	Power for core (1.2 V)	V_{DD}	—
OV_{DD}	B27, D3, D11, D19, E15, E23, F5, F8, F11, F14, F17, F20, G24, H23, H24, J6, J14, J17, J18, K4, L9, L20, L23, L25, M6, M9, M20, P5, P20, P23, R6, R9, R24, U23, V4, V6	PCI, 10/100 Ethernet, and other standard (3.3 V)	OV_{DD}	—
MVREF1	AF19	I	DDR reference voltage	—
MVREF2	AE10	I	DDR reference voltage	—
No Connection				
NC	V1, V2, V5	—	—	—

Notes:
1. This pin is an open-drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to OV_{DD}.
2. This pin is an open-drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to OV_{DD}.
3. During reset, this output is actively driven rather than three-stated.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull-up if the chip is in PCI host mode. Follow the PCI specifications.
6. This pin must always be tied to GND.
7. This pin must always be left not connected.
8. Thermal sensitive resistor.
9. It is recommended that MDIC0 be tied to GRD using an 18 Ω resistor and MDIC1 be tied to DDR power using an 18 Ω resistor.
10. TSEC1_TXD[3] is required an external pull-up resistor. For proper functionality of the device, this pin must be pulled up or actively driven high during a hard reset. No external pull-down resistors are allowed to be attached to this net.
11. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to LV_{DD1}.
12. For systems that boot from local bus (GPCM)-controlled NOR flash, a pullup on LGPL4 is required.

As shown in Figure 42, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create the coherent system bus clock (*csb_clk*), the internal clock for the DDR controller (*ddr_clk*), and the internal clock for the local bus interface unit (*lbiu_clk*).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb\_clk = \{PCI\_SYNC\_IN \times (1 + CFG\_CLKIN\_DIV)\} \times SPMF$$

In PCI host mode, PCI_SYNC_IN × (1 + CFG_CLKIN_DIV) is the CLKIN frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL), which is loaded at power-on reset or by one of the hard-coded reset options. See the chapter on reset, clocking, and initialization in the *MPC8349EA Reference Manual* for more information on the clock subsystem.

The internal *ddr_clk* frequency is determined by the following equation:

$$ddr\_clk = csb\_clk \times (1 + RCWL[DDRCM])$$

ddr_clk is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{\text{MCK}}$). However, the data rate is the same frequency as *ddr_clk*.

The internal *lbiu_clk* frequency is determined by the following equation:

$$lbiu\_clk = csb\_clk \times (1 + RCWL[LBIUCM])$$

lbiu_clk is not the external local bus frequency; *lbiu_clk* passes through the LBIU clock divider to create the external local bus clock outputs (LSYNC_OUT and LCLK[0:2]). The LBIU clock divider ratio is controlled by LCCR[CLKDIV].

In addition, some of the internal units may have to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory-mapped register after the device exits reset. Table 57 specifies which units have a configurable clock frequency.

Table 57. Configurable Clock Units

Unit	Default Frequency	Options
TSEC1	*csb_clk/3*	Off, *csb_clk, csb_clk/2, csb_clk/3*
TSEC2, I^2C1	*csb_clk/3*	Off, *csb_clk, csb_clk/2, csb_clk/3*
Security core	*csb_clk/3*	Off, *csb_clk,* csb_clk/2, *csb_clk/3*
USB DR, USB MPH	*csb_clk/3*	Off, csb_clk, csb_clk/2, *csb_clk/3*
PCI and DMA complex	*csb_clk*	Off, *csb_clk*

Table 58 provides the operating frequencies for the MPC8347EA TBGA under recommended operating conditions (see Table 2). All frequency combinations shown in the table below may not be available. Maximum operating frequencies depend on the part ordered, see Section 22.1, “Part Numbers Fully

[3] The DDR data rate is 2× the DDR memory bus frequency.
[4] The local bus frequency is ½, ¼, or 1/8 of the *lbiu_clk* frequency (depending on LCCR[CLKDIV]) which is in turn 1× or 2× the *csb_clk* frequency (depending on RCWL[LBIUCM]).

19.1 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. Table 60 shows the multiplication factor encodings for the system PLL.

Table 60. System PLL Multiplication Factors

RCWL[SPMF]	System PLL Multiplication Factor
0000	× 16
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111	× 7
1000	× 8
1001	× 9
1010	× 10
1011	× 11
1100	× 12
1101	× 13
1110	× 14
1111	× 15

As described in Section 19, “Clocking,” the LBIUCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 61

Table 62. CSB Frequency Options for Agent Mode

CFG_CLKIN_DIV at Reset[1]	SPMF	*csb_clk* : Input Clock Ratio[2]	Input Clock Frequency (MHz)[2]			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
Low	0010	2 : 1				133
Low	0011	3 : 1			100	200
Low	0100	4 : 1		100	133	266
Low	0101	5 : 1		125	166	333
Low	0110	6 : 1	100	150	200	
Low	0111	7 : 1	116	175	233	
Low	1000	8 : 1	133	200	266	
Low	1001	9 : 1	150	225	300	
Low	1010	10 : 1	166	250	333	
Low	1011	11 : 1	183	275		
Low	1100	12 : 1	200	300		
Low	1101	13 : 1	216	325		
Low	1110	14 : 1	233			
Low	1111	15 : 1	250			
Low	0000	16 : 1	266			
High	0010	4 : 1		100	133	266
High	0011	6 : 1	100	150	200	
High	0100	8 : 1	133	200	266	
High	0101	10 : 1	166	250	333	
High	0110	12 : 1	200	300		
High	0111	14 : 1	233			
High	1000	16 : 1	266			

1 CFG_CLKIN_DIV doubles csb_clk if set high.
2 CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.
DDR2 memory may be used at 133 MHz provided that the memory components are specified for operation at this frequency.

19.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). Table 63 shows the encodings for RCWL[COREPLL]. COREPLL values that are not listed in Table 63 should be considered as reserved.

NOTE

Core VCO frequency = core frequency × VCO divider

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following list:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #12 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-567-8082
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-thermal.com	408-436-8770
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-2800
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102

Interface material vendors include the following:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01801 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials P.O. Box 994 Midland, MI 48686-0997 Internet: www.dowcorning.com	800-248-2481

21 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8347EA.

21.1 System Clocking

The MPC8347EA includes two PLLs:

1. The platform PLL generates the platform clock from the externally supplied CLKIN input. The frequency ratio between the platform and CLKIN is selected using the platform PLL ratio configuration bits as described in Section 19.1, “System PLL Configuration.”
2. The e300 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in Section 19.2, “Core PLL Configuration.”

21.2 PLL Power Supply Filtering

Each PLL gets power through independent power supply pins ($AV_{DD}1$, $AV_{DD}2$, respectively). The AV_{DD} level should always equal to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme.

There are a number of ways to provide power reliably to the PLLs, but the recommended solution is to provide four independent filter circuits as illustrated in Figure 43, one to each of the four AV_{DD} pins. Independent filters to each PLL reduce the opportunity to cause noise injection from one PLL to the other.

The circuit filters noise in the PLL resonant frequency range from 500 kHz to 10 MHz. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

To minimize noise coupled from nearby circuits, each circuit should be placed as closely as possible to the specific AV_{DD} pin being supplied. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

Figure 43 shows the PLL power supply filter circuit.

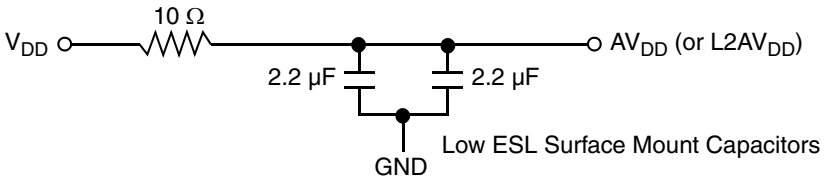


Figure 43. PLL Power Supply Filter Circuit

21.3 Decoupling Recommendations

Due to large address and data buses and high operating frequencies, the MPC8347EA can generate transient power surges and high frequency noise in its power supply, especially while driving large

However, while $\overline{\text{HRESET}}$ is asserted, these pins are treated as inputs, and the value on these pins is latched when $\overline{\text{PORESET}}$ deasserts. Then the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for the output pins.

21.7 Pull-Up Resistor Requirements

The MPC8347EA requires high resistance pull-up resistors (10 kΩ is recommended) on open-drain pins, including I^2C pins, and IPIC interrupt pins.

For more information on required pull-up resistors and the connections required for the JTAG interface, refer to application note AN2931, “PowerQUICC Design Checklist.”

22 Ordering Information

This section presents ordering information for the device discussed in this document, and it shows an example of how the parts are marked.

NOTE

The information in this document is accurate for revision 3.x silicon and later (in other words, for orderable part numbers ending in A or B). For information on revision 1.1 silicon and earlier versions, see the *MPC8347E PowerQUICC II Pro Integrated Host Processor Hardware Specifications* (Document Order No. MPC8347EEC).

22.1 Part Numbers Fully Addressed by This Document

Table 70 shows an analysis of the Freescale part numbering nomenclature for the MPC8347EA. The individual part numbers correspond to a maximum processor core frequency. Each part number also contains a revision code that refers to the die mask revision number. For available frequency configuration