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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	672-LBGA
Supplier Device Package	672-LBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8347zuagdb

- Up to four physical banks (chip selects), each bank up to 1 Gbyte independently addressable
- DRAM chip configurations from 64 Mbits to 1 Gbit with ×8/×16 data ports
- Full error checking and correction (ECC) support
- Support for up to 16 simultaneous open pages (up to 32 pages for DDR2)
- Contiguous or discontiguous memory mapping
- Read-modify-write support
- Sleep-mode support for SDRAM self refresh
- Auto refresh
- On-the-fly power management using CKE
- Registered DIMM support
- 2.5-V SSTL2 compatible I/O for DDR1, 1.8-V SSTL2 compatible I/O for DDR2

- Dual three-speed (10/100/1000) Ethernet controllers (TSECs)
  - Dual controllers designed to comply with IEEE 802.3™, 802.3u™, 820.3x™, 802.3z™, 802.3ac™ standards
  - Ethernet physical interfaces:
    - 1000 Mbps IEEE Std. 802.3 GMII/RGMII, IEEE Std. 802.3z TBI/RTBI, full-duplex
    - 10/100 Mbps IEEE Std. 802.3 MII full- and half-duplex
  - Buffer descriptors are backward-compatible with MPC8260 and MPC860T 10/100 programming models
  - 9.6-Kbyte jumbo frame support
  - RMON statistics support
  - Internal 2-Kbyte transmit and 2-Kbyte receive FIFOs per TSEC module
  - MII management interface for control and status
  - Programmable CRC generation and checking
- PCI interface
  - Designed to comply with *PCI Specification Revision 2.3*
  - Data bus width:
    - 32-bit data PCI interface operating at up to 66 MHz
  - PCI 3.3-V compatible
  - PCI host bridge capabilities
  - PCI agent mode on PCI interface
  - PCI-to-memory and memory-to-PCI streaming
  - Memory prefetching of PCI read accesses and support for delayed read transactions
  - Posting of processor-to-PCI and PCI-to-memory writes
  - On-chip arbitration supporting five masters on PCI
  - Accesses to all PCI address spaces
  - Parity supported
  - Selectable hardware-enforced coherency

  - On-chip digital filtering rejects spikes on the bus
  - System initialization data optionally loaded from I^2C-1 EPROM by boot sequencer embedded hardware
- DMA controller
  - Four independent virtual channels
  - Concurrent execution across multiple channels with programmable bandwidth control
  - Handshaking (external control) signals for all channels: $\overline{\text{DMA\_DREQ}}$[0:3], $\overline{\text{DMA\_DACK}}$[0:3], $\overline{\text{DMA\_DDONE}}$[0:3]
  - All channels accessible to local core and remote PCI masters
  - Misaligned transfer capability
  - Data chaining and direct mode
  - Interrupt on completed segment and chain
- DUART
  - Two 4-wire interfaces (RxD, TxD, RTS, CTS)
  - Programming model compatible with the original 16450 UART and the PC16550D
- Serial peripheral interface (SPI) for master or slave
- General-purpose parallel I/O (GPIO)
  - 52 parallel I/O pins multiplexed on various chip interfaces
- System timers
  - Periodic interrupt timer
  - Real-time clock
  - Software watchdog timer
  - Eight general-purpose timers
- Designed to comply with IEEE Std. 1149.1™, JTAG boundary scan
- Integrated PCI bus and SDRAM clock generation

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8347EA. The device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

supplies are stable and if the I/O voltages are supplied before the core voltage, there may be a period of time that all input and output pins will actively be driven and cause contention and excessive current from 3A to 5A. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD}) before the I/O voltage (GV_{DD}, LV_{DD}, and OV_{DD}) and assert $\overline{\text{PORESET}}$ before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V, see Figure 4.

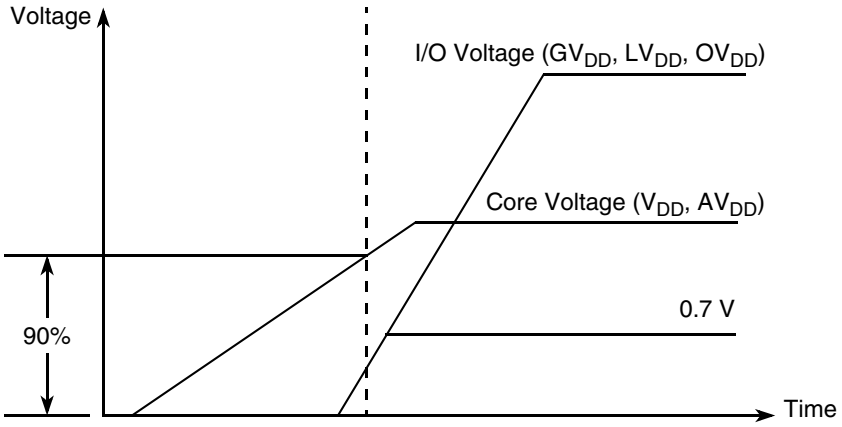


Figure 4. Power Sequencing Example

I/O voltage supplies (GV_{DD}, LV_{DD}, and OV_{DD}) do not have any ordering requirements with respect to one another.

3 Power Characteristics

The estimated typical power dissipation for the MPC8347EA device is shown in Table 4.

Table 4. MPC8347EA Power Dissipation[1]

	Core Frequency (MHz)	CSB Frequency (MHz)	Typical at T_J = 65	Typical[2,3]	Maximum[4]	Unit
PBGA	266	266	1.3	1.6	1.8	W
		133	1.1	1.4	1.6	W
	400	266	1.5	1.9	2.1	W
		133	1.4	1.7	1.9	W
	400	200	1.5	1.8	2.0	W
		100	1.3	1.7	1.9	W

Table 19 provides the input AC timing specifications for the DDR SDRAM interface.

Table 19. DDR and DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC/MDM	t_{CISKEW}			ps	1, 2
400 MHz		–600	600		3
333 MHz		–750	750		—
266 MHz		–750	750		—
200 MHz		–750	750		—

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the equation: $t_{DISKEW} = \pm (T/4 - abs(t_{CISKEW}))$; where T is the clock period and abs (t_{CISKEW}) is the absolute value of t_{CISKEW}.
3. This specification applies only to the DDR interface.

Figure 5 illustrates the DDR input timing diagram showing the t_{DISKEW} timing parameter.

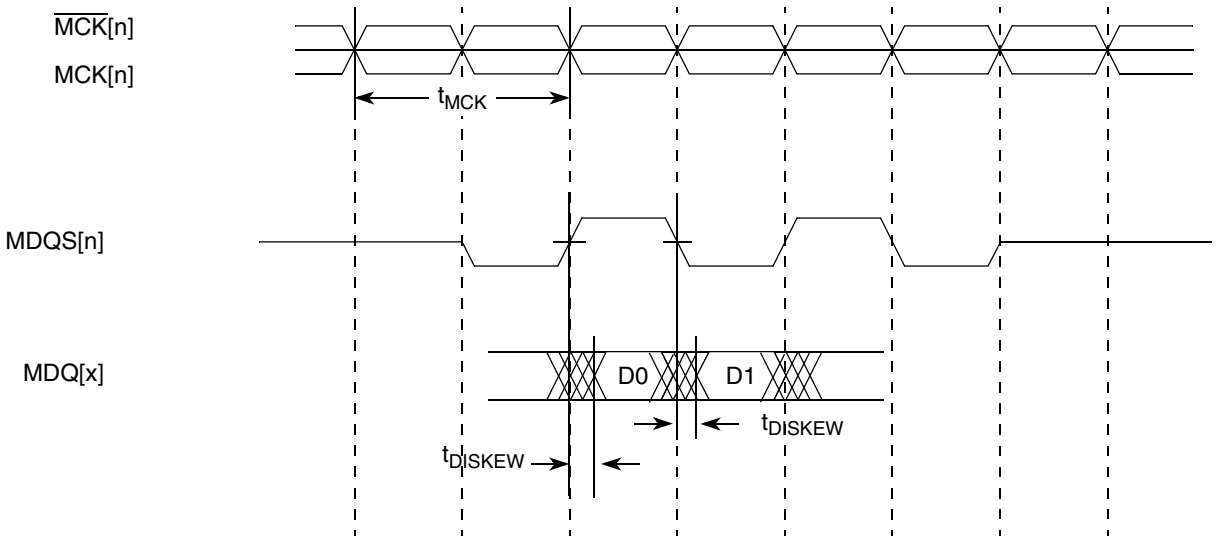


Figure 5. DDR Input Timing Diagram

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol [1]	Min	Max	Unit	Notes
266 MHz		1100	—		
200 MHz		1200	—		
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6
MDQS epilogue end	t_{DDKHME}	–0.6	0.6	ns	6

Notes:

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output goes invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are set up (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.
4. t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register and is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters are set to the same adjustment value. See the *MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual* for the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK(n) at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

Figure 6 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

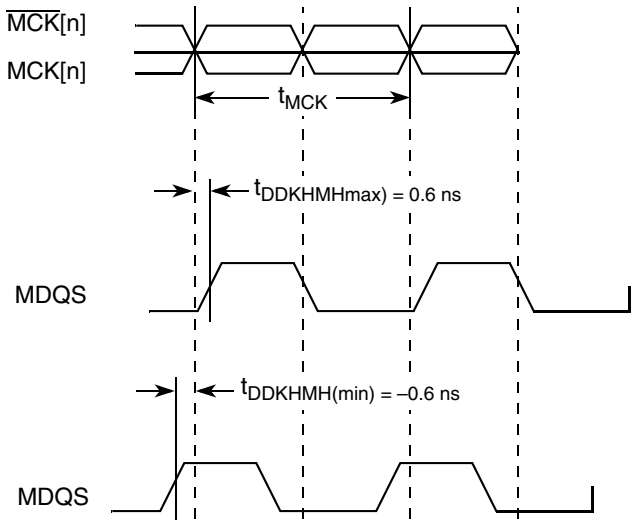


Figure 6. Timing Diagram for t_{DDKHMH}

8.1.1 TSEC DC Electrical Characteristics

GMII, MII, TBI, RGMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 23 and Table 24. The RGMII and RTBI signals in Table 24 are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 23. GMII/TBI and MII DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	LV_{DD}[2]	—		2.97	3.63	V
Output high voltage	V_{OH}	I_{OH} = –4.0 mA	LV_{DD} = Min	2.40	LV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 4.0 mA	LV_{DD} = Min	GND	0.50	V
Input high voltage	V_{IH}	—	—	2.0	LV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	—	–0.3	0.90	V
Input high current	I_{IH}	V_{IN}[1] = LV_{DD}		—	40	μA
Input low current	I_{IL}	V_{IN}[1] = GND		–600	—	μA

Notes:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.
2. GMII/MII pins not needed for RGMII or RTBI operation are powered by the OV_{DD} supply.

Table 24. RGMII/RTBI (When Operating at 2.5 V) DC Electrical Characteristics

Parameters	Symbol	Conditions		Min	Max	Unit
Supply voltage 2.5 V	LV_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	LV_{DD} = Min	2.00	LV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	LV_{DD} = Min	GND – 0.3	0.40	V
Input high voltage	V_{IH}	—	LV_{DD} = Min	1.7	LV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	LV_{DD} = Min	–0.3	0.70	V
Input high current	I_{IH}	V_{IN}[1] = LV_{DD}		—	10	μA
Input low current	I_{IL}	V_{IN}[1] = GND		–15	—	μA

Note:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

8.2 GMII, MII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

8.2.1 GMII Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

8.2.1.1 GMII Transmit AC Timing Specifications

Table 25 provides the GMII transmit AC timing specifications.

Table 25. GMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
GTX_CLK clock period	t_{GTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{GTXH}/t_{GTX}	43.75	—	56.25	%
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX}	0.5	—	5.0	ns
GTX_CLK clock rise time (20%–80%)	t_{GTXR}	—	—	1.0	ns
GTX_CLK clock fall time (80%–20%)	t_{GTXF}	—	—	1.0	ns

Notes:

1. The symbols for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 9 shows the GMII transmit AC timing diagram.

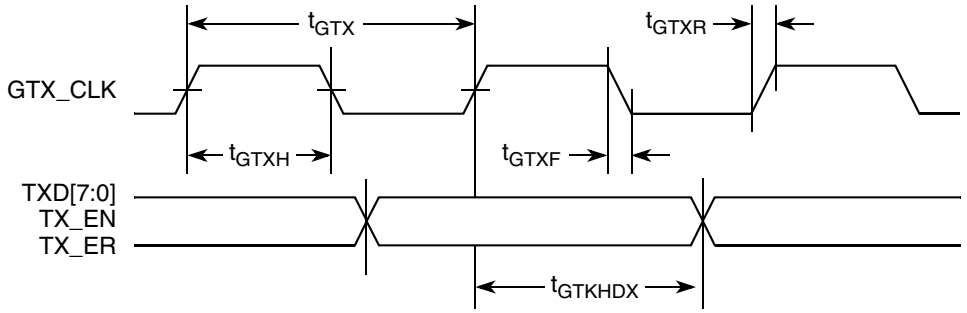


Figure 9. GMII Transmit AC Timing Diagram

8.2.1.2 GMII Receive AC Timing Specifications

Table 26 provides the GMII receive AC timing specifications.

Table 26. GMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
RX_CLK clock period	t_{GRX}	—	8.0	—	ns
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	40	—	60	%
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0.5	—	—	ns

10.2 Local Bus AC Electrical Specification

Table 38 and Table 39 describe the general timing parameters of the local bus interface of the MPC8347EA.

Table 38. Local Bus General Timing Parameters—DLL On

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	—	ns	2
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	1.5	—	ns	3, 4
LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	2.2	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	1.0	—	ns	3, 4
LUPWAIT Input hold from local bus clock	$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
Local bus clock to LALE rise	t_{LBKHLR}	—	4.5	ns	—
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	4.5	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	4.5	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	4.5	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	1	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	1	—	ns	3
Local bus clock to output high impedance for LAD/LDP	t_{LBKHOZ}	—	3.8	ns	8

Notes:

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to the rising edge of LSYNC_IN.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is not set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is set and when the load on the LALE output pin equals the load on the LAD output pins.
8. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

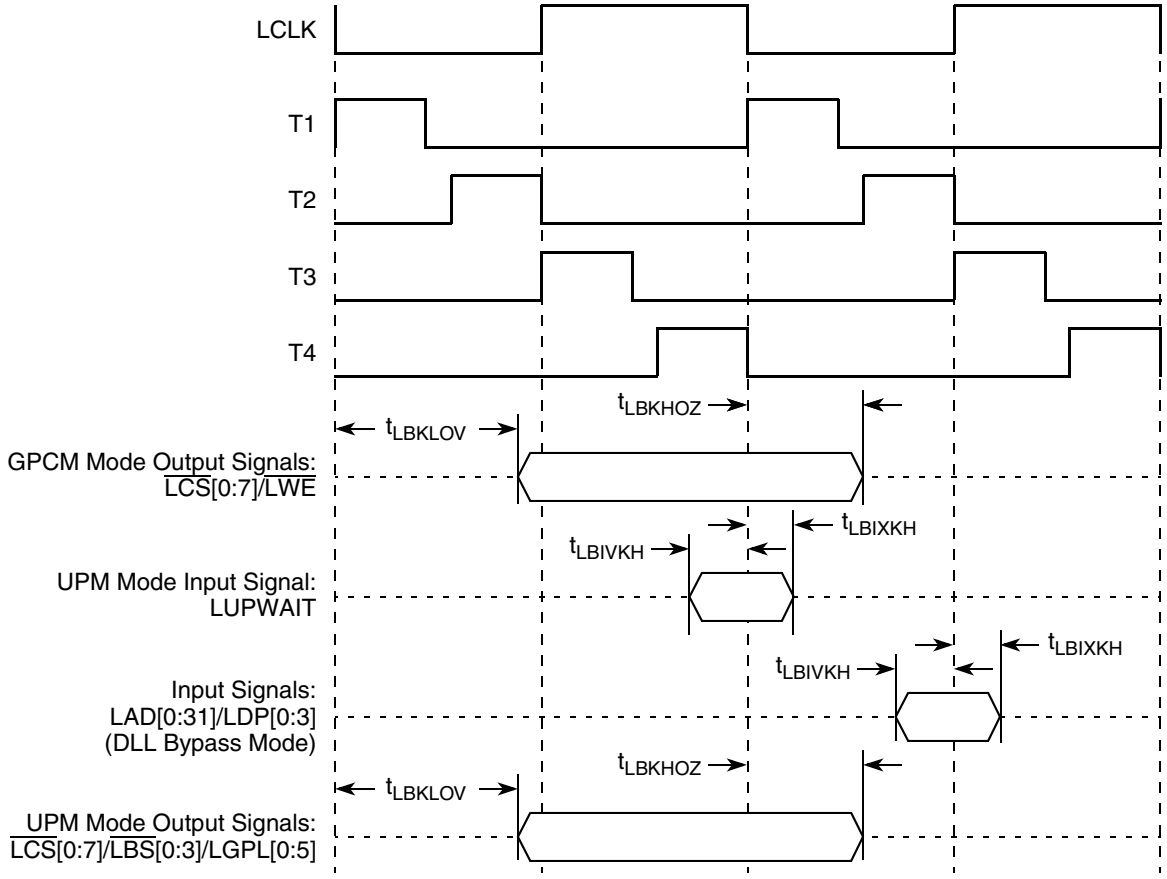


Figure 25. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (DLL Bypass Mode)

12 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8347EA.

12.1 I²C DC Electrical Characteristics

Table 42 provides the DC electrical characteristics for the I²C interface of the MPC8347EA.

Table 42. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	—
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1
Output fall time from V_{IH}(min) to V_{IL}(max) with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max)	I_I	–10	10	μA	4
Capacitance for each I/O pin	C_I	—	10	pF	—

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. Refer to the *MPC8349EA Integrated Host Processor Family Reference Manual,* for information on the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.

12.2 I²C AC Electrical Specifications

Table 43 provides the AC timing parameters for the I²C interface of the MPC8347EA. Note that all values refer to V_{IH}(min) and V_{IL}(max) levels (see Table 42).

Table 43. I²C AC Electrical Specifications

Parameter	Symbol[1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}	1.3	—	μs
High period of the SCL clock	t_{I2CH}	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs
Data setup time	t_{I2DVKH}	100	—	ns
Data hold time:CBUS compatible masters I²C bus devices	t_{I2DXKL}	— 0[2]	— 0.9[3]	μs

16 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins.

16.1 IPIC DC Electrical Characteristics

Table 51 provides the DC electrical characteristics for the external interrupt pins.

Table 51. IPIC DC Electrical Characteristics[1]

Parameter	Symbol	Condition	Min	Max	Unit	Notes
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	—	–0.3	0.8	V	—
Input current	I_{IN}	—	—	±5	μA	—
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V	2
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V	2

Notes:
1. This table applies for pins $\overline{\text{IRQ}}$[0:7], $\overline{\text{IRQ\_OUT}}$, and $\overline{\text{MCP\_OUT}}$.
2. $\overline{\text{IRQ\_OUT}}$ and $\overline{\text{MCP\_OUT}}$ are open-drain pins; thus V_{OH} is not relevant for those pins.

16.2 IPIC AC Timing Specifications

Table 52 provides the IPIC input and output AC timing specifications.

Table 52. IPIC Input AC Timing Specifications[1]

Parameter	Symbol[2]	Min	Unit
IPIC inputs—minimum pulse width	t_{PICWID}	20	ns

Notes:
1. Input specifications are measured at the 50 percent level of the IPIC input signals. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by external synchronous logic. IPIC inputs must be valid for at least t_{PICWID} ns to ensure proper operation in edge triggered mode.

17 SPI

This section describes the SPI DC and AC electrical specifications.

17.1 SPI DC Electrical Characteristics

Table 53 provides the SPI DC electrical characteristics.

Table 53. SPI DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V

Table 53. SPI DC Electrical Characteristics (continued)

Parameter	Symbol	Condition	Min	Max	Unit
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

17.2 SPI AC Timing Specifications

Table 54 provides the SPI input and output AC timing specifications.

Table 54. SPI AC Timing Specifications[1]

Parameter	Symbol[2]	Min	Max	Unit
SPI outputs valid—Master mode (internal clock) delay	t_{NIKHOV}	—	6	ns
SPI outputs hold—Master mode (internal clock) delay	t_{NIKHOX}	0.5	—	ns
SPI outputs valid—Slave mode (external clock) delay	t_{NEKHOV}	—	8	ns
SPI outputs hold—Slave mode (external clock) delay	t_{NEKHOX}	2	—	ns
SPI inputs—Master mode (internal clock input setup time	t_{NIIVKH}	4	—	ns
SPI inputs—Master mode (internal clock input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50 percent level of the rising edge of CLKIN to the 50 percent level of the signal. Timings are measured at the pin.
2. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).

Figure 37 provides the AC test load for the SPI.

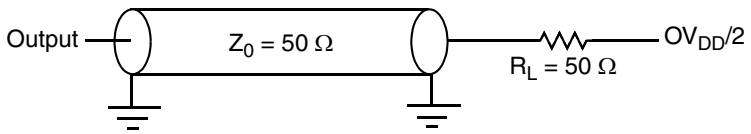
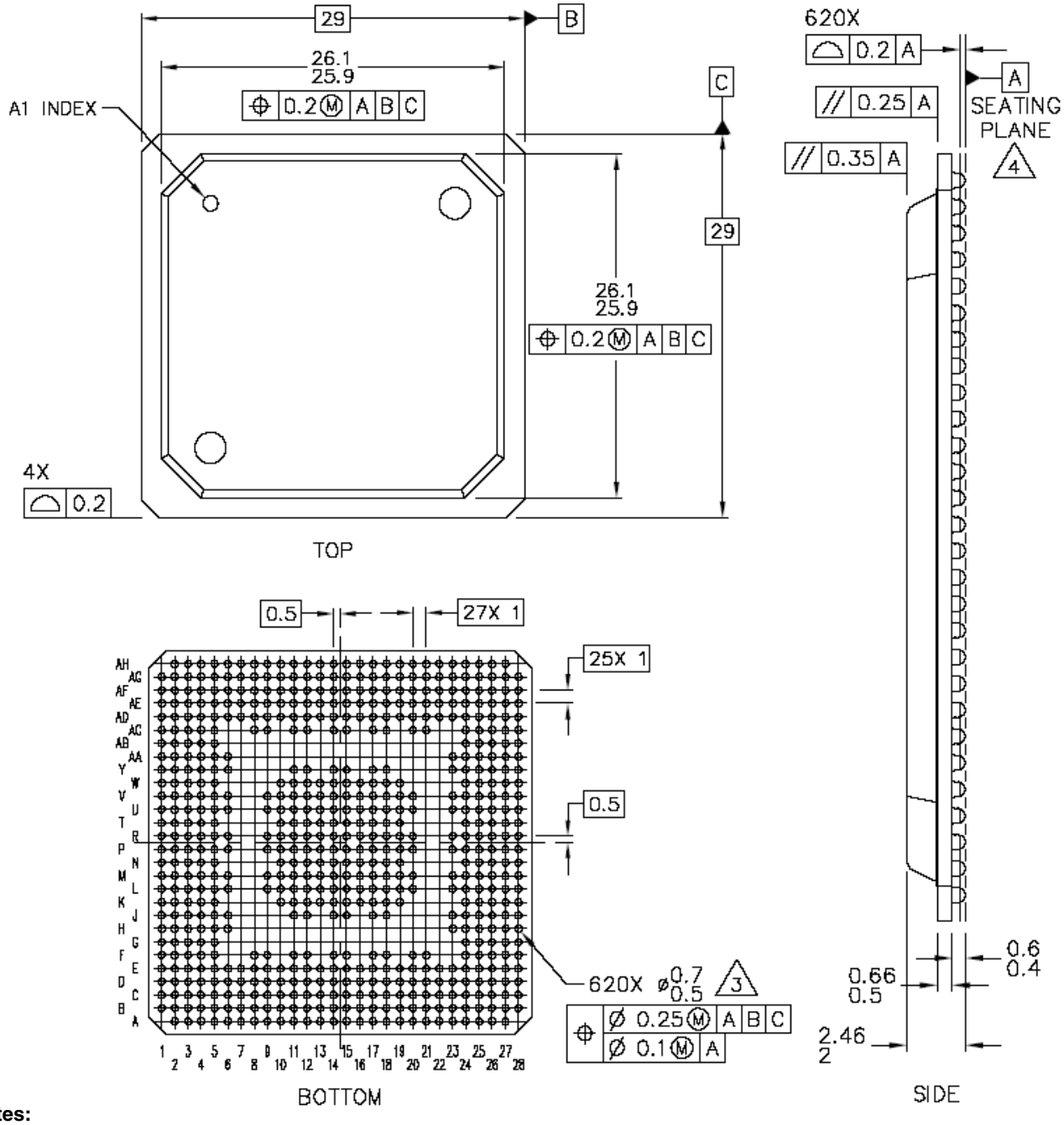


Figure 37. SPI AC Test Load

18.4 Mechanical Dimensions for the MPC8347EA PBGA

Figure 41 shows the mechanical dimensions and bottom surface nomenclature for the MPC8347EA, 620-PBGA package.



Notes:

1. All dimensions are in millimeters.
2. Dimensioning and tolerancing per ASME Y14. 5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

Figure 41. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC8347EA PBGA

Table 55. MPC8347EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
No Connection				
NC	W32, AA31, AA32, AA33, AA34, AB31, AB32, AB33, AB34, AC29, AC31, AC33, AC34, AD30, AD32, AD33, AD34, AE29, AE30, AH32, AH33, AH34, AM33, AJ31, AJ32, AJ33, AJ34, AK32, AK33, AK34, AM34, AL33, AL34, AK31, AH30, AC32, AE32, AH31, AL32, AG34, AE33, AF32, AE34, AF34, AF33, AG33, AG32, AL11, AM11, AP10, Y32, Y34, Y31, Y33	—	—	—

Notes:
1. This pin is an open-drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to OV_{DD}.
2. This pin is an open-drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to OV_{DD}.
3. During reset, this output is actively driven rather than three-stated.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull-up if the chip is in PCI host mode. Follow the PCI specifications.
6. This pin must always be tied to GND.
7. This pin must always be pulled up to OV_{DD}.
8. This pin must always be left not connected.
9. Thermal sensitive resistor.
10. It is recommended that MDIC0 be tied to GRD using an 18 Ω resistor and MDIC1 be tied to DDR power using an 18 Ω resistor.
11. TSEC1_TXD[3] is required an external pull-up resistor. For proper functionality of the device, this pin must be pulled up or actively driven high during a hard reset. No external pull-down resistors are allowed to be attached to this net.
12. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to LV_{DD1}.
13. For systems that boot from local bus (GPCM)-controlled NOR flash, a pullup on LGPL4 is required.

Table 56 provides the pinout listing for the MPC8347EA, 620 PBGA package.

Table 56. MPC8347EA (PBGA) Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI				
$\overline{\text{PCI1\_INTA/IRQ\_OUT}}$	D20	O	OV_{DD}	2
$\overline{\text{PCI1\_RESET\_OUT}}$	B21	O	OV_{DD}	—
PCI1_AD[31:0]	E19, D17, A16, A18, B17, B16, D16, B18, E17, E16, A15, C16, D15, D14, C14, A12, D12, B11, C11, E12, A10, C10, A9, E11, E10, B9, B8, D9, A8, C9, D8, C8	I/O	OV_{DD}	—
PCI1_C/$\overline{\text{BE}}$[3:0]	A17, A14, A11, B10	I/O	OV_{DD}	—
PCI1_PAR	D13	I/O	OV_{DD}	—
$\overline{\text{PCI1\_FRAME}}$	B14	I/O	OV_{DD}	5

Table 56. MPC8347EA (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
General Purpose I/O Timers				
GPIO1[0]/DMA_DREQ0/GTM1_TIN1/ GTM2_TIN2	D27	I/O	OV_{DD}	—
GPIO1[1]/DMA_DACK0/GTM1_TGATE1/ GTM2_TGATE2	E26	I/O	OV_{DD}	—
GPIO1[2]/DMA_DDONE0/GTM1_TOUT1	D28	I/O	OV_{DD}	—
GPIO1[3]/DMA_DREQ1/GTM1_TIN2/ GTM2_TIN1	G25	I/O	OV_{DD}	—
GPIO1[4]/DMA_DACK1/GTM1_TGATE2/ GTM2_TGATE1	J24	I/O	OV_{DD}	—
GPIO1[5]/DMA_DDONE1/GTM1_TOUT2/ GTM2_TOUT1	F26	I/O	OV_{DD}	—
GPIO1[6]/DMA_DREQ2/GTM1_TIN3/ GTM2_TIN4	E27	I/O	OV_{DD}	—
GPIO1[7]/DMA_DACK2/GTM1_TGATE3/ GTM2_TGATE4	E28	I/O	OV_{DD}	—
GPIO1[8]/DMA_DDONE2/GTM1_TOUT3	H25	I/O	OV_{DD}	—
GPIO1[9]/DMA_DREQ3/GTM1_TIN4/ GTM2_TIN3	F27	I/O	OV_{DD}	—
GPIO1[10]/DMA_DACK3/ GTM1_TGATE4/GTM2_TGATE3	K24	I/O	OV_{DD}	—
GPIO1[11]/DMA_DDONE3/ GTM1_TOUT4/GTM2_TOUT3	G26	I/O	OV_{DD}	—
USB Port 1				
MPH1_D0_ENABLEN/DR_D0_ENABLEN	C28	I/O	OV_{DD}	—
MPH1_D1_SER_TXD/DR_D1_SER_TXD	F25	I/O	OV_{DD}	—
MPH1_D2_VMO_SE0/DR_D2_VMO_SE0	B28	I/O	OV_{DD}	—
MPH1_D3_SPEED/DR_D3_SPEED	C27	I/O	OV_{DD}	—
MPH1_D4_DP/DR_D4_DP	D26	I/O	OV_{DD}	—
MPH1_D5_DM/DR_D5_DM	E25	I/O	OV_{DD}	—
MPH1_D6_SER_RCV/DR_D6_SER_RCV	C26	I/O	OV_{DD}	—
MPH1_D7_DRVVBUS/DR_D7_DRVVBUS	D25	I/O	OV_{DD}	—
MPH1_NXT/DR_SESS_VLD_NXT	B26	I	OV_{DD}	—
MPH1_DIR_DPPULLUP/ DR_XCVR_SEL_DPPULLUP	E24	I/O	OV_{DD}	—
MPH1_STP_SUSPEND/ DR_STP_SUSPEND	A27	O	OV_{DD}	—
MPH1_PWRFAULT/ DR_RX_ERROR_PWRFAULT	C25	I	OV_{DD}	—

Table 56. MPC8347EA (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
I^2C interface				
IIC1_SDA	E5	I/O	OV_{DD}	2
IIC1_SCL	A6	I/O	OV_{DD}	2
IIC2_SDA	B6	I/O	OV_{DD}	2
IIC2_SCL	E7	I/O	OV_{DD}	2
SPI				
SPIMOSI/$\overline{\text{LCS}}$[6]	D7	I/O	OV_{DD}	—
SPIMISO/$\overline{\text{LCS}}$[7]	C7	I/O	OV_{DD}	—
SPICLK	B7	I/O	OV_{DD}	—
SPISEL	A7	I	OV_{DD}	—
Clocks				
PCI_CLK_OUT[0:2]	Y1, W3, W2	O	OV_{DD}	—
PCI_CLK_OUT[3]/$\overline{\text{LCS}}$[6]	W1	O	OV_{DD}	—
PCI_CLK_OUT[4]/$\overline{\text{LCS}}$[7]	V3	O	OV_{DD}	—
PCI_SYNC_IN/PCI_CLOCK	U4	I	OV_{DD}	—
PCI_SYNC_OUT	U5	O	OV_{DD}	3
RTC/PIT_CLOCK	E9	I	OV_{DD}	—
CLKIN	W5	I	OV_{DD}	—
JTAG				
TCK	H27	I	OV_{DD}	—
TDI	H28	I	OV_{DD}	4
TDO	M24	O	OV_{DD}	3
TMS	J27	I	OV_{DD}	4
$\overline{\text{TRST}}$	K26	I	OV_{DD}	4
Test				
TEST	F28	I	OV_{DD}	6
TEST_SEL	T3	I	OV_{DD}	6
PMC				
$\overline{\text{QUIESCE}}$	K27	O	OV_{DD}	—
System Control				
$\overline{\text{PORESET}}$	K28	I	OV_{DD}	—
$\overline{\text{HRESET}}$	M25	I/O	OV_{DD}	1
$\overline{\text{SRESET}}$	L27	I/O	OV_{DD}	2

Table 56. MPC8347EA (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Thermal Management				
THERM0	B15	I	—	8
Power and Ground Signals				
$AV_{DD}1$	C15	Power for e300 PLL (1.2 V) nominal, 1.3 V for 667 MHz)	$AV_{DD}1$	—
$AV_{DD}2$	U1	Power for system PLL (1.2 V) nominal, 1.3 V for 667 MHz)	$AV_{DD}2$	—
$AV_{DD}3$	AF9	Power for DDR DLL (1.2 V nominal, 1.3 V for 667 MHz)		—
$AV_{DD}4$	U2	Power for LBIU DLL (1.2 V nominal, 1.3 V for 667 MHz)	$AV_{DD}4$	—
GND	A2, B1, B2, D10, D18, E6, E14, E22, F9, F12, F15, F18, F21, F24, G5, H6, J23, L4, L6, L12, L13, L14, L15, L16, L17, M11, M12, M13, M14, M15, M16, M17, M18, M23, N11, N12, N13, N14, N15, N16, N17, N18, P6, P11, P12, P13, P14, P15, P16, P17, P18, P24, R5, R11, R12, R13, R14, R15, R16, R17, R18, R23, T11, T12, T13, T14, T15, T16, T17, T18, U6, U11, U12, U13, U14, U15, U16, U17, U18, V12, V13, V14, V15, V16, V17, V23, V25, W4, Y6, AA23, AB24, AC5, AC8, AC11, AC14, AC17, AC20, AD9, AD15, AD21, AE12, AE18, AF3, AF26	—	—	—
GV_{DD}	U9, V9, W10, W19, Y11, Y12, Y14, Y15, Y17, Y18, AA6, AB5, AC9, AC12, AC15, AC18, AC21, AC24, AD6, AD8, AD14, AD20, AE5, AE11, AE17, AG2, AG27	Power for DDR DRAM I/O voltage (2.5 V)	GV_{DD}	—

and Table 62 show the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

Table 61. CSB Frequency Options for Host Mode

CFG_CLKIN_DIV at Reset[1]	SPMF	*csb_clk* : Input Clock Ratio[2]	Input Clock Frequency (MHz)[2]			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
Low	0010	2 : 1				133
Low	0011	3 : 1			100	200
Low	0100	4 : 1		100	133	266
Low	0101	5 : 1		125	166	333
Low	0110	6 : 1	100	150	200	
Low	0111	7 : 1	116	175	233	
Low	1000	8 : 1	133	200	266	
Low	1001	9 : 1	150	225	300	
Low	1010	10 : 1	166	250	333	
Low	1011	11 : 1	183	275		
Low	1100	12 : 1	200	300		
Low	1101	13 : 1	216	325		
Low	1110	14 : 1	233			
Low	1111	15 : 1	250			
Low	0000	16 : 1	266			
High	0010	2 : 1				133
High	0011	3 : 1			100	200
High	0100	4 : 1			133	266
High	0101	5 : 1			166	333
High	0110	6 : 1			200	
High	0111	7 : 1			233	
High	1000	8 : 1				

1 CFG_CLKIN_DIV selects the ratio between CLKIN and PCI_SYNC_OUT.

2 CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

DDR2 memory may be used at 133 MHz provided that the memory components are specified for operation at this frequency.

Table 67 and Table 68 show heat sink thermal resistance for TBGA and PBGA of the MPC8347EA.

Table 67. Heat Sink and Thermal Resistance of MPC8347EA (TBGA)

Heat Sink Assuming Thermal Grease	Air Flow	35 × 35 mm TBGA
		Thermal Resistance
AAVID 30 × 30 × 9.4 mm pin fin	Natural convection	10
AAVID 30 × 30 × 9.4 mm pin fin	1 m/s	6.5
AAVID 30 × 30 × 9.4 mm pin fin	2 m/s	5.6
AAVID 31 × 35 × 23 mm pin fin	Natural convection	8.4
AAVID 31 × 35 × 23 mm pin fin	1 m/s	4.7
AAVID 31 × 35 × 23 mm pin fin	2 m/s	4
Wakefield, 53 × 53 × 25 mm pin fin	Natural convection	5.7
Wakefield, 53 × 53 × 25 mm pin fin	1 m/s	3.5
Wakefield, 53 × 53 × 25 mm pin fin	2 m/s	2.7
MEI, 75 × 85 × 12 no adjacent board, extrusion	Natural convection	6.7
MEI, 75 × 85 × 12 no adjacent board, extrusion	1 m/s	4.1
MEI, 75 × 85 × 12 no adjacent board, extrusion	2 m/s	2.8
MEI, 75 × 85 × 12 mm, adjacent board, 40 mm side bypass	1 m/s	3.1

Table 68. Heat Sink and Thermal Resistance of MPC8347EA (PBGA)

Heat Sink Assuming Thermal Grease	Air Flow	29 × 29 mm PBGA
		Thermal Resistance
AAVID 30 × 30 × 9.4 mm pin fin	Natural convection	13.5
AAVID 30 × 30 × 9.4 mm pin fin	1 m/s	9.6
AAVID 30 × 30 × 9.4 mm pin fin	2 m/s	8.8
AAVID 31 × 35 × 23 mm pin fin	Natural convection	11.3
AAVID 31 × 35 × 23 mm pin fin	1 m/s	8.1
AAVID 31 × 35 × 23 mm pin fin	2 m/s	7.5
Wakefield, 53 × 53 × 25 mm pin fin	Natural convection	9.1
Wakefield, 53 × 53 × 25 mm pin fin	1 m/s	7.1
Wakefield, 53 × 53 × 25 mm pin fin	2 m/s	6.5
MEI, 75 × 85 × 12 no adjacent board, extrusion	Natural convection	10.1
MEI, 75 × 85 × 12 no adjacent board, extrusion	1 m/s	7.7
MEI, 75 × 85 × 12 no adjacent board, extrusion	2 m/s	6.6
MEI, 75 × 85 × 12 mm, adjacent board, 40 mm side bypass	1 m/s	6.9

However, while $\overline{\text{HRESET}}$ is asserted, these pins are treated as inputs, and the value on these pins is latched when $\overline{\text{PORESET}}$ deasserts. Then the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for the output pins.

21.7 Pull-Up Resistor Requirements

The MPC8347EA requires high resistance pull-up resistors (10 kΩ is recommended) on open-drain pins, including I^2C pins, and IPIC interrupt pins.

For more information on required pull-up resistors and the connections required for the JTAG interface, refer to application note AN2931, “PowerQUICC Design Checklist.”

22 Ordering Information

This section presents ordering information for the device discussed in this document, and it shows an example of how the parts are marked.

NOTE

The information in this document is accurate for revision 3.x silicon and later (in other words, for orderable part numbers ending in A or B). For information on revision 1.1 silicon and earlier versions, see the *MPC8347E PowerQUICC II Pro Integrated Host Processor Hardware Specifications* (Document Order No. MPC8347EEC).

22.1 Part Numbers Fully Addressed by This Document

Table 70 shows an analysis of the Freescale part numbering nomenclature for the MPC8347EA. The individual part numbers correspond to a maximum processor core frequency. Each part number also contains a revision code that refers to the die mask revision number. For available frequency configuration