NXP USA Inc. - KMPC8347ZUAJF Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	-
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	672-LBGA
Supplier Device Package	672-LBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8347zuajf

NOTE

The information in this document is accurate for revision 3.x silicon and later (in other words, for orderable part numbers ending in A or B). For information on revision 1.1 silicon and earlier versions, see the *MPC8347E PowerQUICC II Pro Integrated Host Processor Hardware Specifications*.

See Section 22.1, “Part Numbers Fully Addressed by This Document,” for silicon revision level determination.

1 Overview

This section provides a high-level overview of the device features. Figure 1 shows the major functional units within the MPC8347EA.

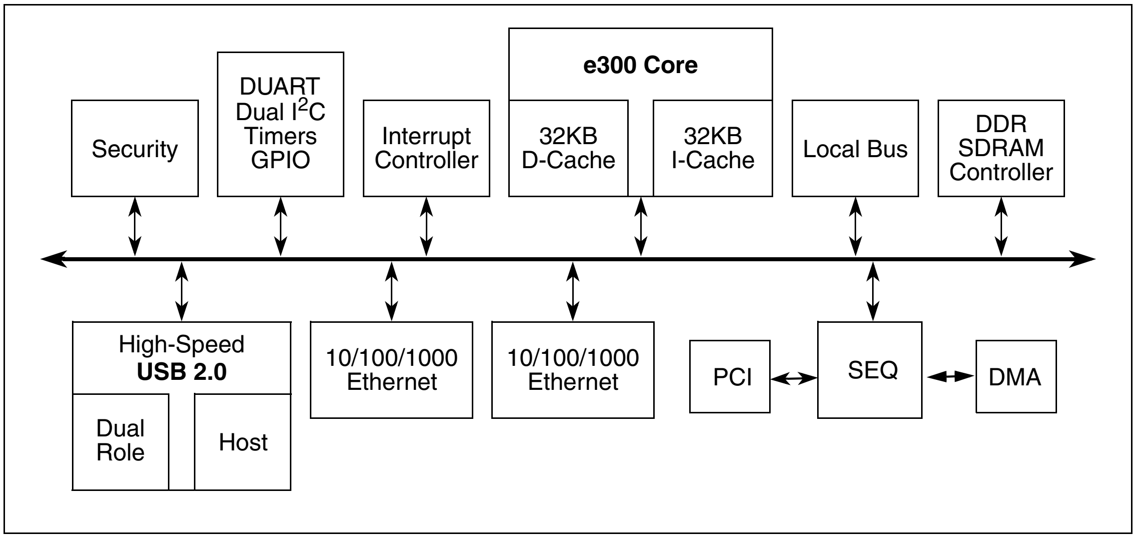


Figure 1. MPC8347EA Block Diagram

Major features of the device are as follows:

- Embedded PowerPC e300 processor core; operates at up to 667 MHz
  - High-performance, superscalar processor core
  - Floating-point, integer, load/store, system register, and branch processing units
  - 32-Kbyte instruction cache, 32-Kbyte data cache
  - Lockable portion of L1 cache
  - Dynamic power management
  - Software-compatible with the other Freescale processor families that implement Power Architecture technology
- Double data rate, DDR1/DDR2 SDRAM memory controller
  - Programmable timing supporting DDR1 and DDR2 SDRAM
  - 32- or 64-bit data interface, up to 400 MHz data rate for TBGA, 266 MHz for PBGA

- — Up to four physical banks (chip selects), each bank up to 1 Gbyte independently addressable
- — DRAM chip configurations from 64 Mbits to 1 Gbit with ×8/×16 data ports
- — Full error checking and correction (ECC) support
- — Support for up to 16 simultaneous open pages (up to 32 pages for DDR2)
- — Contiguous or discontiguous memory mapping
- — Read-modify-write support
- — Sleep-mode support for SDRAM self refresh
- — Auto refresh
- — On-the-fly power management using CKE
- — Registered DIMM support
- — 2.5-V SSTL2 compatible I/O for DDR1, 1.8-V SSTL2 compatible I/O for DDR2

- Dual three-speed (10/100/1000) Ethernet controllers (TSECs)
  - — Dual controllers designed to comply with IEEE 802.3™, 802.3u™, 820.3x™, 802.3z™, 802.3ac™ standards
  - — Ethernet physical interfaces:
    - – 1000 Mbps IEEE Std. 802.3 GMII/RGMII, IEEE Std. 802.3z TBI/RTBI, full-duplex
    - – 10/100 Mbps IEEE Std. 802.3 MII full- and half-duplex
  - — Buffer descriptors are backward-compatible with MPC8260 and MPC860T 10/100 programming models
  - — 9.6-Kbyte jumbo frame support
  - — RMON statistics support
  - — Internal 2-Kbyte transmit and 2-Kbyte receive FIFOs per TSEC module
  - — MII management interface for control and status
  - — Programmable CRC generation and checking
- PCI interface
  - — Designed to comply with *PCI Specification Revision 2.3*
  - — Data bus width:
    - – 32-bit data PCI interface operating at up to 66 MHz
  - — PCI 3.3-V compatible
  - — PCI host bridge capabilities
  - — PCI agent mode on PCI interface
  - — PCI-to-memory and memory-to-PCI streaming
  - — Memory prefetching of PCI read accesses and support for delayed read transactions
  - — Posting of processor-to-PCI and PCI-to-memory writes
  - — On-chip arbitration supporting five masters on PCI
  - — Accesses to all PCI address spaces
  - — Parity supported
  - — Selectable hardware-enforced coherency

Table 5 shows the estimated typical I/O power dissipation for MPC8347EA.

Table 5. MPC8347EA Typical I/O Power Dissipation

Interface	Parameter	DDR2 GV_{DD} (1.8 V)	DDR1 GV_{DD} (2.5 V)	OV_{DD} (3.3 V)	LV_{DD} (3.3 V)	LV_{DD} (2.5 V)	Unit	Comments
DDR I/O 65% utilization 2.5 V Rs = 20 Ω Rt = 50 Ω 2 pair of clocks	200 MHz, 32 bits	0.31	0.42	—	—	—	W	—
	200 MHz, 64 bits	0.42	0.55	—	—	—	W	—
	266 MHz, 32 bits	0.35	0.5	—	—	—	W	—
	266 MHz, 64 bits	0.47	0.66	—	—	—	W	—
	300 MHz,[1] 32 bits	0.37	0.54	—	—	—	W	—
	300 MHz,[1] 64 bits	0.50	0.7	—	—	—	W	—
	333 MHz,[1] 32 bits	0.39	0.58	—	—	—	W	—
	333 MHz,[1] 64 bits	0.53	0.76	—	—	—	W	—
	400 MHz,[1] 32 bits	0.44	—	—	—	—		—
	400 MHz,[1] 64 bits	0.59	—	—	—	—		—
PCI I/O load = 30 pF	33 MHz, 32 bits	—	—	0.04	—	—	W	—
	66 MHz, 32 bits	—	—	0.07	—	—	W	—
Local bus I/O load = 25 pF	167 MHz, 32 bits	—	—	0.34	—	—	W	—
	133 MHz, 32 bits	—	—	0.27	—	—	W	—
	83 MHz, 32 bits	—	—	0.17	—	—	W	—
	66 MHz, 32 bits	—	—	0.14	—	—	W	—
	50 MHz, 32 bits	—	—	0.11	—	—	W	—
TSEC I/O load = 25 pF	MII	—	—	—	0.01	—	W	Multiply by number of interfaces used.
	GMII or TBI	—	—	—	0.06	—	W	
	RGMII or RTBI	—	—	—	—	0.04	W	
USB	12 MHz	—	—	0.01	—	—	W	Multiply by 2 if using 2 ports.
	480 MHz	—	—	0.2	—	—	W	
Other I/O		—	—	0.01	—	—	W	—

[1] TBGA package only.

4.3 TSEC Gigabit Reference Clock Timing

Table 8 provides the TSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications.

Table 8. EC_GTX_CLK125 AC Timing Specifications

At recommended operating conditions with LV_{DD} = 2.5 ± 0.125 mV/ 3.3 V ± 165 mV

Parameter	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	t_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK125 rise and fall time LV_{DD} = 2.5 V LV_{DD} = 3.3 V	t_{G125R}/t_{G125F}	—	—	 0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	 45 47	—	 55 53	%	2
EC_GTX_CLK125 jitter	—	—	—	±150	ps	2

Notes:

1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for LV_{DD} = 2.5 V and from 0.6 and 2.7 V for LV_{DD} = 3.3 V.
2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. The EC_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 8.2.4, "RGMII and RTBI AC Timing Specifications for the duty cycle for 10Base-T and 100Base-T reference clock.

5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8347EA.

5.1 RESET DC Electrical Characteristics

Table 9 provides the DC electrical characteristics for the RESET pins of the MPC8347EA.

Table 9. RESET Pins DC Electrical Characteristics[1]

Parameter	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage[2]	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V

Table 11 lists the PLL and DLL lock times.

Table 11. PLL and DLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	µs	—
DLL lock times	7680	122,880	csb_clk cycles	1, 2

Notes:

1. DLL lock times are a function of the ratio between the output clock and the coherency system bus clock (csb_clk). A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.
2. The csb_clk is determined by the CLKIN and system PLL ratio. See Section 19, “Clocking.”

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8347EA. Note that DDR SDRAM is GV_{DD}(typ) = 2.5 V and DDR2 SDRAM is GV_{DD}(typ) = 1.8 V. The AC electrical specifications are the same for DDR and DRR2 SDRAM.

NOTE

> The information in this document is accurate for revision 3.0 silicon and later. For information on revision 1.1 silicon and earlier versions see the *MPC8347E PowerQUICC II Pro Integrated Host Processor Hardware Specifications*. See Section 22.1, “Part Numbers Fully Addressed by This Document,” for silicon revision level determination.

6.1 DDR and DDR2 SDRAM DC Electrical Characteristics

Table 12 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8347EA when GV_{DD}(typ) = 1.8 V.

Table 12. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.71	1.89	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.125$	$GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	–0.3	$MV_{REF} - 0.125$	V	—
Output leakage current	I_{OZ}	–9.9	9.9	µA	4
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA	—

Table 19 provides the input AC timing specifications for the DDR SDRAM interface.

Table 19. DDR and DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC/MDM	t_{CISKEW}			ps	1, 2
400 MHz		–600	600		3
333 MHz		–750	750		—
266 MHz		–750	750		—
200 MHz		–750	750		—

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the equation: t_{DISKEW} = ± (T/4 – abs (t_{CISKEW})); where T is the clock period and abs (t_{CISKEW}) is the absolute value of t_{CISKEW}.
3. This specification applies only to the DDR interface.

Figure 5 illustrates the DDR input timing diagram showing the t_{DISKEW} timing parameter.

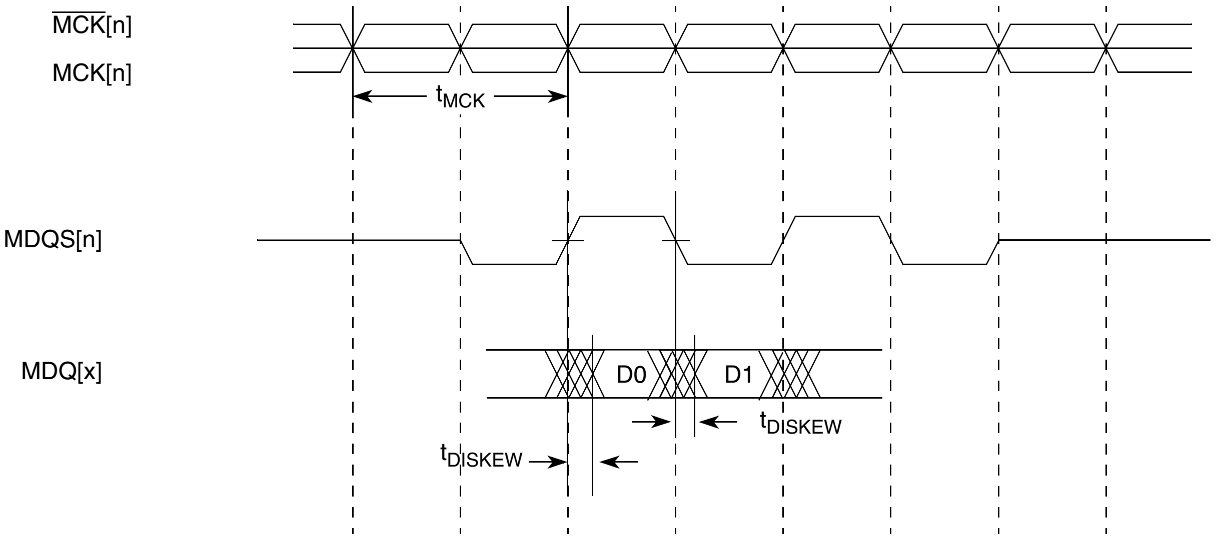


Figure 5. DDR Input Timing Diagram

6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 20 shows the DDR and DDR2 output AC timing specifications.

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol [1]	Min	Max	Unit	Notes
MCK[n] cycle time, (MCK[n]/$\overline{\text{MCK}}$[n] crossing) (PBGA package)	t_{MCK}	5	—	ns	2
MCK[n] cycle time, (MCK[n]/$\overline{\text{MCK}}$[n] crossing) (TBGA package)	t_{MCK}	7.5	—	ns	2
ADDR/CMD/MODT output setup with respect to MCK	t_{DDKHAS}			ns	3
400 MHz		1.95	—		
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	—		
ADDR/CMD/MODT output hold with respect to MCK	t_{DDKHAX}			ns	3
400 MHz		1.95	—		
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	—		
$\overline{\text{MCS}}$(n) output setup with respect to MCK	t_{DDKHCS}			ns	3
400 MHz		1.95	—		
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	—		
$\overline{\text{MCS}}$(n) output hold with respect to MCK	t_{DDKHCX}			ns	3
400 MHz		1.95	—		
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	—		
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
400 MHz		700	—		
333 MHz		775	—		
266 MHz		1100	—		
200 MHz		1200	—		
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
400 MHz		700	—		
333 MHz		900	—		

8.2.1.1 GMII Transmit AC Timing Specifications

Table 25 provides the GMII transmit AC timing specifications.

Table 25. GMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
GTX_CLK clock period	t_{GTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{GTXH}/t_{GTX}	43.75	—	56.25	%
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX}	0.5	—	5.0	ns
GTX_CLK clock rise time (20%–80%)	t_{GTXR}	—	—	1.0	ns
GTX_CLK clock fall time (80%–20%)	t_{GTXF}	—	—	1.0	ns

Notes:

1. The symbols for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 9 shows the GMII transmit AC timing diagram.

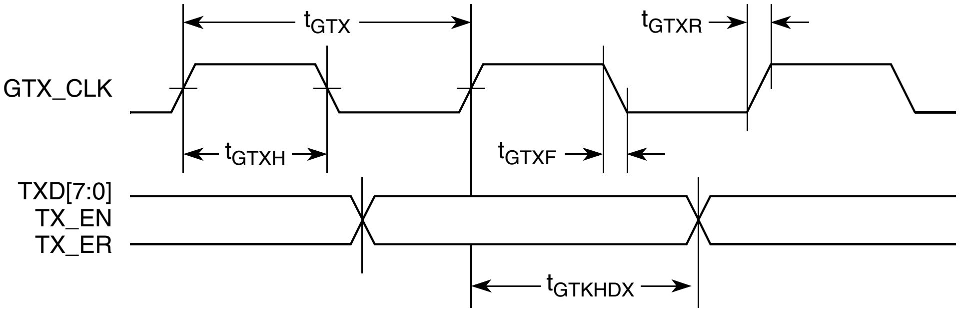


Figure 9. GMII Transmit AC Timing Diagram

8.2.1.2 GMII Receive AC Timing Specifications

Table 26 provides the GMII receive AC timing specifications.

Table 26. GMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
RX_CLK clock period	t_{GRX}	—	8.0	—	ns
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	40	—	60	%
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0.5	—	—	ns

Table 39. Local Bus General Timing Parameters—DLL Bypass[9]

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	15	—	ns	2
Input setup to local bus clock	t_{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock	t_{LBIXKH}	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
Local bus clock to output valid	t_{LBKLOV}	—	3	ns	3
Local bus clock to output high impedance for LAD/LDP	t_{LBKHOZ}	—	4	ns	8

Notes:

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to the falling edge of LCLK0 (for all outputs and for $\overline{\text{LGTA}}$ and LUPWAIT inputs) or the rising edge of LCLK0 (for all other inputs).
3. All signals are measured from $OV_{DD}/2$ of the rising/falling edge of LCLK0 to 0.4 × OV_{DD} of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is not set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.the
7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is not set and when the load on the LALE output pin equals to the load on the LAD output pins.
8. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
9. DLL bypass mode is not recommended for use at frequencies above 66 MHz.

Figure 20 provides the AC test load for the local bus.

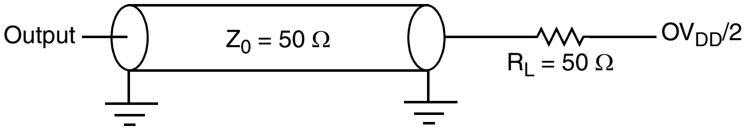


Figure 20. Local Bus C Test Load

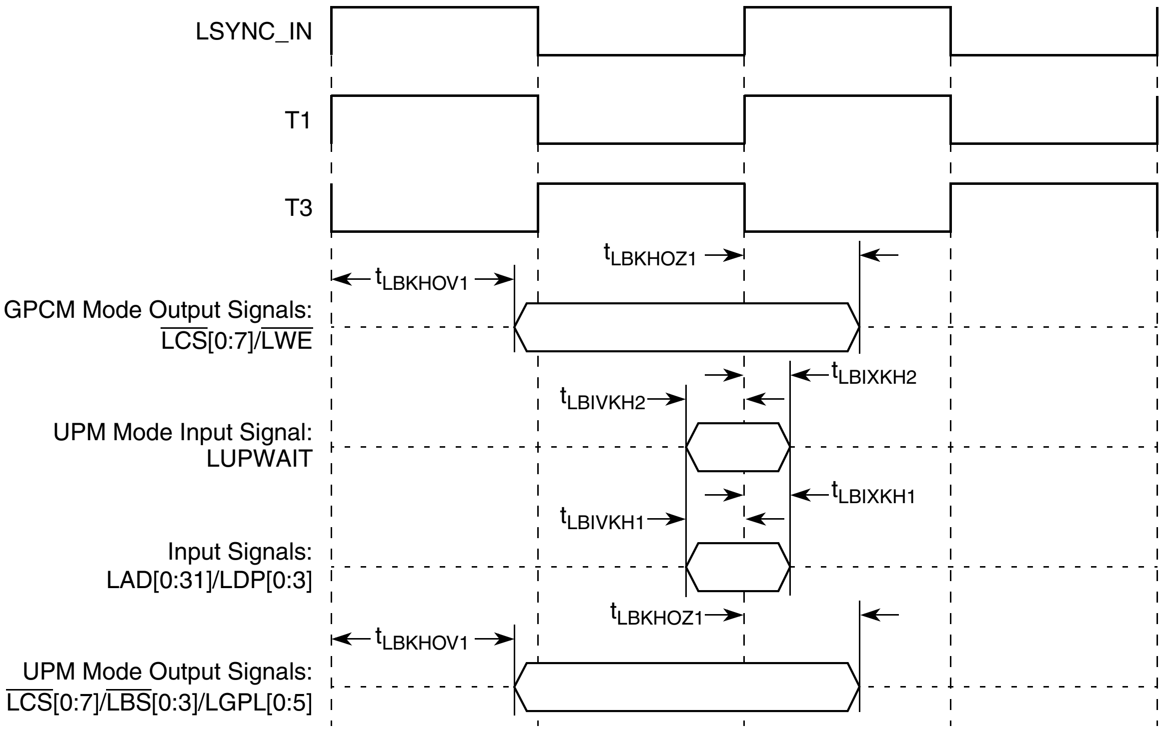


Figure 23. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Enabled)

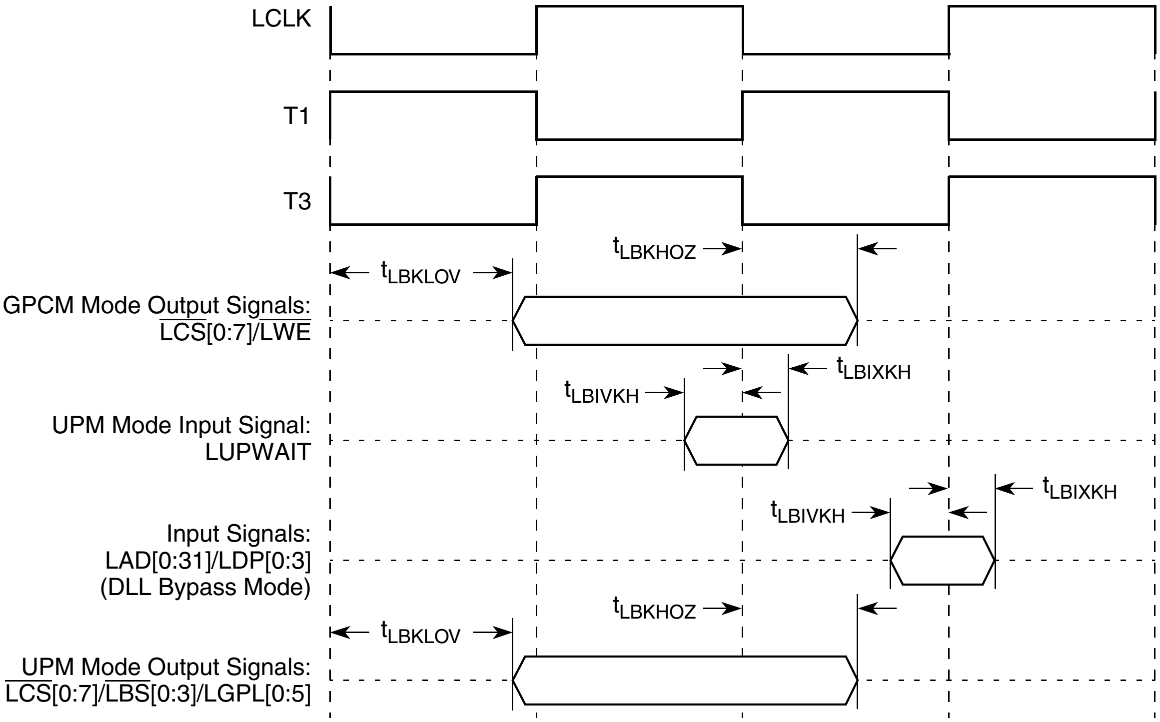


Figure 24. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Bypass Mode)

Table 41. JTAG AC Timing Specifications (Independent of CLKIN)[1] (continued)

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock to output high impedance:				ns	
Boundary-scan data	t_{JTKLDZ}	2	19		5, 6
TDO	t_{JTKLOZ}	2	9		

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50 Ω load (see Figure 18). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design and characterization.

Figure 27 provides the AC test load for TDO and the boundary-scan outputs of the MPC8347EA.

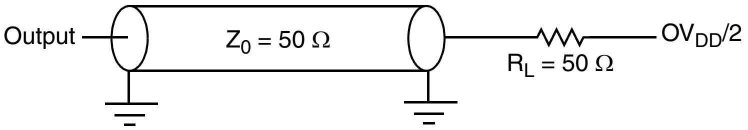
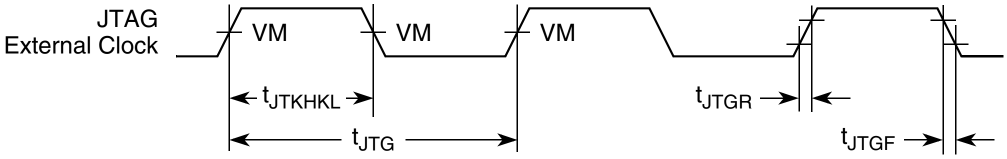


Figure 27. AC Test Load for the JTAG Interface

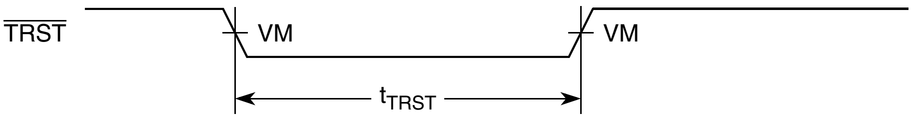
Figure 28 provides the JTAG clock input timing diagram.



VM = Midpoint Voltage ($OV_{DD}/2$)

Figure 28. JTAG Clock Input Timing Diagram

Figure 29 provides the $\overline{\text{TRST}}$ timing diagram.



VM = Midpoint Voltage ($OV_{DD}/2$)

Figure 29. $\overline{\text{TRST}}$ Timing Diagram

Figure 30 provides the boundary-scan timing diagram.

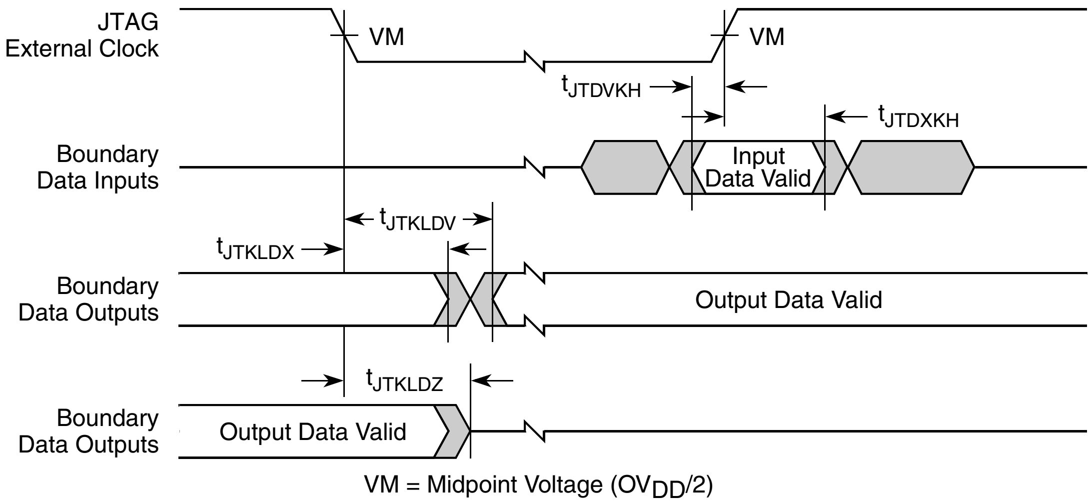


Figure 30. Boundary-Scan Timing Diagram

Figure 31 provides the test access port timing diagram.

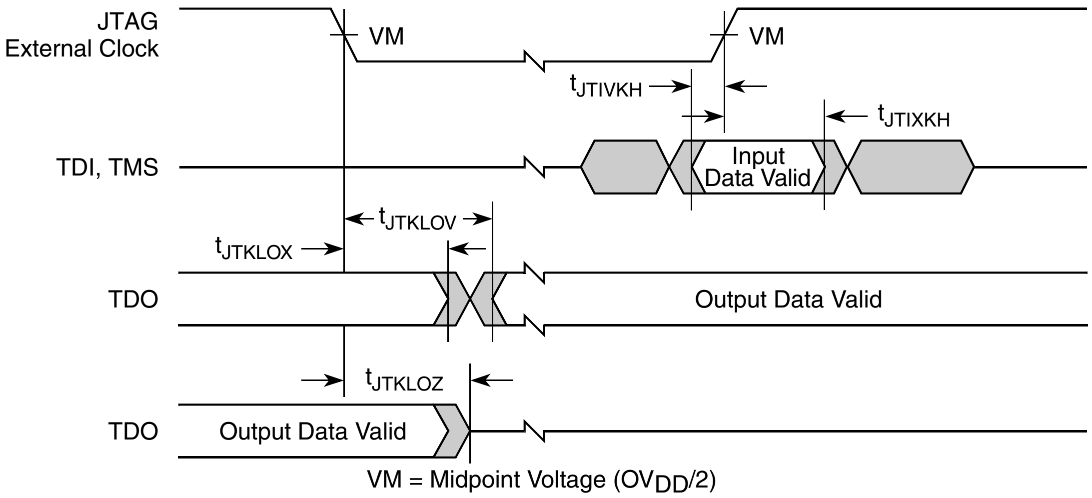


Figure 31. Test Access Port Timing Diagram

Table 43. I^{2}C AC Electrical Specifications (continued)

Parameter	Symbol[1]	Min	Max	Unit
Fall time of both SDA and SCL signals[5]	t_{I2CF}	—	300	ns
Setup time for STOP condition	t_{I2PVKH}	0.6	—	μs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V

Notes:

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I^{2}C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I^{2}C timing (I2) for the time that the data with respect to the start condition (S) goes invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I^{2}C timing (I2) for the time that the data with respect to the stop condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. The device provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKH} must be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.
5.)The device does not follow the "I2C-BUS Specifications" version 2.1 regarding the tI2CF AC parameter.

Figure 32 provides the AC test load for the I^{2}C.

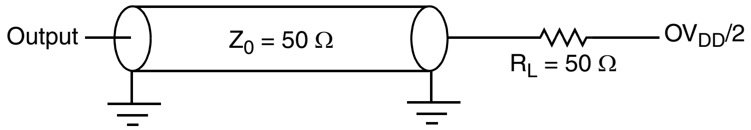


Figure 32. I^{2}C AC Test Load

Figure 33 shows the AC timing diagram for the I^{2}C bus.

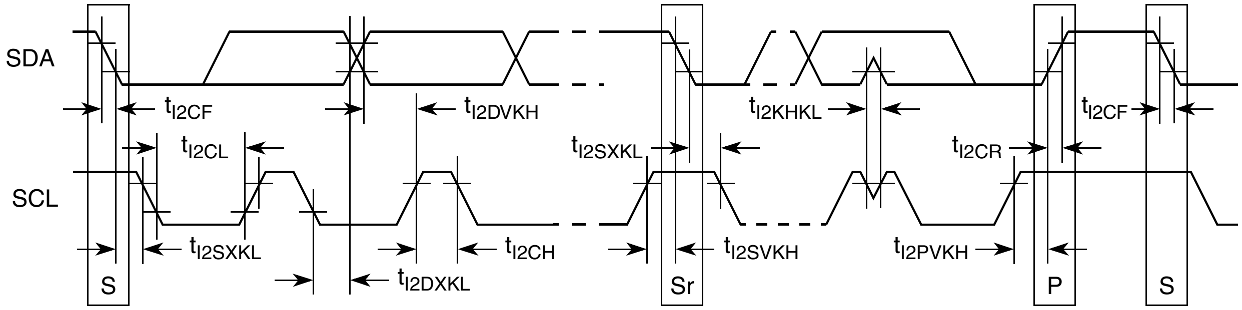


Figure 33. I^{2}C Bus AC Timing Diagram

Table 53. SPI DC Electrical Characteristics (continued)

Parameter	Symbol	Condition	Min	Max	Unit
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	$I_{OH} = -8.0$ mA	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0$ mA	—	0.5	V
Output low voltage	V_{OL}	$I_{OL} = 3.2$ mA	—	0.4	V

17.2 SPI AC Timing Specifications

Table 54 provides the SPI input and output AC timing specifications.

Table 54. SPI AC Timing Specifications[1]

Parameter	Symbol[2]	Min	Max	Unit
SPI outputs valid—Master mode (internal clock) delay	t_{NIKHOV}	—	6	ns
SPI outputs hold—Master mode (internal clock) delay	t_{NIKHOX}	0.5	—	ns
SPI outputs valid—Slave mode (external clock) delay	t_{NEKHOV}	—	8	ns
SPI outputs hold—Slave mode (external clock) delay	t_{NEKHOX}	2	—	ns
SPI inputs—Master mode (internal clock input setup time	t_{NIIVKH}	4	—	ns
SPI inputs—Master mode (internal clock input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:

1. Output specifications are measured from the 50 percent level of the rising edge of CLKIN to the 50 percent level of the signal. Timings are measured at the pin.
2. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).

Figure 37 provides the AC test load for the SPI.

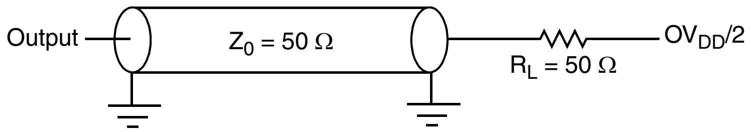


Figure 37. SPI AC Test Load

Table 55. MPC8347EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LALE	AK24	O	OV_{DD}	—
LGPL0/LSDA10/cfg_reset_source0	AP27	I/O	OV_{DD}	—
LGPL1/LSDWE/cfg_reset_source1	AL25	I/O	OV_{DD}	—
LGPL2/LSDRAS/LOE	AJ24	O	OV_{DD}	—
LGPL3/LSDCAS/cfg_reset_source2	AN27	I/O	OV_{DD}	—
LGPL4/LGTA/LUPWAIT/LPBSE	AP28	I/O	OV_{DD}	13
LGPL5/cfg_clkin_div	AL26	I/O	OV_{DD}	—
LCKE	AM27	O	OV_{DD}	—
LCLK[0:2]	AN28, AK26, AP29	O	OV_{DD}	—
LSYNC_OUT	AM12	O	OV_{DD}	—
LSYNC_IN	AJ10	I	OV_{DD}	—
General Purpose I/O Timers				
GPIO1[0]/DMA_DREQ0/GTM1_TIN1/ GTM2_TIN2	F24	I/O	OV_{DD}	—
GPIO1[1]/DMA_DACK0/GTM1_TGATE1/ GTM2_TGATE2	E24	I/O	OV_{DD}	—
GPIO1[2]/DMA_DDONE0/GTM1_TOUT1	B25	I/O	OV_{DD}	—
GPIO1[3]/DMA_DREQ1/GTM1_TIN2/ GTM2_TIN1	D24	I/O	OV_{DD}	—
GPIO1[4]/DMA_DACK1/GTM1_TGATE2/ GTM2_TGATE1	A25	I/O	OV_{DD}	—
GPIO1[5]/DMA_DDONE1/GTM1_TOUT2/ GTM2_TOUT1	B24	I/O	OV_{DD}	—
GPIO1[6]/DMA_DREQ2/GTM1_TIN3/ GTM2_TIN4	A24	I/O	OV_{DD}	—
GPIO1[7]/DMA_DACK2/GTM1_TGATE3/ GTM2_TGATE4	D23	I/O	OV_{DD}	—
GPIO1[8]/DMA_DDONE2/GTM1_TOUT3	B23	I/O	OV_{DD}	—
GPIO1[9]/DMA_DREQ3/GTM1_TIN4/ GTM2_TIN3	A23	I/O	OV_{DD}	—
GPIO1[10]/DMA_DACK3/GTM1_TGATE4/ GTM2_TGATE3	F22	I/O	OV_{DD}	—
GPIO1[11]/DMA_DDONE3/GTM1_TOUT4/ GTM2_TOUT3	E22	I/O	OV_{DD}	—
USB Port 1				
MPH1_D0_ENABLEN/DR_D0_ENABLEN	A26	I/O	OV_{DD}	—
MPH1_D1_SER_TXD/DR_D1_SER_TXD	B26	I/O	OV_{DD}	—
MPH1_D2_VMO_SE0/DR_D2_VMO_SE0	D25	I/O	OV_{DD}	—

Table 56. MPC8347EA (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
General Purpose I/O Timers				
GPIO1[0]/DMA_DREQ0/GTM1_TIN1/ GTM2_TIN2	D27	I/O	OV_{DD}	—
GPIO1[1]/DMA_DACK0/GTM1_TGATE1/ GTM2_TGATE2	E26	I/O	OV_{DD}	—
GPIO1[2]/DMA_DDONE0/GTM1_TOUT1	D28	I/O	OV_{DD}	—
GPIO1[3]/DMA_DREQ1/GTM1_TIN2/ GTM2_TIN1	G25	I/O	OV_{DD}	—
GPIO1[4]/DMA_DACK1/GTM1_TGATE2/ GTM2_TGATE1	J24	I/O	OV_{DD}	—
GPIO1[5]/DMA_DDONE1/GTM1_TOUT2/ GTM2_TOUT1	F26	I/O	OV_{DD}	—
GPIO1[6]/DMA_DREQ2/GTM1_TIN3/ GTM2_TIN4	E27	I/O	OV_{DD}	—
GPIO1[7]/DMA_DACK2/GTM1_TGATE3/ GTM2_TGATE4	E28	I/O	OV_{DD}	—
GPIO1[8]/DMA_DDONE2/GTM1_TOUT3	H25	I/O	OV_{DD}	—
GPIO1[9]/DMA_DREQ3/GTM1_TIN4/ GTM2_TIN3	F27	I/O	OV_{DD}	—
GPIO1[10]/DMA_DACK3/ GTM1_TGATE4/GTM2_TGATE3	K24	I/O	OV_{DD}	—
GPIO1[11]/DMA_DDONE3/ GTM1_TOUT4/GTM2_TOUT3	G26	I/O	OV_{DD}	—
USB Port 1				
MPH1_D0_ENABLEN/DR_D0_ENABLEN	C28	I/O	OV_{DD}	—
MPH1_D1_SER_TXD/DR_D1_SER_TXD	F25	I/O	OV_{DD}	—
MPH1_D2_VMO_SE0/DR_D2_VMO_SE0	B28	I/O	OV_{DD}	—
MPH1_D3_SPEED/DR_D3_SPEED	C27	I/O	OV_{DD}	—
MPH1_D4_DP/DR_D4_DP	D26	I/O	OV_{DD}	—
MPH1_D5_DM/DR_D5_DM	E25	I/O	OV_{DD}	—
MPH1_D6_SER_RCV/DR_D6_SER_RCV	C26	I/O	OV_{DD}	—
MPH1_D7_DRVVBUS/DR_D7_DRVVBUS	D25	I/O	OV_{DD}	—
MPH1_NXT/DR_SESS_VLD_NXT	B26	I	OV_{DD}	—
MPH1_DIR_DPPULLUP/ DR_XCVR_SEL_DPPULLUP	E24	I/O	OV_{DD}	—
MPH1_STP_SUSPEND/ DR_STP_SUSPEND	A27	O	OV_{DD}	—
MPH1_PWRFAULT/ DR_RX_ERROR_PWRFAULT	C25	I	OV_{DD}	—

Table 56. MPC8347EA (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MPH1_PCTL0/DR_TX_VALID_PCTL0	A26	O	OV_{DD}	—
MPH1_PCTL1/DR_TX_VALIDH_PCTL1	B25	O	OV_{DD}	—
MPH1_CLK/DR_CLK	A25	I	OV_{DD}	—
USB Port 0				
MPH0_D0_ENABLEN/DR_D8_CHGVBUS	D24	I/O	OV_{DD}	—
MPH0_D1_SER_TXD/DR_D9_DCHGVBUS	C24	I/O	OV_{DD}	—
MPH0_D2_VMO_SE0/DR_D10_DPPD	B24	I/O	OV_{DD}	—
MPH0_D3_SPEED/DR_D11_DMMD	A24	I/O	OV_{DD}	—
MPH0_D4_DP/DR_D12_VBUS_VLD	D23	I/O	OV_{DD}	—
MPH0_D5_DM/DR_D13_SESS_END	C23	I/O	OV_{DD}	—
MPH0_D6_SER_RCV/DR_D14	B23	I/O	OV_{DD}	—
MPH0_D7_DRVVBUS/DR_D15_IDPULLUP	A23	I/O	OV_{DD}	—
MPH0_NXT/DR_RX_ACTIVE_ID	D22	I	OV_{DD}	—
MPH0_DIR_DPPULLUP/DR_RESET	C22	I/O	OV_{DD}	—
MPH0_STP_SUSPEND/DR_TX_READY	B22	I/O	OV_{DD}	—
MPH0_PWRFAULT/DR_RX_VALIDH	A22	I	OV_{DD}	—
MPH0_PCTL0/DR_LINE_STATE0	E21	I/O	OV_{DD}	—
MPH0_PCTL1/DR_LINE_STATE1	D21	I/O	OV_{DD}	—
MPH0_CLK/DR_RX_VALID	C21	I	OV_{DD}	—
Programmable Interrupt Controller				
$\overline{\text{MCP\_OUT}}$	E8	O	OV_{DD}	2
$\overline{\text{IRQ0}}$/$\overline{\text{MCP\_IN}}$/GPIO2[12]	J28	I/O	OV_{DD}	—
$\overline{\text{IRQ}}$[1:5]/GPIO2[13:17]	K25, J25, H26, L24, G27	I/O	OV_{DD}	—
$\overline{\text{IRQ}}$[6]/GPIO2[18]/CKSTOP_OUT	G28	I/O	OV_{DD}	—
$\overline{\text{IRQ}}$[7]/GPIO2[19]/CKSTOP_IN	J26	I/O	OV_{DD}	—
Ethernet Management Interface				
EC_MDC	Y24	O	LV_{DD1}	—
EC_MDIO	Y25	I/O	LV_{DD1}	11
Gigabit Reference Clock				
EC_GTX_CLK125	Y26	I	LV_{DD1}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_COL/GPIO2[20]	M26	I/O	OV_{DD}	—
TSEC1_CRS/GPIO2[21]	U25	I/O	LV_{DD1}	—
TSEC1_GTX_CLK	V24	O	LV_{DD1}	3

19.3 Suggested PLL Configurations

Table 64 shows suggested PLL configurations for 33 and 66 MHz input clocks.

Table 64. Suggested PLL Configurations

Ref No.[1]	RCWL		400 MHz Device			533 MHz Device			667 MHz Device		
	SPMF	CORE PLL	Input Clock Freq (MHz)[2]	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz)[2]	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz)[2]	CSB Freq (MHz)	Core Freq (MHz)
33 MHz CLKIN/PCI_CLK Options											
922	**1001**	**0100010**	—	—	—	—	—	f300	33	300	300
723	**0111**	**0100011**	33	233	350	33	233	350	33	233	350
604	**0110**	**0000100**	33	200	400	33	200	400	33	200	400
624	**0110**	**0100100**	33	200	400	33	200	400	33	200	400
803	**1000**	**0000011**	33	266	400	33	266	400	33	266	400
823	**1000**	**0100011**	33	266	400	33	266	400	33	266	400
903	**1001**	**0000011**	—			33	300	450	33	300	450
923	**1001**	**0100011**	—			33	300	450	33	300	450
704	**0111**	**0000011**	—			33	233	466	33	233	466
724	**0111**	**0100011**	—			33	233	466	33	233	466
A03	1010	0000011	—			33	333	500	33	333	500
804	**1000**	**0000100**	—			33	266	533	33	266	533
705	**0111**	**0000101**	—			—			33	233	583
606	**0110**	**0000110**	—			—			33	200	600
904	**1001**	**0000100**	—			—			33	300	600
805	**1000**	**0000101**	—			—			33	266	667
A04	**1010**	**0000100**	—			—			33	333	667
66 MHz CLKIN/PCI_CLK Options											
304	**0011**	**0000100**	66	200	400	66	200	400	66	200	400
324	**0011**	**0100100**	66	200	400	66	200	400	66	200	400
403	**0100**	**0000011**	66	266	400	66	266	400	66	266	400
423	**0100**	**0100011**	66	266	400	66	266	400	66	266	400
305	**0011**	**0000101**	—			66	200	500	66	200	500
503	0101	0000011	—			66	333	500	66	333	500
404	**0100**	**0000100**	—			66	266	533	66	266	533

20.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature and a measure of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per the JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

20.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

Some application environments require a heat sink to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

The thermal performance of devices with heat sinks has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following list:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech 408-567-8082
473 Sapena Ct. #12
Santa Clara, CA 95054
Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

Millennium Electronics (MEI) 408-436-8770
Loroco Sites
671 East Brokaw Road
San Jose, CA 95112
Internet: www.mei-thermal.com

Tyco Electronics 800-522-2800
Chip Coolers™
P.O. Box 3668
Harrisburg, PA 17105-3668
Internet: www.chipcoolers.com

Wakefield Engineering 603-635-5102
33 Bridge St.
Pelham, NH 03076
Internet: www.wakefield.com

Interface material vendors include the following:

Chomerics, Inc. 781-935-4850
77 Dragon Ct.
Woburn, MA 01801
Internet: www.chomerics.com

Dow-Corning Corporation 800-248-2481
Dow-Corning Electronic Materials
P.O. Box 994
Midland, MI 48686-0997
Internet: www.dowcorning.com