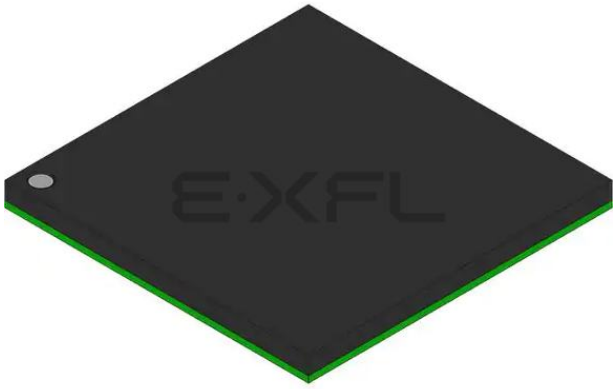

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Multimedia; VFP
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad, KPP, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Secure Fusebox, Secure JTAG
Package / Case	400-LFBGA
Supplier Device Package	400-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx351avm4b

The ball map for silicon revision 2.1 is different than the ballmap for silicon revision 2.0. The layout for each revision is not compatible, so it is important that the correct ballmap be used to implement the layout. See Section 5, “Package Information and Pinout.”

Table 2 shows the functional differences between the different parts in the i.MX35 family.

Table 2. Functional Differences in the i.MX35 Parts

Module	MCIMX351	MCIMX353	MCIMX355	MCIMX356	MCIMX357
I2C (3)	Yes	Yes	Yes	Yes	Yes
CSPI (2)	Yes	Yes	Yes	Yes	Yes
SSI/I2S (2)	Yes	Yes	Yes	Yes	Yes
ESAI	Yes	Yes	Yes	Yes	Yes
SPDIF I/O	Yes	Yes	Yes	Yes	Yes
USB HS Host	Yes	Yes	Yes	Yes	Yes
USB OTG	Yes	Yes	Yes	Yes	Yes
FlexCAN (2)	Yes	Yes	Yes	Yes	Yes
MLB	Yes	Yes	Yes	Yes	Yes
Ethernet	Yes	Yes	Yes	Yes	Yes
1-Wire	Yes	Yes	Yes	Yes	Yes
KPP	Yes	Yes	Yes	Yes	Yes
SDIO/MMC (2)	Yes	Yes	Yes	Yes	Yes
SDIO/Memory Stick	Yes	Yes	Yes	Yes	Yes
External Memory Controller (EMC)	Yes	Yes	Yes	Yes	Yes
JTAG	Yes	Yes	Yes	Yes	Yes
PATA	—	Yes	Yes	Yes	Yes
CE-ATA	—	Yes	Yes	Yes	Yes
Image Processing Unit (IPU) (inversion and rotation, pre- and post-processing, camera interface, blending, display controller)	—	Yes	Yes	Yes	Yes
Open VG graphics acceleration (GPU)	—	Yes	—	Yes	Yes

Table 4. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Domain[1]	Subsystem	Brief Description
ESAI	Enhanced serial audio interface	SDMA	Connectivity peripherals	The enhanced serial audio interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other DSPs. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator.
eSDHCv2 (3)	Enhanced secure digital host controller	ARM	Connectivity peripherals	The eSDHCv2 consists of four main modules: CE-ATA, MMC, SD and SDIO. CE-ATA is a hard drive interface that is optimized for embedded applications of storage. The MultiMediaCard (MMC) is a universal, low-cost, data storage and communication media to applications such as electronic toys, organizers, PDAs, and smart phones. The secure digital (SD) card is an evolution of MMC and is specifically designed to meet the security, capacity, performance, and environment requirements inherent in emerging audio and video consumer electronic devices. SD cards are categorized into Memory and I/O. A memory card enables a copyright protection mechanism that complies with the SDMI security standard. SDIO cards provide high-speed data I/O (such as wireless LAN via SDIO interface) with low power consumption. **Note:** CE-ATA is not available for the MCIMX351.
FEC	Ethernet	SDMA	Connectivity peripherals	The Ethernet media access controller (MAC) is designed to support both 10 and 100 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media
GPIO(3)	General purpose I/O modules	ARM	Pins	Used for general purpose input/output to external ICs. Each GPIO module supports 32 bits of I/O.
GPT	General purpose timers	ARM	Timer peripherals	Each GPT is a 32-bit free-running or set-and-forget mode timer with a programmable prescaler and compare and capture registers. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in set-and-forget mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU2D	Graphics processing unit 2Dv1	ARM	Multimedia peripherals	This module accelerates OpenVG and GDI graphics. **Note:** Not available for the MCIMX351.

4.1.2 Interface Frequency Limits

Table 9 provides information on interface frequency limits.

Table 9. Interface Frequency

ID	Parameter	Symbol	Min.	Typ.	Max.	Units
1	JTAG TCK Frequency	f_{JTAG}	DC	5	10	MHz

4.2 Power Modes

Table 10 provides descriptions of the power modes of the i.MX35 processor.

Table 10. i.MX35 Power Modes

Power Mode	Description	QVCC (ARM/L2 Peripheral)		MVDD/PVDD		OSC24M_VDD OSC_AUDO_VDD	
		Typ.	Max.	Typ.	Max.	Typ.	Max.
Wait	VDD1,2,3,4 = 1.1 V (min.) ARM is in wait for interrupt mode. MAX is active. L2 cache is kept powered. MCU PLL is on (400 MHz) PER PLL is off (can be configured) (default: 300 MHz) Module clocks are gated off (can be configured by CGR register). OSC 24M is ON. OSC audio is off (can be configured). RNGC internal osc is off.	16 mA	170 mA	7.2 mA	14 mA	1.2 mA	3 mA
Doze	VDD1,2,3,4 = 1.1 V (min.) ARM is in wait for interrupt mode. MAX is halted. L2 cache is kept powered. L2 cache control logic off. AWB enabled. MCU PLL is on(400 MHz) PER PLL is off (can be configured). (300 Mhz). Module clocks are gated off (can be configured by CGR register). OSC 24M is ON. OSC audio is off (can be configured) RNGC internal osc is off	12.4 mA	105 mA	7.2 mA	14 mA	1.2 mA	3 mA

NOTE

Deviation from these sequences may also result in one or more of the following:

- Excessive current during power-up phase
- Prevent the device from booting
- Programming of unprogrammed fuses

4.3.1 Powering Up

The power-up sequence should be completed as follows:

1. Assert Power on Reset ($\overline{\text{POR}}$).
2. Turn on digital logic domain and IO power supply: VDD*n*, NVCC*x*
3. Wait until VDD*n* and NVCC*x* power supplies are stable + 32 µs.
4. Turn on all other power supplies: PHY1_VDDA, USBPHY1_VDDA_BIAS, PHY2_VDD, USBPHY1_UPLLVDD, OSC24M_VDD, OSC_AUDIO_VDD, MVDD, PVDD, FUSEVDD. (Always FUSE_VDD should be connected to ground, except when eFuses are to be programmed.)
5. Wait until PHY1_VDDA, USBPHY1_VDDA_BIAS, PHY2_VDD, USBPHY1_UPLLVDD, OSC24M_VDD, OSC_AUDIO_VDD, MVDD, PVDD, (FUSEVDD, optional). Power supplies are stable + 100 µs.
6. Deassert the $\overline{\text{POR}}$ signal.

Table 11. Power Consumption

Power Supply	Voltage (V)	Max Current (mA)
QVCC	1.47	400
MVDD, PVDD	1.65	20
NVCC_EMI1, NVCC_EMI2, NVCC_EMI3, NVCC_LCDC, NVCC_NFC	1.9	90
FUSE_VDD[1]	3.6	62
NVCC_MISC, NVCC_CSI, NVCC_SDIO, NVCC_CRM, NVCC_ATA, NVCC_MLB, NVCC_JTAG	3.6	60
OSC24M_VDD, OSC_AUDIO_VDD, PHY1_VDDA, PHY2_VDD, USBPHY1_UPLLVDD, USBPHY1_VDDA_BIAS	3.6	25

1 This rail is connected to ground; it only needs a voltage if eFuses are to be programmed. FUSE_VDD should be supplied by following the power up sequence given in Section 4.3.1, “Powering Up.”

The method for obtaining max current is as follows:

1. Measure worst case power consumption on individual rails using directed test on i.MX35.
2. Correlate worst case power consumption power measurements with worst case power consumption simulations.
3. Combine common voltage rails based on power supply sequencing requirements
4. Guard band worst case numbers for temperature and process variation. Guard band is based on process data and correlated with actual data measured on i.MX35.
5. The sum of individual rails is greater than real world power consumption, as a real system does not typically maximize power consumption on all peripherals simultaneously.

4.6 Thermal Characteristics

The thermal resistance characteristics for the device are given in Table 12. These values were measured under the following conditions:

- Two-layer substrate
- Substrate solder mask thickness: 0.025 mm
- Substrate metal thicknesses: 0.016 mm
- Substrate core thickness: 0.200 mm
- Core via I.D: 0.168 mm, Core via plating 0.016 mm.
- Full array map design, but nearly all balls under die are power or ground.
- Die Attach: 0.033 mm non-conductive die attach, k = 0.3 W/m K
- Mold compound: k = 0.9 W/m K

Table 12. Thermal Resistance Data

Rating	Condition	Symbol	Value	Unit
Junction to ambient[1] natural convection	Single layer board (1s)	$R_{\theta JA}$	53	ºC/W
Junction to ambient[1] natural convection	Four layer board (2s2p)	$R_{\theta JA}$	30	ºC/W

Table 14 shows the DC electrical characteristics for GPIO, DDR2, mobile DDR, and SDRAM pins. The term NVCC refers to the power supply voltage that feeds the I/O of the module in question. For example, NVCC for the SD/MMC interface refers to NVCC_SDIO.

Table 14. I/O Pin DC Electrical Characteristics

Pin	DC Electrical Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
GPIO	High-level output voltage	Voh	Ioh = –1 mA Ioh = specified drive	NVCC – 0.15 0.8 × NVCC	—	—	V
	Low-level output voltage	Vol	Iol = 1 mA Iol = specified drive	—	—	0.15 0.2 × NVCC	V
	High-level output current for slow mode (Voh = 0.8 × NVCC)	Ioh	Standard drive High drive Max. drive	–2.0 –4.0 –8.0	—	—	mA
	High-level output current for fast mode (Voh = 0.8 × NVCC)	Ioh	Standard drive High drive Max. drive	–4.0 –6.0 –8.0	—	—	mA
	Low-level output current for slow mode (Voh = 0.2 × NVCC)	Iol	Standard drive High drive Max. drive	2.0 4.0 8.0	—	—	mA
	Low-level output current for fast mode (Voh = 0.2 × NVCC)	Iol	Standard drive High drive Max. drive	4.0 6.0 8.0	—	—	mA
	High-level DC Input Voltage with 1.8 V, 3.3 V NVCC (for digital cells in input mode)	VIH	—	0.7 × NVCC	—	NVCC	V
	Low-level DC Input Voltage with 1.8 V, 3.3 V NVCC (for digital cells in input mode	VIL	—	–0.3 V	—	0.3 × NVCC	V
	Input Hysteresis	VHYS	OVDD = 3.3 V OVDD = 1.8 V	—	410 330	—	mV
	Schmitt trigger VT+	VT+	—	0.5 × NVCC	—		V
	Schmitt trigger VT–	VT–	—	—	—	0.5 × NVCC	V
	Pull-up resistor (22 kΩ PU)	Rpu	Vi = 0	—	22	—	kΩ
	Pull-up resistor (47 kΩ PU)	Rpu	Vi = 0	—	47	—	kΩ
	Pull-up resistor (100 kΩ PU)	Rpu	Vi = 0	—	100	—	kΩ
	Pull-down resistor (100 kΩ PD)	Rpd	Vi = NVCC	—	100	—	kΩ
	External resistance to pull keeper up when enabled	Rkpu	Ipu > 620 μA @ min Vddio = 3.0 V	—	—	4.8	kΩ
	External resistance to pull keeper down when enabled	Rkpd	Ipu > 510 μA @min Vddio = 3.0 V	—	—	5.9	kΩ

4.9.4 Embedded Trace Macrocell (ETM) Electrical Specifications

ETM is an ARM protocol. The timing specifications in this section are given as a guide for a test point access (TPA) that supports TRACECLK frequencies up to 133 MHz.

Figure 9 depicts the TRACECLK timings of ETM, and Table 30 lists the timing parameters.

Figure 9. ETM TRACECLK Timing Diagram

Table 30. ETM TRACECLK Timing Parameters

ID	Parameter	Min.	Max.	Unit
T_{cyc}	Clock period	Frequency dependent	—	ns
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	—	3	ns
T_f	Clock and data fall time	—	3	ns

Figure 10 depicts the setup and hold requirements of the trace data pins with respect to TRACECLK, and Table 31 lists the timing parameters.

Figure 10. Trace Data Timing Diagram

Table 31. ETM Trace Data Timing Parameters

ID	Parameter	Min.	Max.	Unit
T_s	Data setup	2	—	ns
T_h	Data hold	1	—	ns

4.9.4.1 Half-Rate Clocking Mode

When half-rate clocking is used, the trace data signals are sampled by the TPA on both the rising and falling edges of TRACECLK, where TRACECLK is half the frequency of the clock shown in Figure 10. The same T_s and T_h parameters from Table 31 still apply with respect to the falling edge of the TRACECLK signal.

Table 46. Enhanced Serial Audio Interface Timing (continued)

No.	Characteristics[1,2]	Symbol	Expression[2]	Min.	Max.	Condition[3]	Unit
80	SCKT rising edge to FST out (wr) high[5]	— —	— —	— —	20.0 10.0	x ck i ck	ns
81	SCKT rising edge to FST out (wr) low[5]	— —	— —	— —	22.0 12.0	x ck i ck	ns
82	SCKT rising edge to FST out (wl) high	— —	— —	— —	19.0 9.0	x ck i ck	ns
83	SCKT rising edge to FST out (wl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
84	SCKT rising edge to data out enable from high impedance	— —	— —	— —	22.0 17.0	x ck i ck	ns
86	SCKT rising edge to data out valid	— —	— —	— —	18.0 13.0	x ck i ck	ns
87	SCKT rising edge to data out high impedance [67]	— —	— —	— —	21.0 16.0	x ck i ck	ns
89	FST input (bl, wr) setup time before SCKT falling edge[5]	— —	— —	2.0 18.0	— —	x ck i ck	ns
90	FST input (wl) setup time before SCKT falling edge	— —	— —	2.0 18.0	— —	x ck i ck	ns
91	FST input hold time after SCKT falling edge	— —	— —	4.0 5.0	— —	x ck i ck	ns

1 i ck = internal clock
x ck = external clock
i ck a = internal clock, asynchronous mode
(asynchronous implies that SCKT and SCKR are two different clocks)
i ck s = internal clock, synchronous mode
(synchronous implies that SCKT and SCKR are the same clock)

2 bl = bit length
wl = word length
wr = word length relative

3 SCKT(SCKT pin) = transmit clock
SCKR(SCKR pin) = receive clock
FST(FST pin) = transmit frame sync
FSR(FSR pin) = receive frame sync
HCKT(HCKT pin) = transmit high frequency clock
HCKR(HCKR pin) = receive high frequency clock

4 For the internal clock, the external clock cycle is defined by Icyc and the ESAI control register.

5 The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but it spreads from one serial clock before the first bit clock (like the bit length frame sync signal), until the second-to-last bit clock of the first word in the frame.

6 Periodically sampled and not 100% tested.

4.9.8 Fast Ethernet Controller (FEC) AC Electrical Specifications

This section describes the electrical information of the FEC module. The FEC is designed to support both 10- and 100-Mbps Ethernet networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The FEC supports the 10/100 Mbps Media Independent Interface (MII) using a total of 18 pins. The 10-Mbps 7-wire interface that is restricted to a 10-Mbps data rate uses seven of the MII pins for connection to an external Ethernet transceiver.

4.9.8.1 FEC AC Timing

This section describes the AC timing specifications of the FEC. The MII signals are compatible with transceivers operating at a voltage of 3.3 V.

4.9.8.2 MII Receive Signal Timing

The MII receive timing signals consist of FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER, and FEC_RX_CLK. The receiver functions correctly up to a FEC_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the FEC_RX_CLK frequency. Table 48 lists MII receive channel timings.

Table 48. MII Receive Signal Timing

Num.	Characteristic[1]	Min.	Max.	Unit
M1	FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER to FEC_RX_CLK setup	5	—	ns
M2	FEC_RX_CLK to FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER hold	5	—	ns
M3	FEC_RX_CLK pulse width high	35%	65%	FEC_RX_CLK period
M4	FEC_RX_CLK pulse width low	35%	65%	FEC_RX_CLK period

[1] FEC_RX_DV, FEC_RX_CLK, and FEC_RXD0 have the same timing when in 10 Mbps 7-wire interface mode.

Figure 39 shows the MII receive signal timings listed in Table 48.

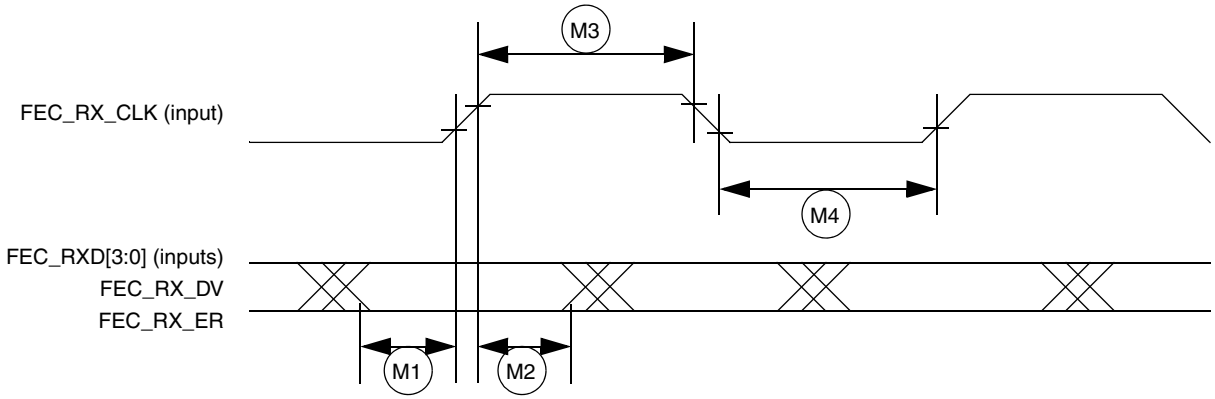

Figure 39. MII Receive Signal Timing Diagram

4.9.13.1 Synchronous Interfaces

This section discusses the interfaces to active matrix TFT LCD panels, Sharp HR-TFT, and dual-port smart displays.

4.9.13.1.4 Interface to Active Matrix TFT LCD Panels, Functional Description

Figure 47 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure, signals are shown with negative polarity. The sequence of events for active matrix interface timing is as follows:

- DISPB_D3_CLK latches data into the panel on its negative edge (when positive polarity is selected). In active mode, DISPB_D3_CLK runs continuously.
- DISPB_D3_HSYNC causes the panel to start a new line.
- DISPB_D3_VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse.
- DISPB_D3_DRDY acts like an output enable signal to the CRT display. This output enables the data to be shifted to the display. When disabled, the data is invalid and the trace is off.

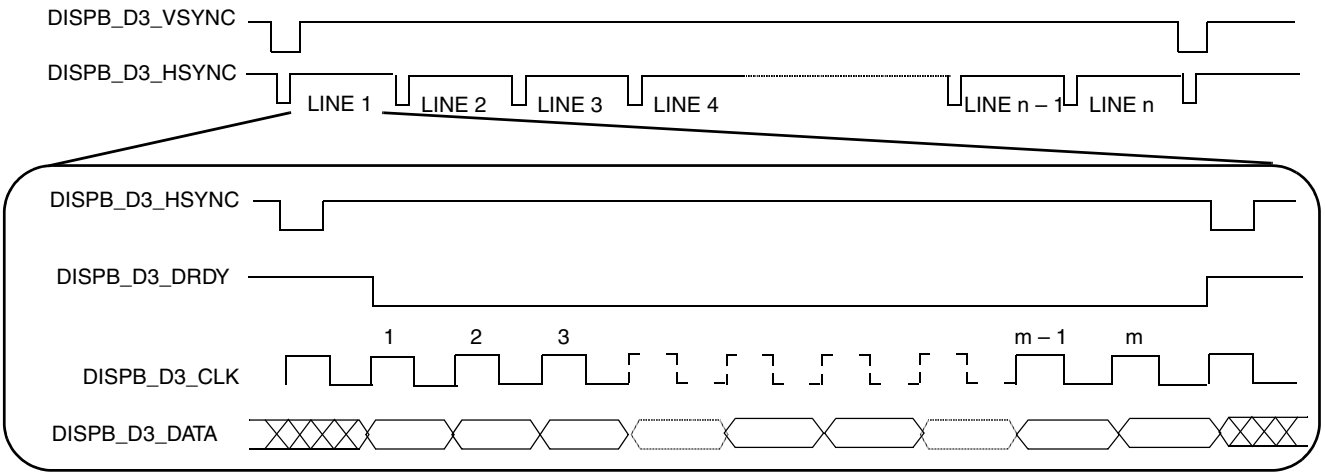

Figure 47. Interface Timing Diagram for TFT (Active Matrix) Panels

4.9.13.1.5 Interface to Active Matrix TFT LCD Panels, Electrical Characteristics

Figure 48 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and the data. All figure parameters shown are programmable. The timing images correspond to inverse polarity

Figure 64 depicts timing of the 5-wire serial interface (Type 1). For this interface, a separate RS line is added. When a burst is transmitted within a single active chip select interval, the RS can be changed at boundaries of words.

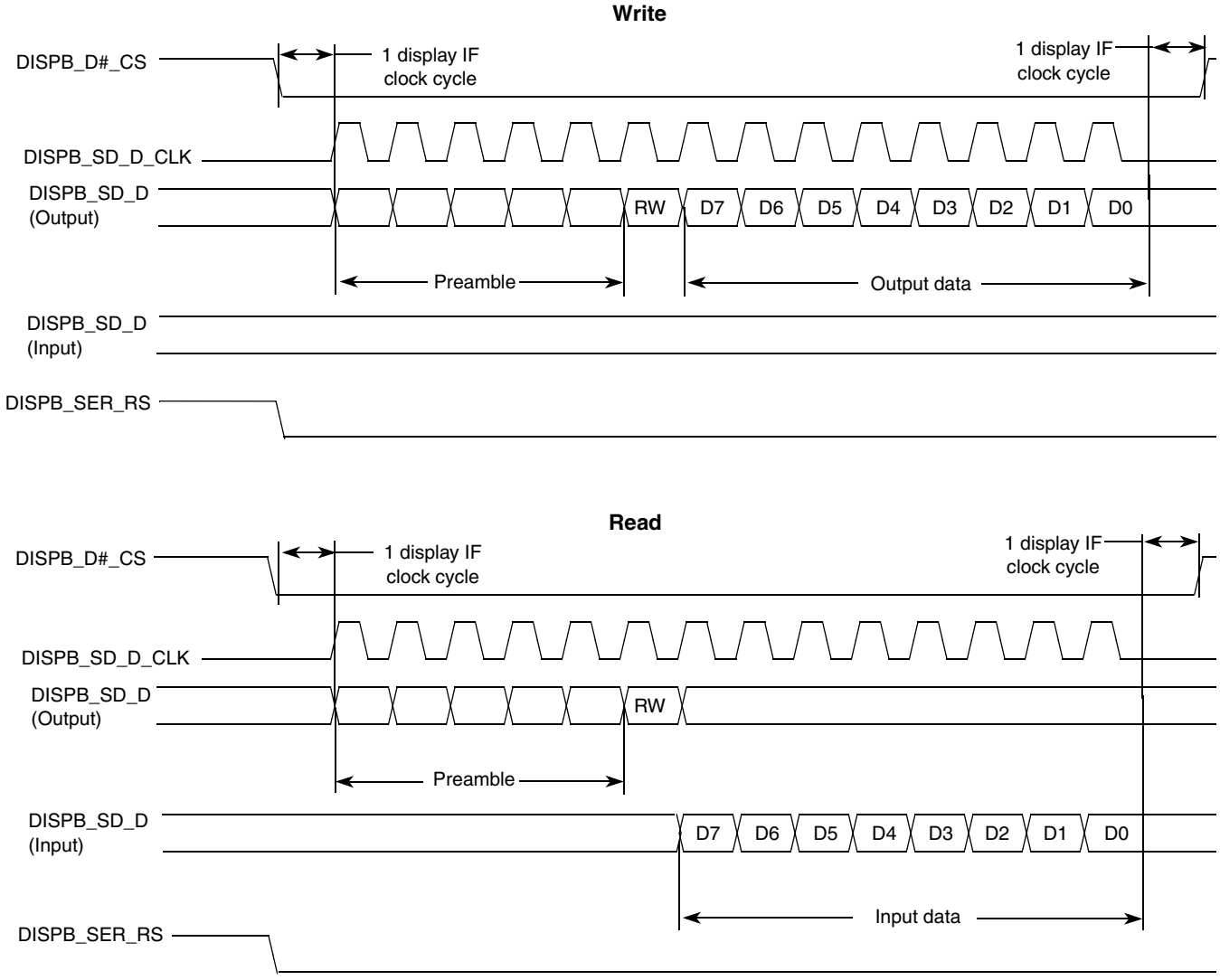

Figure 64. 5-Wire Serial Interface (Type 1) Timing Diagram

Table 60. Serial Interface Timing Parameters[1] (continued)

Signal	Parameter	Symbol	Standards		Unit
			Min.	Max.	
MSHC_DATA	Setup time	tDsu	5	—	ns
	Hold time	tDh	5	—	ns
	Output delay time	tDd	—	15	ns

1 Timing is guaranteed for NVCC from 2.7 V through 3.1 V and up to a maximum overdrive NVCC of 3.3 V. See NVCC restrictions described in Table 61.

Table 61. Parallel Interface Timing Parameters[1]

Signal	Parameter	Symbol	Standards		Unit
			Min.	Max.	
MSHC_SCLK	Cycle	tSCLKc	25	—	ns
	H pulse length	tSCLKwh	5	—	ns
	L pulse length	tSCLKwl	5	—	ns
	Rise time	tSCLKr	—	10	ns
	Fall time	tSCLKf	—	10	ns
MSHC_BS	Setup time	tBSsu	8	—	ns
	Hold time	tBSh	1	—	ns
MSHC_DATA	Setup time	tDsu	8	—	ns
	Hold time	tDh	1	—	ns
	Output delay time	tDd	—	15	ns

1 Timing is guaranteed for NVCC from 2.7 V through 3.1 V and up to a maximum overdrive NVCC of 3.3 V. See the NVCC restrictions described in Table 8.

4.9.15 MediaLB Controller Electrical Specifications

This section describes the electrical information of the MediaLB Controller module.

Table 62. MLB 256/512 Fs Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units	Comment
MLBCLK operating frequency[1]	f_{mck}	11.264	12.288 24.576	24.6272 25.600	MHz	Min: 256 × Fs at 44.0 kHz Typ: 256 × Fs at 48.0 kHz Typ: 512 × Fs at 48.0 kHz Max: 512 × Fs at 48.1 kHz Max: 512 × Fs PLL unlocked
MLBCLK rise time	t_{mckr}	—	—	3	ns	V_{IL} TO V_{IH}

4.9.17 Parallel ATA Module AC Electrical Specifications

The parallel ATA module can work on PIO/multiword DMA/ultra-DMA transfer modes (not available for the MCIMX351). Each transfer mode has a different data transfer rate, Ultra DMA mode 4 data transfer rate is up to 100 MBps.

The parallel ATA module interface consists of a total of 29 pins. Some pins have different functions in different transfer modes. There are various requirements for timing relationships among the function pins, in compliance with the ATA/ATAPI-6 specification, and these requirements are configurable by the ATA module registers.

4.9.17.1 General Timing Requirements

Table 67 and Figure 74 define the AC characteristics of the interface signals on all data transfer modes.

Table 67. AC Characteristics of All Interface Signals

ID	Parameter	Symbol	Min.	Max.	Unit
SI1	Rising edge slew rate for any signal on the ATA interface[1]	S_{rise}[1]	—	1.25	V/ns
SI2	Falling edge slew rate for any signal on the ATA interface[1]	S_{fall}[1]	—	1.25	V/ns
SI3	Host interface signal capacitance at the host connector	C_{host}	—	20	pF

[1] SRISE and SFALL meet this requirement when measured at the sender's connector from 10–90% of full signal amplitude with all capacitive loads from 15 pF through 40 pF, where all signals have the same capacitive load value.

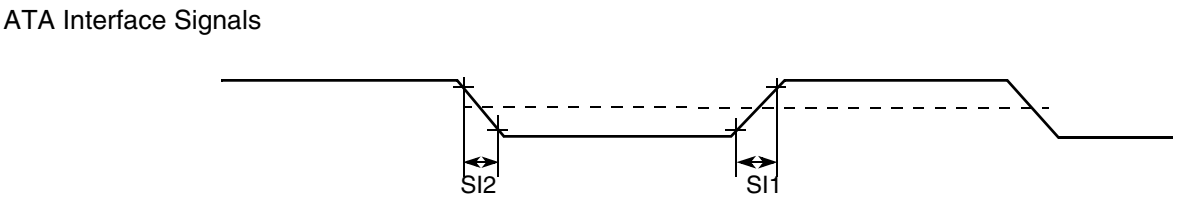

Figure 74. ATA Interface Signals Timing Diagram

4.9.17.2 ATA Electrical Specifications (ATA Bus, Bus Buffers)

This section discusses ATA parameters. For a detailed description, refer to the ATA-6 specification.

Level shifters are required for 3.3-V or 5.0-V compatibility on the ATA interface.

The use of bus buffers introduces delays on the bus and introduces skew between signal lines. These factors make it difficult to operate the bus at the highest speed (UDMA-5) when bus buffers are used. Use of bus buffers is not recommended if fast UDMA mode is required.

The ATA specification imposes a slew rate limit on the ATA bus. According to this limit, any signal driven on the bus should have a slew rate between 0.4 and 1.2 V/ns with a 40 pF load. Few vendors of bus buffers specify the slew rate of the outgoing signals.

When bus buffers are used the ata_data bus buffer is bidirectional, and uses the direction control signal ata_buffer_en. When ata_buffer_en is asserted, the bus should drive from host to device. When

Figure 81. UDMA-In Device Terminates Transfer Timing Diagram

Table 72. UDMA-In Burst Timing Parameters

ATA Parameter	Parameters from Figure 79, Figure 80, Figure 81	Description	Controlling Variable
tack	tack	tack (min.) = (time_ack × T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv (min.) = (time_env × T) – (tskew1 + tskew2) tenv (max.) = (time_env × T) + (tskew1 + tskew2)	time_env
tds	tds1	tds – (tskew3) – ti_ds > 0	tskew3, ti_ds, ti_dh should be low enough
tdh	tdh1	tdh – (tskew3) – ti_dh > 0	
tcyc	tc1	(tcyc – tskew > T	T big enough
trp	trp	trp (min.) = time_rp × T – (tskew1 + tskew2 + tskew6)	time_rp
—	tx1[1]	(time_rp × T) – (tco + tsu + 3T + 2 × tbuf + 2 × tcable2) > trfs (drive)	time_rp
tmli	tmli1	tmli1 (min.) = (time_mlix + 0.4) × T	time_mlix
tzah	tzah	tzah (min.) = (time_zah + 0.4) × T	time_zah
tdzfs	tdzfs	tdzfs = (time_dzfs × T) – (tskew1 + tskew2)	time_dzfs
tcvh	tcvh	tcvh = (time_cvh × T) – (tskew1 + tskew2)	time_cvh
—	ton toff	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

1 There is a special timing requirement in the ATA host that requires the internal DIOW to go high three clocks after the last active edge on the DSTROBE signal. The equation given on this line tries to capture this constraint.

2. Make ton and toff large enough to avoid bus contention.

Figure 84. UDMA-Out Device Terminates Transfer Timing Diagram

Table 73. UDMA-Out Burst Timing Parameters

ATA Parameter	Parameter from Figure 82, Figure 83, Figure 84	Value	Controlling Variable
tack	tack	tack (min.) = (time_ack × T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv (min.) = (time_env × T) – (tskew1 + tskew2) tenv (max.) = (time_env × T) + (tskew1 + tskew2)	time_env
tdvs	tdvs	tdvs = (time_dvs ×T) – (tskew1 + tskew2)	time_dvs
tdvh	tdvh	tdvs = (time_dvh × T) – (tskew1 + tskew2)	time_dvh
tcyc	tcyc	tcyc = time_cyc × T – (tskew1 + tskew2)	time_cyc
t2cyc	—	t2cyc = time_cyc × 2 × T	time_cyc
trfs1	trfs	trfs = 1.6 × T + tsui + tco + tbuf + tbuf	—
—	tdzfs	tdzfs = time_dzfs × T – (tskew1)	time_dzfs
tss	tss	tss = time_ss × T – (tskew1 + tskew2)	time_ss
tmli	tdzfs_mli	tdzfs_mli = max. (time_dzfs, time_mli) × T – (tskew1 + tskew2)	—
tli	tli1	tli1 > 0	—
tli	tli2	tli2 > 0	—
tli	tli3	tli3 > 0	—
tcvh	tcvh	tcvh = (time_cvh × T) – (tskew1 + tskew2)	time_cvh
—	ton toff	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

Table 91. USB Port Timing Specification in VP_VM Bidirectional Mode (continued)

No.	Parameter	Signal Name	Direction	Min.	Max.	Unit	Condition/ Reference Signal
US28	Rx skew	USB_DAT_VP	In	–4.0	+4.0	ns	USB_SE0_VM
US29	Rx skew	USB_RCV	In	–6.0	+2.0	ns	USB_DAT_VP

4.9.24.4 VP_VM Unidirectional Mode

Table 92 defines the signals for VP_VM unidirectional mode. Figure 106 and Figure 107 show the transmit and receive waveforms respectively.

Table 92. Signal Definitions—VP_VM Unidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out	Tx VP data when USB_TXOE_B is low
USB_SE0_VM	Out	Tx VM data when USB_TXOE_B is low
USB_VP1	In	Rx VP data when USB_TXOE_B is high
USB_VM1	In	Rx VM data when USB_TXOE_B is high
USB_RCV	In	Differential Rx data

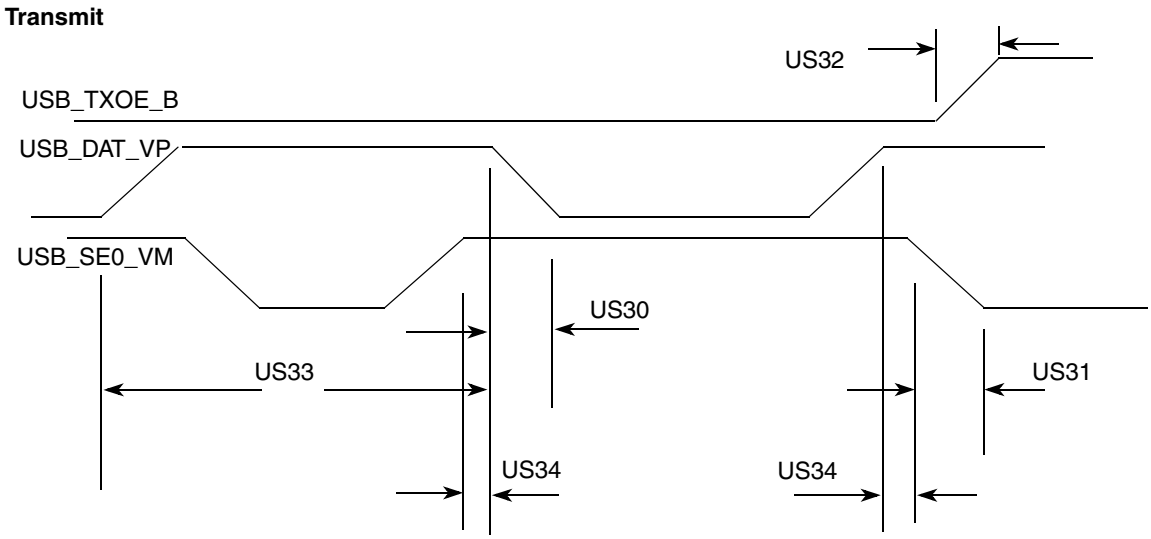

Figure 106. USB Transmit Waveform in VP_VM Unidirectional Mode

5 Package Information and Pinout

This section includes the following:

- Mechanical package drawing
- Pin/contact assignment information

5.1 MAPBGA Production Package 1568-01, 17 × 17 mm, 0.8 Pitch

See Figure 108 for the package drawing and dimensions of the production package.

Figure 108. Production Package: Mechanical Drawing

Table 95. Silicon Revision 2.1 Signal Ball Map Locations (continued)

Signal ID	Ball Location
CTS2	G5
D0	A2
D1	D4
D10	D2
D11	E6
D12	E3
D13	F5
D14	D1
D15	E2
D2	B2
D3	E5
D3_CLS	L17
D3_DRDY	L20
D3_FPSHIFT	L15
D3_HSYNC	L18
D3_REV	M17
D3_SPL	M18
D3_VSYNC	M19
D4	C3
D5	B1
D6	D3
D7	C2
D8	C1
D9	E4
DE_B	W19
DQM0	B19
SDCKE1	D17
DQM2	D16
DQM3	C18
EB0	F18
EB1	F16
ECB	D19
EXT_ARMCLK	V8
EXTAL_AUDIO	W20
EXTAL24M	T20
FEC_COL	P3
FEC_CRS	N5
FEC_MDC	R1
FEC_MDIO	P1
FEC_RDATA0	P2
FEC_RDATA1	N2
FEC_RDATA2	M3
FEC_RDATA3	N1
FEC_RX_CLK	R2
FEC_RX_DV	T2
FEC_RX_ERR	N3

Signal ID	Ball Location
FEC_TDATA0	P5
FEC_TDATA1	M4
FEC_TDATA2	M5
FEC_TDATA3	L6
FEC_TX_CLK	P4
FEC_TX_EN	T1
FEC_TX_ERR	N4
FSR	K5
FST	J1
FUSE_VDD	P13
FUSE_VSS	M11
GPIO1_0	T11
GPIO1_1	Y11
GPIO2_0	U11
GPIO3_0	V11
HCKR	K2
HCKT	J5
I2C1_CLK	M20
I2C1_DAT	N17
I2C2_CLK	L3
I2C2_DAT	M1
LBA	D20
LD0	F20
LD1	G18
LD10	H20
LD11	J18
LD12	J16
LD13	J19
LD14	J17
LD15	J20
LD16	K14
LD17	K19
LD18	K18
LD19	K20
LD2	G17
LD20	K16
LD21	K17
LD22	K15
LD23	L19
LD3	G16
LD4	G19
LD5	H16
LD6	H18
LD7	G20
LD8	H17
LD9	H19

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Japan
0120 191014 or
+81 3 5437 9125
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Asia/Pacific:
Freescale Semiconductor China Ltd.
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