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Understanding Embedded - Microprocessors

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	532MHz
Co-Processors/DSP	Multimedia; IPU, VFP
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad, KPP, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Secure Fusebox, Secure JTAG
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx355ajq5c

4 Electrical Characteristics

The following sections provide the device-level and module-level electrical characteristics for the i.MX35 processor.

4.1 i.MX35 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

Table 6. i.MX35 Chip-Level Conditions

Characteristics	Table/Location
Absolute Maximum Ratings	Table 7 on page 13
i.MX35 Operating Ranges	Table 8 on page 14
Interface Frequency	Table 9 on page 15

Stresses beyond those listed in Table 7 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in Table 8 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 7. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply voltage (core)	VDD_{max}[1]	–0.5	1.47	V
Supply voltage (I/O)	$NVCC_{max}$	–0.5	3.6	V
Input voltage range	V_{Imax}	–0.5	3.6	V
Storage temperature	$T_{storage}$	–40	125	°C
ESD damage immunity:	V_{esd}			V
Human Body Model (HBM)		—	2000[2]	
Charge Device Model (CDM)		—	500[3]	

1 VDD is also known as QVCC.

2 HBM ESD classification level according to the AEC-Q100-002 standard

3 Corner pins max. 750 V

4.1.1 i.MX35 Operating Ranges

Table 8 provides the recommended operating ranges. The term NVCC in this section refers to the associated supply rail of an input or output.

Table 8. i.MX35 Operating Ranges

Parameter	Symbol	Min.	Typical	Max.	Units
Core Operating Voltage 0 < fARM < 400 MHz	V_{DD}	1.22	—	1.47	V
Core Operating Voltage 0 < fARM < 532 MHz		1.33	—	1.47	V
State Retention Voltage		1	—	—	V
EMI[1]	NVCC_EMI1,2,3	1.7	—	3.6	V
WTDG, Timer, CCM, CSPI1	NVCC_CRM	1.75	—	3.6	V
NANDF	NVCC_NANDF	1.75	—	3.6	V
ATA, USB generic	NVCC_ATA	1.75	—	3.6	V
eSDHC1	NVCC_SDIO	1.75	—	3.6	V
CSI, SDIO2	NVCC_CSI	1.75	—	3.6	V
JTAG	NVCC_JTAG	1.75	—	3.6	V
LCDC, TTM, I2C1	NVCC_LCDC	1.75	—	3.6	V
I2Sx2,ESAI, I2C2, UART2, UART1, FEC	NVCC_MISC	1.75	—	3.6	V
MLB	NVCC_MLB[2]	1.75	—	3.6	V
USB OTG PHY	PHY1_VDDA	3.17	3.3	3.43	V
USB OTG PHY	USBPHY1_VDDA_BIAS	3.17	3.3	3.43	V
USB OTG PHY	USBPHY1_UPLLVDD	3.17	3.3	3.43	V
USB HOST PHY	PHY2_VDD	3.0	3.3	3.6	V
OSC24M	OSC24M_VDD	3.0	3.3	3.6	V
OSC_AUDIO	OSC_AUDIO_VDD	3.0	3.3	3.6	V
MPLL	MVDD	1.4	—	1.65	V
PPLL	PVDD	1.4	—	1.65	V
Fusebox program supply voltage	FUSE_VDD[3]	3.0	3.6	3.6	V
Operating ambient temperature range	TA	–40	—	85	°C
Junction temperature range	TJ	–40	—	105	°C

1 EMI I/O interface power supply should be set up according to external memory. For example, if using SDRAM then NVCC_EMI1,2,3 should all be set at 3.3 V (typ.). If using MDDR or DDR2, NVC_EMI1,2,3 must be set at 1.8 V (typ.).

2 MLB interface I/O pads can be programmed to function as GPIO by setting NVCC_MLB to 1.8 or 3.3 V, but if used as MLB pads, NVCC_MLB must be set to 2.5 V in order to be compliant with external MOST devices. NVCC_MLB may be left floating.

3 The Fusebox read supply is connected to supply of the full speed USB PHY. FUSE_VDD is only used for programming. It is recommended that FUSE_VDD be connected to ground when not being used for programming. FUSE_VDD should be supplied by following the power up sequence given in Section 4.3.1, “Powering Up.”

4.1.2 Interface Frequency Limits

Table 9 provides information on interface frequency limits.

Table 9. Interface Frequency

ID	Parameter	Symbol	Min.	Typ.	Max.	Units
1	JTAG TCK Frequency	f_{JTAG}	DC	5	10	MHz

4.2 Power Modes

Table 10 provides descriptions of the power modes of the i.MX35 processor.

Table 10. i.MX35 Power Modes

Power Mode	Description	QVCC (ARM/L2 Peripheral)		MVDD/PVDD		OSC24M_VDD OSC_AUDO_VDD	
		Typ.	Max.	Typ.	Max.	Typ.	Max.
Wait	VDD1,2,3,4 = 1.1 V (min.) ARM is in wait for interrupt mode. MAX is active. L2 cache is kept powered. MCU PLL is on (400 MHz) PER PLL is off (can be configured) (default: 300 MHz) Module clocks are gated off (can be configured by CGR register). OSC 24M is ON. OSC audio is off (can be configured). RNGC internal osc is off.	16 mA	170 mA	7.2 mA	14 mA	1.2 mA	3 mA
Doze	VDD1,2,3,4 = 1.1 V (min.) ARM is in wait for interrupt mode. MAX is halted. L2 cache is kept powered. L2 cache control logic off. AWB enabled. MCU PLL is on(400 MHz) PER PLL is off (can be configured). (300 Mhz). Module clocks are gated off (can be configured by CGR register). OSC 24M is ON. OSC audio is off (can be configured) RNGC internal osc is off	12.4 mA	105 mA	7.2 mA	14 mA	1.2 mA	3 mA

Table 14 shows the DC electrical characteristics for GPIO, DDR2, mobile DDR, and SDRAM pins. The term NVCC refers to the power supply voltage that feeds the I/O of the module in question. For example, NVCC for the SD/MMC interface refers to NVCC_SDIO.

Table 14. I/O Pin DC Electrical Characteristics

Pin	DC Electrical Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
GPIO	High-level output voltage	Voh	Ioh = –1 mA Ioh = specified drive	NVCC – 0.15 0.8 × NVCC	—	—	V
	Low-level output voltage	Vol	Iol = 1 mA Iol = specified drive	—	—	0.15 0.2 × NVCC	V
	High-level output current for slow mode (Voh = 0.8 × NVCC)	Ioh	Standard drive High drive Max. drive	–2.0 –4.0 –8.0	—	—	mA
	High-level output current for fast mode (Voh = 0.8 × NVCC)	Ioh	Standard drive High drive Max. drive	–4.0 –6.0 –8.0	—	—	mA
	Low-level output current for slow mode (Voh = 0.2 × NVCC)	Iol	Standard drive High drive Max. drive	2.0 4.0 8.0	—	—	mA
	Low-level output current for fast mode (Voh = 0.2 × NVCC)	Iol	Standard drive High drive Max. drive	4.0 6.0 8.0	—	—	mA
	High-level DC Input Voltage with 1.8 V, 3.3 V NVCC (for digital cells in input mode)	VIH	—	0.7 × NVCC	—	NVCC	V
	Low-level DC Input Voltage with 1.8 V, 3.3 V NVCC (for digital cells in input mode	VIL	—	–0.3 V	—	0.3 × NVCC	V
	Input Hysteresis	VHYS	OVDD = 3.3 V OVDD = 1.8 V	—	410 330	—	mV
	Schmitt trigger VT+	VT+	—	0.5 × NVCC	—		V
	Schmitt trigger VT–	VT–	—	—	—	0.5 × NVCC	V
	Pull-up resistor (22 kΩ PU)	Rpu	Vi = 0	—	22	—	kΩ
	Pull-up resistor (47 kΩ PU)	Rpu	Vi = 0	—	47	—	kΩ
	Pull-up resistor (100 kΩ PU)	Rpu	Vi = 0	—	100	—	kΩ
	Pull-down resistor (100 kΩ PD)	Rpd	Vi = NVCC	—	100	—	kΩ
	External resistance to pull keeper up when enabled	Rkpu	Ipu > 620 μA @ min Vddio = 3.0 V	—	—	4.8	kΩ
	External resistance to pull keeper down when enabled	Rkpd	Ipu > 510 μA @min Vddio = 3.0 V	—	—	5.9	kΩ

Table 14. I/O Pin DC Electrical Characteristics (continued)

Pin	DC Electrical Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
DDR2	High-level output voltage	Voh	—	NVCC – 0.28	—	—	V
	Low-level output voltage	Vol	—		—	0.28	V
	Output min. source current	Ioh	—	–13.4	—	—	mA
	Output min. sink current	Iol	—	13.4	—	—	mA
	DC input logic high	VIH(dc)	—	NVCC ÷ 2 + 0.125	—	NVCC + 0.3	V
	DC input logic low	VIL(dc)	—	–0.3 V	—	NVCC ÷ 2 – 0.125	V
	DC input signal voltage (for differential signal)	Vin(dc)	—	–0.3	—	NVCC + 0.3	V
	DC differential input voltage	Vid(dc)	—	0.25	—	NVCC + 0.6	V
	Termination voltage	Vtt	—	NVCC ÷ 2 – 0.04	NVCC ÷ 2	NVCC ÷ 2 + 0.04	V
	Input current (no pull-up/down)	IIN	—	—	—	±1	μA
	Tri-state I/O supply current	Icc – NVCC	—	—	—	±1	μA
Mobile DDR	High-level output voltage	—	I_{OH} = –1mA I_{OH} = specified drive	NVCC – 0.08 0.8 × NVCC	—	—	V
	Low-level output voltage	—	I_{OL} = 1mA I_{OL} = specified drive	—	—	0.08 0.2 × NVCC	V
	High-level output current (Voh = 0.8 × NVCCV)	—	Standard drive High drive Max. drive	–3.6 –7.2 –10.8	—	—	mA
	Low-level output current (Vol = 0.2 × NVCCV)	—	Standard Drive High Drive Max. Drive	3.6 7.2 10.8	—	—	mA
	High-Level DC CMOS input voltage	VIH	—	0.7 × NVCC	—	NVCC + 0.3	V
	Low-Level DC CMOS input voltage	VIL	—	–0.3	—	0.2 × NVCC	V
	Differential receiver VTH+	VTH+	—	—	—	100	mV
	Differential receiver VTH–	VTH–	—	–100	—		mV
	Input current (no pull-up/down)	IIN	VI = 0 VI = NVCC	—	—	±1	μA
	Tri-state I/O supply current	Icc – NVCC	VI = NVCC or 0	—	—	±1	μA

Figure 6 shows the output pin transition time waveform.

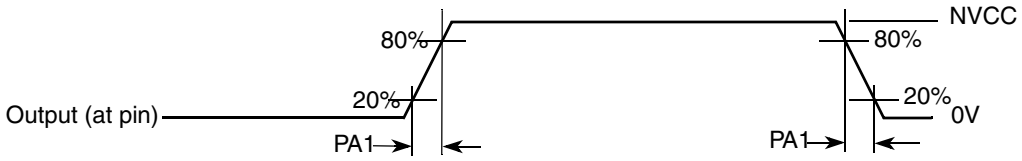


Figure 6. Output Pin Transition Time Waveform

4.8.1 AC Electrical Test Parameter Definitions

AC electrical characteristics in Table 16 through Table 21 are not applicable for the output open drain pull-down driver.

The dI/dt parameters are measured with the following methodology:

- The zero voltage source is connected between pin and load capacitance.
- The current (through this source) derivative is calculated during output transitions.

Table 15. AC Requirements of I/O Pins

Parameter	Symbol	Min.	Max.	Units
AC input logic high	VIH(ac)	NVCC ÷ 2 + 0.25	NVCC + 0.3	V
AC input logic low	VIL(ac)	–0.3	NVCC ÷ 2 – 0.25	V

Table 16. AC Electrical Characteristics of GPIO Pins in Slow Slew Rate Mode [NVCC = 3.0 V–3.6 V]

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ. Rise/Fall	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	—	60	%
Output pin slew rate (max. drive)	tps	25 pF 50 pF	0.79/1.12 0.49/0.73	1.30/1.77 0.84/1.23	2.02/2.58 1.19/1.58	V/ns
Output pin slew rate (high drive)	tps	25 pF 50 pF	0.48/0.72 0.27/0.42	0.76/1.10 0.41/0.62	1.17/1.56 0.63/0.86	V/ns
Output pin slew rate (standard drive)	tps	25 pF 50 pF	0.25/0.40 0.14/0.21	0.40/0.59 0.21/0.32	0.60/0.83 0.32/0.44	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	15 16	36 38	76 80	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	8 9	20 21	45 47	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	4 4	10 10	22 23	mA/ns

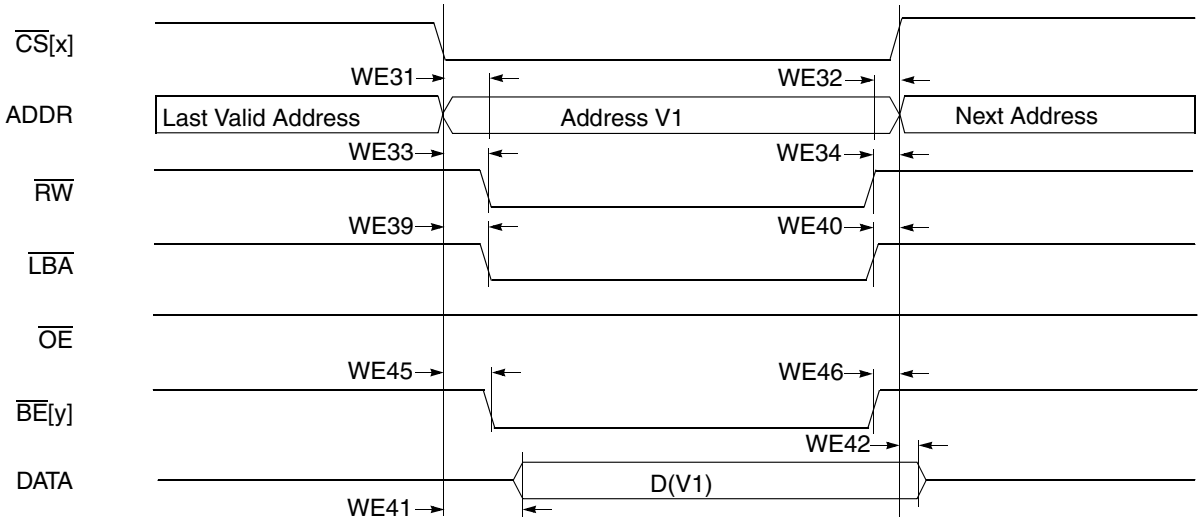


Figure 24. Asynchronous Memory Write Access

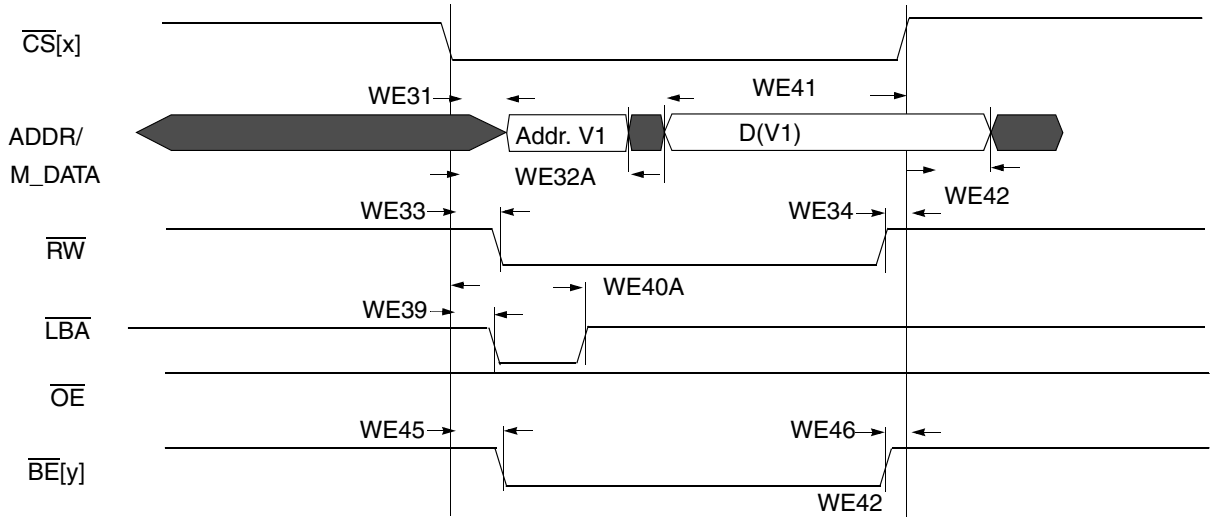


Figure 25. Asynchronous A/D Mux Write Access

Table 34. WEIM Asynchronous Timing Parameters Relative Chip Select Table (continued)

Ref No.	Parameter	Determination By Synchronous Measured Parameters[1]	Min	Max (If 133 MHz is supported by SoC)	Unit
WE40A (muxed A/D)	$\overline{CS}$[x] valid to $\overline{LBA}$ invalid	WE14 – WE6 + (LBN + LBA + 1 – CSA)	–3 + (LBN + LBA + 1 – CSA)	3 + (LBN + LBA + 1 – CSA)	ns
WE41	$\overline{CS}$[x] valid to Output Data valid	WE16 – WE6 – WCSA	—	3 – WCSA	ns
WE41A (muxed A/D)	$\overline{CS}$[x] valid to Output Data valid	WE16 – WE6 + (WLBN + WLBA + ADH + 1 – WCSA)	—	3 + (WLBN + WLBA + ADH + 1 – WCSA)	ns
WE42	Output Data invalid to $\overline{CS}$[x] Invalid	WE17 – WE7 – CSN	—	3 – CSN	ns
WE43	Input Data valid to $\overline{CS}$[x] invalid	MAXCO – MAXCSO + MAXDI	MAXCO[6] – MAXCSO[7] + MAXDI[8]	—	ns
WE44	$\overline{CS}$[x] invalid to Input Data invalid	0	0	—	ns
WE45	$\overline{CS}$[x] valid to $\overline{BE}$[y] valid (write access)	WE12 – WE6 + (WBEA – CSA)	—	3 + (WBEA – CSA)	ns
WE46	$\overline{BE}$[y] invalid to $\overline{CS}$[x] invalid (write access)	WE7 – WE13 + (WBEN – CSN)	—	–3 + (WBEN – CSN)	ns
WE47	$\overline{DTACK}$ valid to $\overline{CS}$[x] invalid	MAXCO – MAXCSO + MAXDTI	MAXCO[6] – MAXCSO[7] + MAXDTI[9]	—	ns
WE48	$\overline{CS}$[x] Invalid to $\overline{DTACK}$ invalid	0	0	—	ns

1 For the value of parameters WE4–WE21, see column BCD = 0 in Table 33.

2 $\overline{CS}$ Assertion. This bit field determines when the $\overline{CS}$ signal is asserted during read/write cycles.

3 $\overline{CS}$ Negation. This bit field determines when the $\overline{CS}$ signal is negated during read/write cycles.

4 $\overline{BE}$ Assertion. This bit field determines when the $\overline{BE}$ signal is asserted during read cycles.

5 $\overline{BE}$ Negation. This bit field determines when the $\overline{BE}$ signal is negated during read cycles.

6 Output maximum delay from internal driving ADDR/control FFs to chip outputs.

7 Output maximum delay from $\overline{CS}$[x] internal driving FFs to $\overline{CS}$[x] out.

8 DATA maximum delay from chip input data to its internal FF.

9 DTACK maximum delay from chip dtack input to its internal FF.

Note: All configuration parameters (CSA, CSN, WBEA, WBEN, LBA, LBN, OEN, OEA, RBEA, and RBEN) are in cycle units.

Figure 41 shows MII asynchronous input timings listed in Table 50.

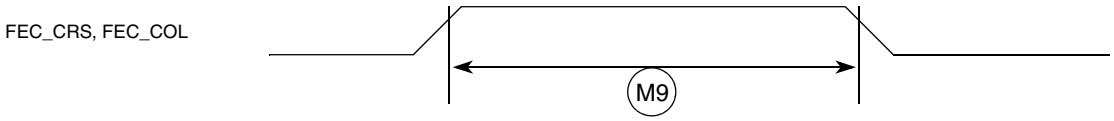


Figure 41. MII Asynch Inputs Timing Diagram

4.9.8.5 MII Serial Management Channel Timing

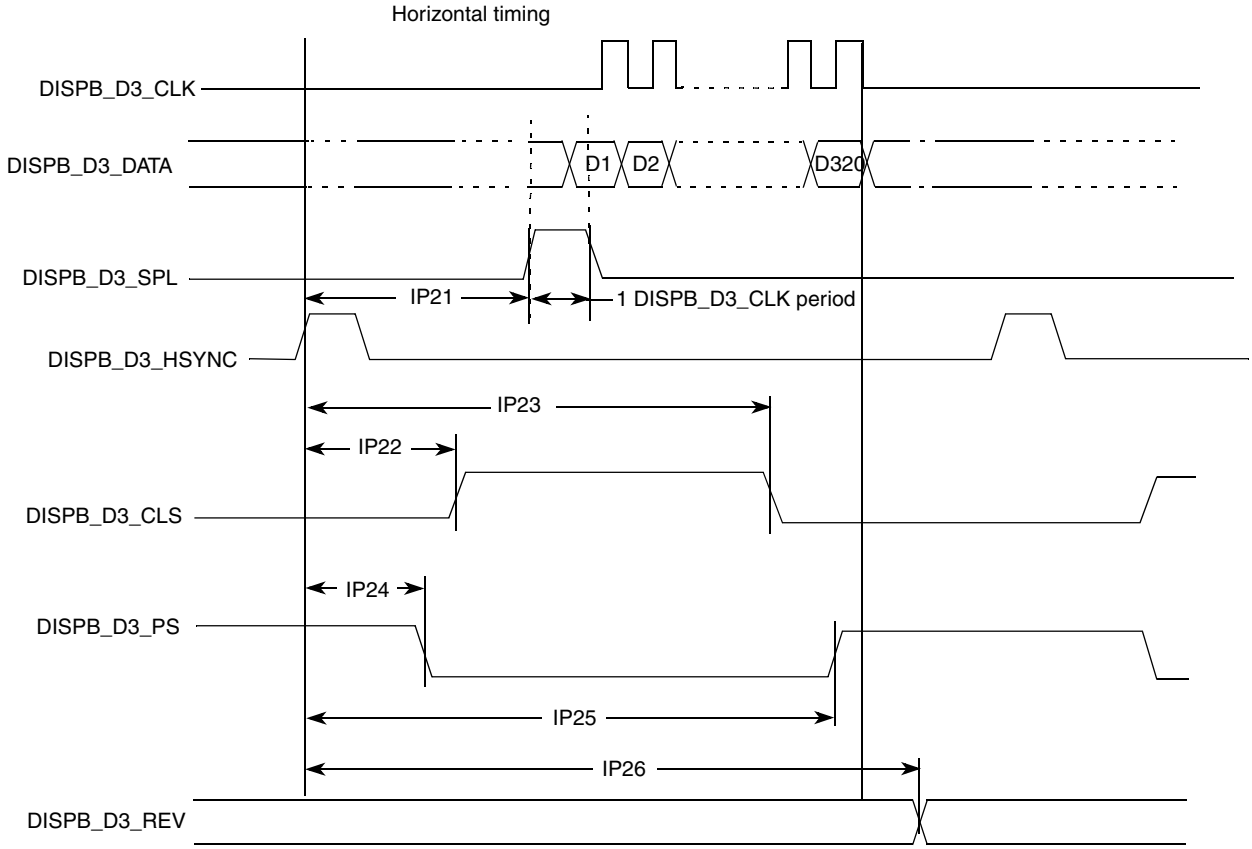
Serial management channel timing is accomplished using FEC_MDIO and FEC_MDC. The FEC functions correctly with a maximum MDC frequency of 2.5 MHz. Table 51 lists MII serial management channel timings.

The MDC frequency should be equal to or less than 2.5 MHz to be compliant with the IEEE 802.3 MII specification. However the FEC can function correctly with a maximum MDC frequency of 15 MHz.

Table 51. MII Transmit Signal Timing

Num	Characteristic	Min.	Max.	Units
M10	FEC_MDC falling edge to FEC_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	FEC_MDC falling edge to FEC_MDIO output valid (max. propagation delay)	—	5	ns
M12	FEC_MDIO (input) to FEC_MDC rising edge setup	18	—	ns
M13	FEC_MDIO (input) to FEC_MDC rising edge hold	0	—	ns
M14	FEC_MDC pulse width high	40%	60%	FEC_MDC period
M15	FEC_MDC pulse width low	40%	60%	FEC_MDC period

Section 4.9.13.1.5, “Interface to Active Matrix TFT LCD Panels, Electrical Characteristics.” The timing images correspond to straight polarity of the Sharp signals.



Example is drawn with FW + 1 = 320 pixel/line, FH + 1 = 240 lines.
SPL pulse width is fixed and aligned to the first data of the line.
REV toggles every HSYNC period.

Figure 51. Sharp HR-TFT Panel Interface Timing Diagram—Pixel Level

Table 57. Sharp Synchronous Display Interface Timing Parameters—Pixel Level

ID	Parameter	Symbol	Value	Units
IP21	SPL rise time	Tsplr	(BGXP – 1) × Tdpcp	ns
IP22	CLS rise time	Tclsr	CLS_RISE_DELAY × Tdpcp	ns
IP23	CLS fall time	Tclsf	CLS_FALL_DELAY × Tdpcp	ns
IP24	CLS rise and PS fall time	Tpsf	PS_FALL_DELAY × Tdpcp	ns
IP25	PS rise time	Tpsr	PS_RISE_DELAY × Tdpcp	ns
IP26	REV toggle time	Trev	REV_TOGGLE_DELAY × Tdpcp	ns

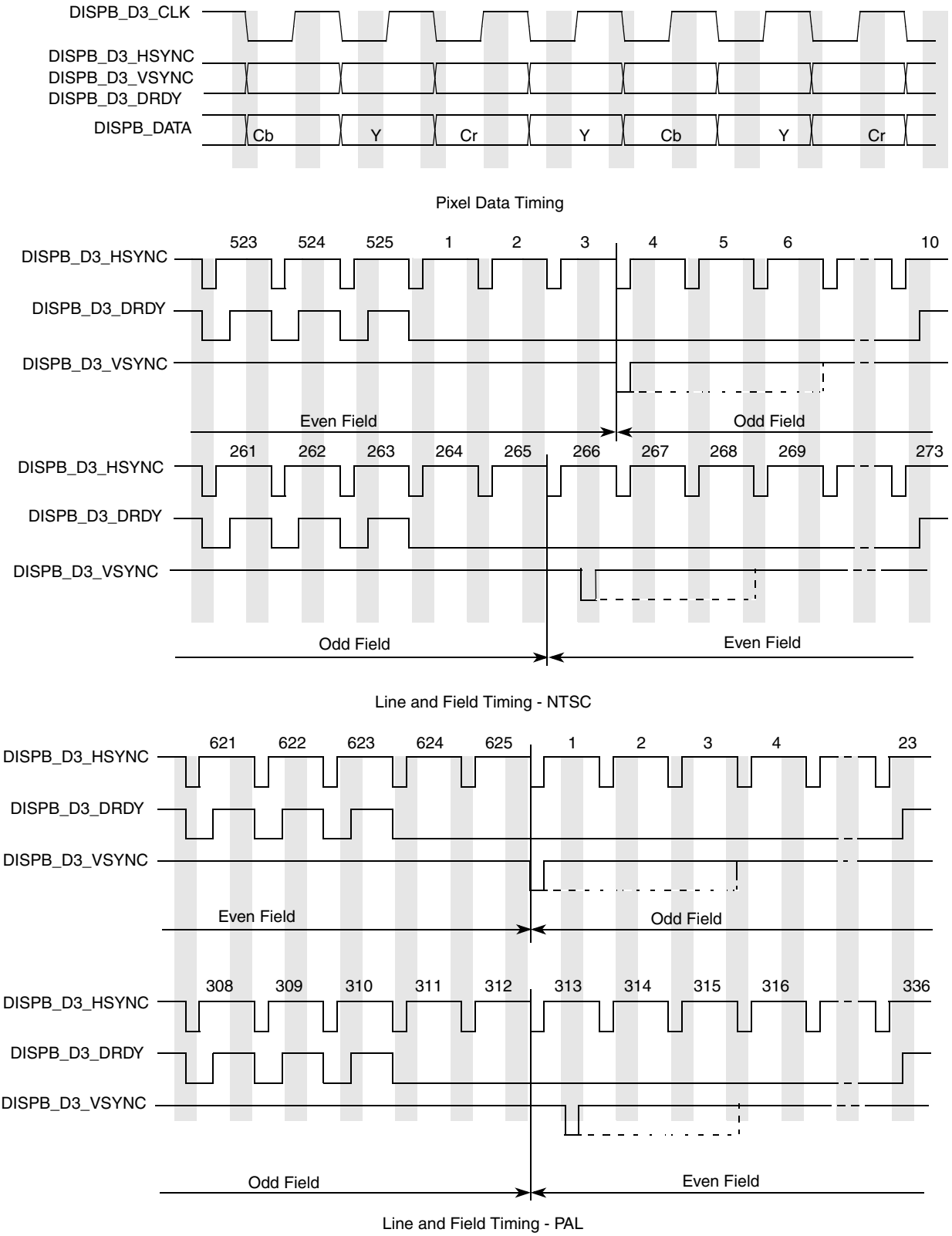


Figure 52. TV Encoder Interface Timing Diagram

4.9.13.3.7 Interface to a TV Encoder, Electrical Characteristics

The timing characteristics of the TV encoder interface are identical to the synchronous display characteristics. See Section 4.9.13.1.5, “Interface to Active Matrix TFT LCD Panels, Electrical Characteristics.”

4.9.13.4 Asynchronous Interfaces

This section discusses the asynchronous parallel and serial interfaces.

4.9.13.4.8 Parallel Interfaces, Functional Description

The IPU supports the following asynchronous parallel interfaces:

- System 80 interface
  - Type 1 (sampling with the chip select signal) with and without byte enable signals.
  - Type 2 (sampling with the read and write signals) with and without byte enable signals.
- System 68k interface
  - Type 1 (sampling with the chip select signal) with or without byte enable signals.
  - Type 2 (sampling with the read and write signals) with or without byte enable signals.

For each of four system interfaces, there are three burst modes:

1. Burst mode without a separate clock—The burst length is defined by the corresponding parameters of the IDMAC (when data is transferred from the system memory) or by the HBURST signal (when the MCU directly accesses the display via the slave AHB bus). For system 80 and system 68k type 1 interfaces, data is sampled by the CS signal and other control signals change only when transfer direction is changed during the burst. For type 2 interfaces, data is sampled by the WR/RD signals (system 80) or by the ENABLE signal (system 68k), and the CS signal stays active during the whole burst.
2. Burst mode with the separate clock DISPB_BCLK—In this mode, data is sampled with the DISPB_BCLK clock. The CS signal stays active during whole burst transfer. Other controls are changed simultaneously with data when the bus state (read, write or wait) is altered. The CS signals and other controls move to non-active state after burst has been completed.
3. Single access mode—In this mode, slave AHB and DMA burst are broken to single accesses. The data is sampled with CS or other controls according to the interface type as described above. All controls (including CS) become non-active for one display interface clock after each access. This mode corresponds to the ATI single access mode.

Both system 80 and system 68k interfaces are supported for all described modes as depicted in Figure 53, Figure 54, Figure 55, and Figure 56. These timing images correspond to active-low DISPB_D*n*_CS, DISPB_D*n*_WR and DISPB_D*n*_RD signals.

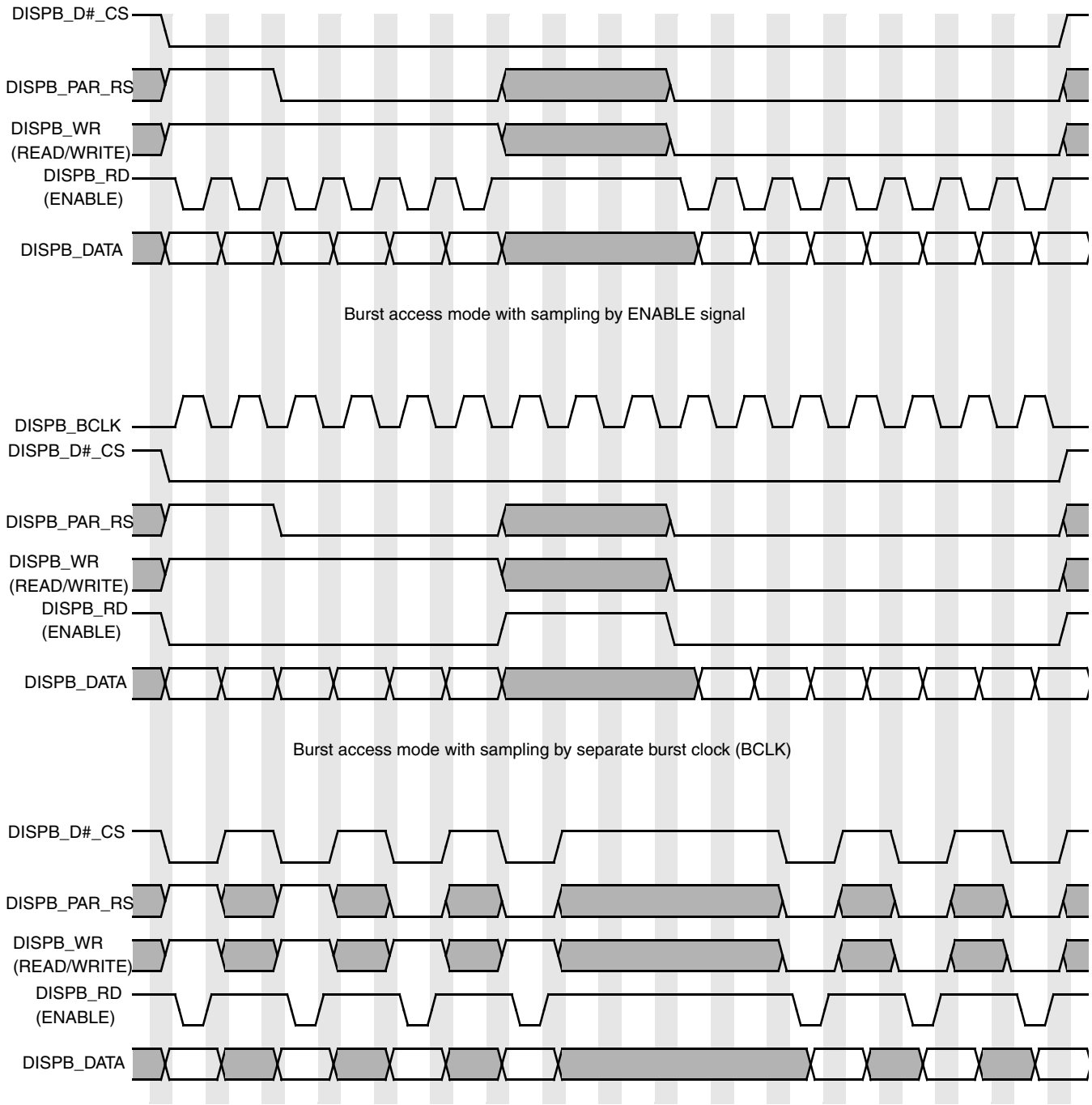


Figure 56. Asynchronous Parallel System 68k Interface (Type 2) Burst Mode TIming Diagram

Display read operation can be performed with wait states when each read access takes up to 4 display interface clock cycles according to the DISP0_RD_WAIT_ST parameter in the

Figure 77 shows timing for MDMA read, and Figure 78 shows timing for MDMA write. Table 71 lists the timing parameters for MDMA read and write.

Figure 77. MDMA Read Timing Diagram

Figure 78. MDMA Write Timing Diagram

Table 71. MDMA Read and Write Timing Parameters

ATA Parameter	Parameter from Figure 77, Figure 78	Value	Controlling Variable
tm, ti	tm	tm (min.) = ti (min.) = time_m × T – (tskew1 + tskew2 + tskew5)	time_m
td	td, td1	td1.(min.) = td (min.) = time_d × T – (tskew1 + tskew2 + tskew6)	time_d
tk	tk	tk.(min.) = time_k × T – (tskew1 + tskew2 + tskew6)	time_k
t0	—	t0 (min.) = (time_d + time_k) × T	time_d, time_k
tg(read)	tgr	tgr (min. – read) = tco + tsu + tbuf + tbuf + tcable1 + tcable2 tgr.(min. – drive) = td – te(drive)	time_d
tf(read)	tfr	tfr (min. – drive) = 0	—
tg(write)	—	tg (min. – write) = time_d × T – (tskew1 + tskew2 + tskew5)	time_d
tf(write)	—	tf (min. – write) = time_k × T – (tskew1 + tskew2 + tskew6)	time_k
tL	—	tL (max.) = (time_d + time_k–2) × T – (tsu + tco + 2 × tbuf + 2 × tcable2)	time_d, time_k

4.9.22.4 SSI Receiver Timing with External Clock

Figure 95 depicts the SSI receiver timing with external clock, and Table 81 lists the timing parameters.

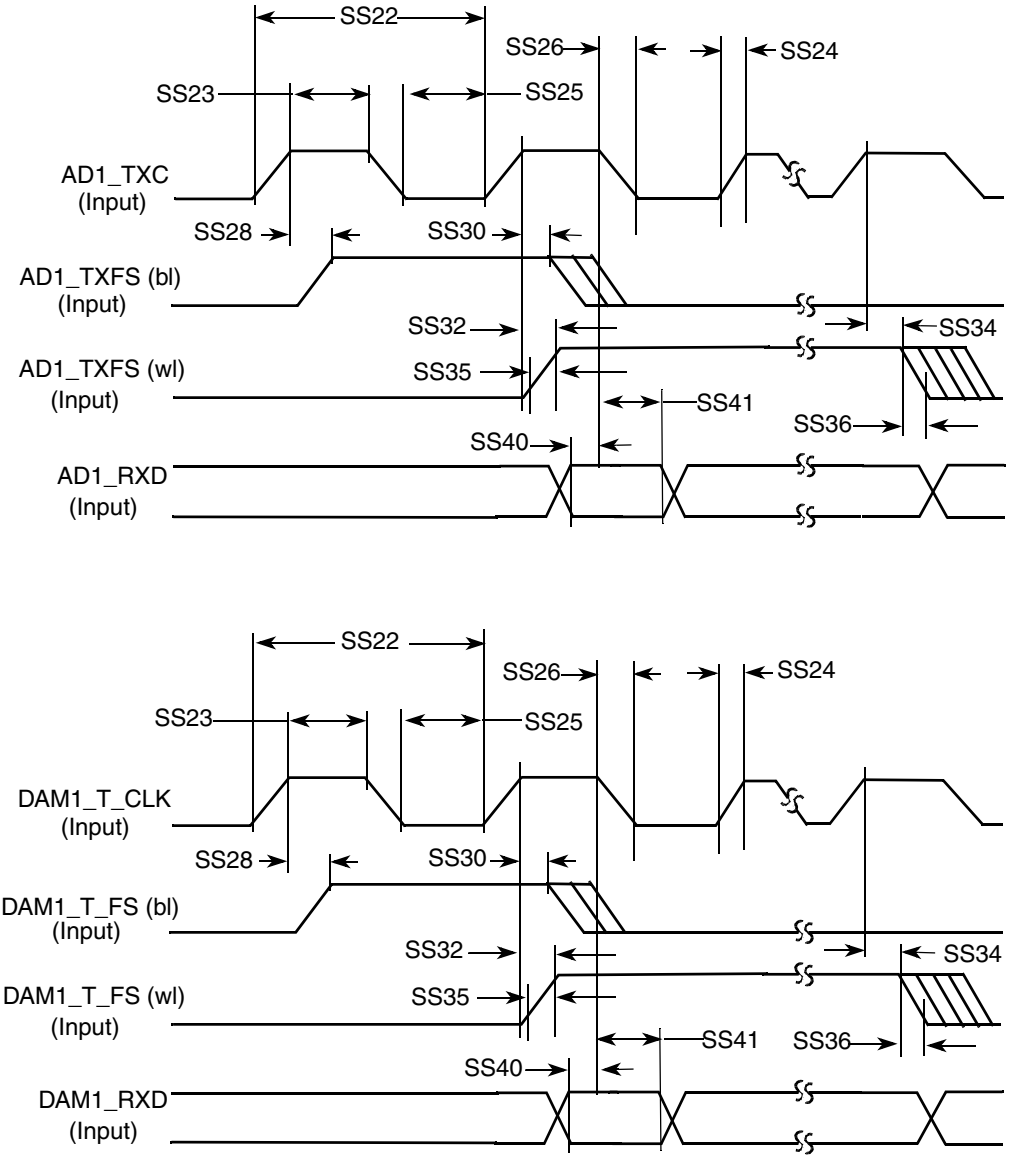


Figure 95. SSI Receiver with External Clock Timing Diagram

Table 81. SSI Receiver with External Clock Timing Parameters

ID	Parameter	Min.	Max.	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns

Table 81. SSI Receiver with External Clock Timing Parameters (continued)

ID	Parameter	Min.	Max.	Unit
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS28	(Rx) CK high to FS (bl) high	–10.0	15.0	ns
SS30	(Rx) CK high to FS (bl) low	10.0	—	ns
SS32	(Rx) CK high to FS (wl) high	–10.0	15.0	ns
SS34	(Rx) CK high to FS (wl) low	10.0	—	ns
SS35	(Tx/Rx) External FS rise time	—	6.0	ns
SS36	(Tx/Rx) External FS fall time	—	6.0	ns
SS40	SRXD setup time before (Rx) CK low	10.0	—	ns
SS41	SRXD hold time after (Rx) CK low	2.0	—	ns

4.9.23 UART Electrical

This section describes the electrical information of the UART module.

4.9.23.1 UART RS-232 Serial Mode Timing

The following subsections give the UART transmit and receive timings in RS-232 serial mode.

4.9.23.1.11 UART Transmitter

Figure 96 depicts the transmit timing of UART in RS-232 serial mode, with 8 data bit/1 stop bit format. Table 82 lists the UART RS-232 serial mode transmit timing characteristics.

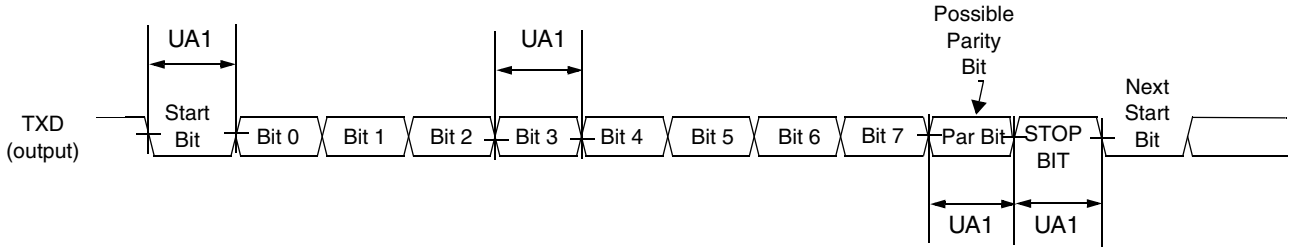


Figure 96. UART RS-232 Serial Mode Transmit Timing Diagram

Table 82. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$ [1] – T_{ref_clk} [2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.
[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.9.23.1.12 UART Receiver

Figure 97 depicts the RS-232 serial mode receive timing, with 8 data bit/1 stop bit format. Table 83 lists serial mode receive timing characteristics.

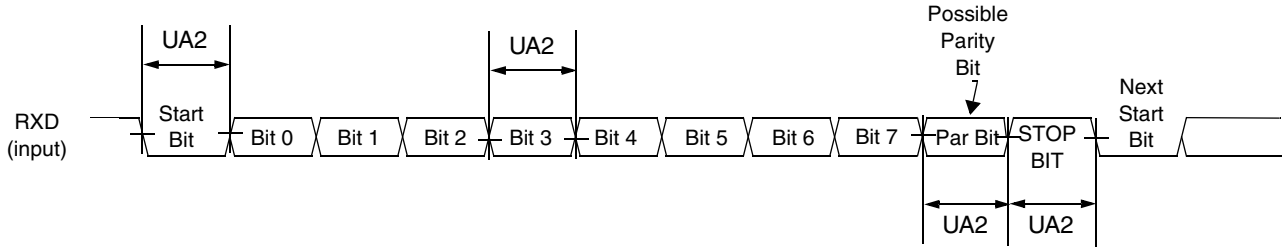


Figure 97. UART RS-232 Serial Mode Receive Timing Diagram

Table 83. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$ [2] – $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—

[1] The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.
[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency) ÷ 16.

4.9.23.2 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

4.9.23.2.13 UART IrDA Mode Transmitter

Figure 98 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 84 lists the transmit timing characteristics.

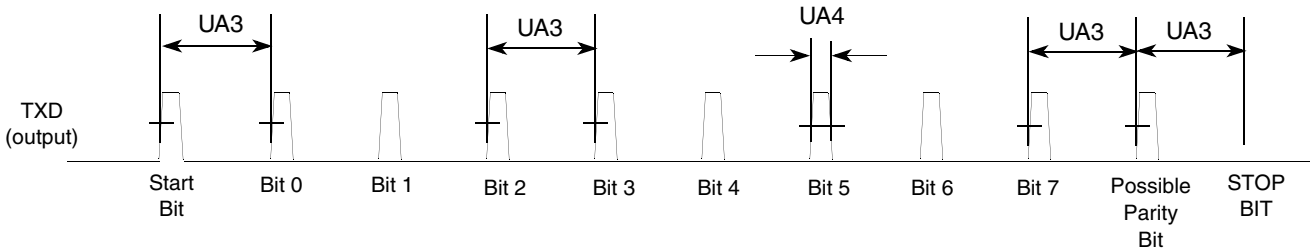


Figure 98. UART IrDA Mode Transmit Timing Diagram

Table 95. Silicon Revision 2.1 Signal Ball Map Locations (continued)

Signal ID	Ball Location
VDD	L7
VDD	N7
VDD	R7
VDD	F8
VDD	R8
VDD	F9
VDD	F12
VDD	R12
VDD	G13
VDD	H15
VDD	J15
VSS	A1
VSS	Y1
VSS	J8
VSS	M8
VSS	N8
VSS	J9

Signal ID	Ball Location
VSS	L9
VSS	N9
VSS	K10
VSS	P10
VSS	H11
VSS	H12
NVCC_EMI2	H13
VSS	J13
VSS	K13
VSS	L13
VSS	T17
VSS	A20
VSS	Y20
VSTBY	T9
WDOG_RST	Y12
XTAL_AUDIO	V19
XTAL24M	U20

[1] Not available for the MCIMX351.

Table 96. Silicon Revision 2.0 Ball Map—17 x 17, 0.8 mm Pitch[1] (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
V	ATA_DA1	ATA_INTRQ	ATA_DATA10	ATA_DATA6	ATA_DATA2	ATA_DMACK	ATA_CS0	EXT_ARMCLK	CSPI1_MISO	CLKO	GPIO3_0	CAPTURE	SD2_DATA0	CSI_HSYNC	CSI_D13	CSI_D10	SD1_DATA3	SD1_CLK	XTAL_AUDIO	OSC_AUDIO_VDD	V
W	ATA_DATA14	ATA_DATA13	ATA_DATA9	ATA_DATA5	ATA_DATA1	ATA_DIOW	USBOTG_PWR	CSPI1_SCLK	CSPI1_MOSI	BOOT_MODE0	POR_B	MLB_SIG	MLB_CLK	SD2_CLK	CSI_MCLK	CSI_D12	CSI_D9	SD1_DATA2	DE_B	EXTAL_AUDIO	W
Y	VSS	ATA_DATA11	ATA_DATA7	ATA_DATA4	ATA_DATA0	ATA_DIOR	TEST_MODE	CSPI1_SS0	POWER_FAIL	CLK_MODE0	GPIO1_1	WDOG_RST	MLB_DAT	SD2_DATA2	CSI_PIXCLK	CSI_D15	USBPHY2_DM	USBPHY2_DP	SD1_CMD	VSS	Y

[1] See Table 95 for pins unavailable in the MCIMX351 SoC.

Table 97. Silicon Revision 2.1 Ball Map—17 x 17, 0.8 mm Pitch

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	GND	D0	A9	A7	A0	SDBA0	SD30	SD27	SD24	SD23	SD21	SD18	SD15	SD14	SD10	SD9	SD6	SD4	SD1	GND	A
B	D5	D2	A13	A8	A5	SDBA1	SD31	SD28	SD26	SD22	SD20	SD19	SD12	SD13	SD11	SD7	SD0	SD2	DQM0	CS2	B
C	D8	D7	D4	MA10	A6	A3	A23	SD29	SD25	A20	SD17	SD16	A17	SD8	SD5	SD3	DQM1	DQM3	CS3	RW	C
D	D14	D10	D6	D1	A11	A4	A1	A24	A22	A21	A19	A18	A16	A14	A15	DQM2	SDCKE1	SDCKE0	ECB	LBA	D
E	NFCLE	D15	D12	D9	D3	D11	A2	A25	SDQS3	SDQS2	SDQS1	SDCLK	SDCLK_B	SDQS0	BCLK	RAS	CAS	CS4	CS1	OE	E
F	NFRE_B	NFALE	NFRB	NFWP_B	D13	A12	VDD7	VDD7	VDD7	GND	NVCC_EMI1	VDD7	NVCC_EMI2	GND	A10	EB1	CS0	EB0	CS5	LD0	F
G	RTS2	NFWE_B	NF_CE0	TX0	CTS2	NVCC_NFC	NVCC_EMI1	NVCC_EMI1	NVCC_EMI1	NVCC_EMI1	NVCC_EMI1	NVCC_EMI2	VDD6	NVCC_EMI3	SDWE	LD3	LD2	LD1	LD4	LD7	G
H	TX1	TXD2	RXD2	TX4_RX1	TX2_RX3	NVCC_NFC	NVCC_NFC	GND	NVCC_EMI1	NVCC_EMI1	GND	GND	NVCC_EMI2	NVCC_LCDC	VDD5	LD5	LD8	LD6	LD9	LD10	H
J	FST	TX3_RX2	TX5_RX0	SCKT	HCKT	STXFS5	VDD1	GND	GND	GND	GND	GND	GND	NVCC_LCDC	VDD5	LD12	LD14	LD11	LD13	LD15	J
K	STXD5	HCKR	SCKR	SRXD5	FSR	NVCC_MISC	NVCC_MISC	GND	GND	GND	GND	GND	GND	LD16	LD22	LD20	LD21	LD18	LD17	LD19	K
L	SRXD4	STXFS4	I2C2_CLK	SCK4	SCK5	FEC_TDATA3	VDD2	NVCC_MISC	GND	GND	GND	GND	GND	NVCC_LCDC	D3_FPSHIFT	CONTRAST	D3_CLS	D3_HSYNC	LD23	D3_DRDY	L
M	I2C2_DAT	STXD4	FEC_RDATA2	FEC_TDATA1	FEC_TDATA2	VDD2	GND	GND	GND	GND	FUSE_VSS	PGND	GND	NVCC_LCDC	PHY1_VDDA	TTM_PAD	D3_REV	D3_SPL	D3_VSYNC	I2C1_CLK	M
N	FEC_RDATA3	FEC_RDATA1	FEC_RX_ERR	FEC_TX_ERR	FEC_CRS	NVCC_ATA	VDD3	GND	GND	GND	MGND	GND	PVDD	USBPHY1_UPLLGND	USBPHY1_UPLLVDD	PHY1_VSSA	I2C1_DAT	USBPHY1_UID	USBPHY1_DM	PHY1_VDDA	N

7 Revision History

Table 98 shows the revision history of this document. Note: There were no revisions of this document between revision 1 and revision 4 or between revision 6 and revision 7.

Table 98. i.MX35 Data Sheet Revision History

Revision Number	Date	Substantive Change(s)
10	06/2012	• In Table 2, "Functional Differences in the i.MX35 Parts," on page 4, added two columns for part numbers MCIMX353 and MCIMX357. • Added Table 29, "Clock Input Tolerance," on page 32 in Section 4.9.3, “DPLL Electrical Specifications.” • Updated Table 39, "DDR2 SDRAM Timing Parameter Table," on page 51 for DDR2-400 values. • Updated Table 41, "DDR2 SDRAM Write Cycle Parameters," on page 53 for DDR2-400 values. • Added Table 15, "AC Requirements of I/O Pins," on page 25. • Updated WE4 parameter in Table 33, "WEIM Bus Timing Parameters," on page 38.
9	08/2010	• Updated Table 32, “NFC Timing Parameters.” • Updated Table 33, “WEIM Bus Timing Parameters.”
8	04/2010	• Updated Table 1, “Ordering Information.” • Updated Table 14, “I/O Pin DC Electrical Characteristics.”
6	10/21/2009	• Added information for silicon rev. 2.1 • Updated Table 1, “Ordering Information.” • Added Table 95, “Silicon Revision 2.1 Signal Ball Map Locations.” • Added Table 97, “Silicon Revision 2.1 Ball Map—17 x 17, 0.8 mm Pitch.”
5	08/06/2009	• Filled in TBDs in Table 14. • Revised Figure 15 and Table 33 by removing FCE = 0 and FCE = 1. Added footnote 3 to the table. • Added Table 26, “AC Electrical Characteristics of DDR Type IO Pins in SDRAM Mode Max Drive (1.8 V).”
4	04/30/2009	Note: There were no revisions of this document between revision 1 and revision 4. • In Section 4.3.1, “Powering Up,” reverse positions of steps 5 and 6. • Updated values in Table 10, “i.MX35 Power Modes.” • Added Section 4.4, “Reset Timing.” • In Section 4.8.2, “AC Electrical Characteristics for DDR Pins (DDR2, Mobile DDR, and SDRAM Modes),” removed Slow Slew rate tables, relabeled Table 24, “AC Electrical Characteristics of DDR Type IO Pins in mDDR Mode,” and Table 25, “AC Electrical Characteristics of DDR Type IO Pins in SDRAM Mode,” to exclude mention of slew rate. • In Section 4.9.5.2, “Wireless External Interface Module (WEIM),” modified Figure 16, “Synchronous Memory Timing Diagram for Read Access—WSC = 1,” through Figure 21, “Muxed A/D Mode Timing Diagram for Synchronous Read Access— WSC = 7, LBA = 1, LBN = 1, LAH = 1, OEA = 7.” • In Section 4.9.6, “Enhanced Serial Audio Interface (ESAI) Timing Specifications,” modified Figure 36, “ESAI Transmitter Timing,” and Figure 37, “ESAI Receiver Timing,” to remove extraneous signals. Removed a note from Figure 36, “ESAI Transmitter Timing.”
1	12/2008	• Updated Section 4.3.1, “Powering Up.” • Section 4.7, “Module-Level AC Electrical Specifications”: Updated NFC, SDRAM and mDDR SDRAM timing. Inserted DDR2 SDRAM timing.
0	10/2008	Initial public release