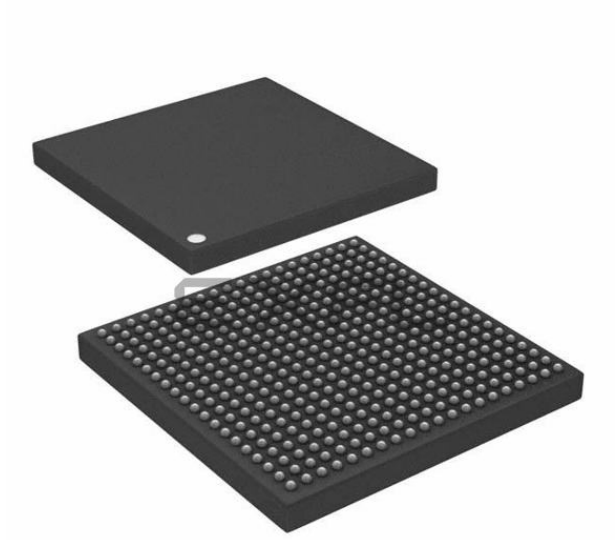

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	532MHz
Co-Processors/DSP	Multimedia; IPU, VFP
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad, KPP, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Secure Fusebox, Secure JTAG
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx355ajq5cr2

Table 10. i.MX35 Power Modes (continued)

Power Mode	Description	QVCC (ARM/L2 Peripheral)		MVDD/PVDD		OSC24M_VDD OSC_AUDO_VDD	
		Typ.	Max.	Typ.	Max.	Typ.	Max.
Stop	VDD1,2,3,4 = 1.1 V (min.) ARM is in wait for interrupt mode. MAX is halted L2 cache is kept powered. L2 cache control logic off. AWB enabled. MCU PLL is off. PER PLL is off. All clocks are gated off. OSC 24 MHz is on OSC audio is off RNGC internal osc is off	1.1 mA	77 mA	400 µA	2.2 mA	1.2 mA	2.2 mA
Static	VDD1,2,3,4 = 1.1 V (min.) ARM is in wait for interrupt mode. MAX is halted L2 cache is kept powered. L2 cache control logic off. AWB enabled. MCU PLL is off. PER PLL is off. All clocks are gated off. OSC 24MHz is on OSC audio is off RNGC internal osc is off	820 µA	72 mA	50 µA	1.7 mA	24 µA	35 µA
Note: Typical column: T_A = 25 °C **Note:** Maximum column: T_A = 85 °C							

4.3 Supply Power-Up/Power-Down Requirements and Restrictions

This section provides power-up and power-down sequence guidelines for the i.MX35 processor.

Any i.MX35 board design must comply with the power-up and power-down sequence guidelines as described in this section to guarantee reliable operation of the device. Any deviation from these sequences can result in irreversible damage to the i.MX35 processor (worst-case scenario).

Table 14 shows the DC electrical characteristics for GPIO, DDR2, mobile DDR, and SDRAM pins. The term NVCC refers to the power supply voltage that feeds the I/O of the module in question. For example, NVCC for the SD/MMC interface refers to NVCC_SDIO.

Table 14. I/O Pin DC Electrical Characteristics

Pin	DC Electrical Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
GPIO	High-level output voltage	Voh	Ioh = –1 mA Ioh = specified drive	NVCC – 0.15 0.8 × NVCC	—	—	V
	Low-level output voltage	Vol	Iol = 1 mA Iol = specified drive	—	—	0.15 0.2 × NVCC	V
	High-level output current for slow mode (Voh = 0.8 × NVCC)	Ioh	Standard drive High drive Max. drive	–2.0 –4.0 –8.0	—	—	mA
	High-level output current for fast mode (Voh = 0.8 × NVCC)	Ioh	Standard drive High drive Max. drive	–4.0 –6.0 –8.0	—	—	mA
	Low-level output current for slow mode (Voh = 0.2 × NVCC)	Iol	Standard drive High drive Max. drive	2.0 4.0 8.0	—	—	mA
	Low-level output current for fast mode (Voh = 0.2 × NVCC)	Iol	Standard drive High drive Max. drive	4.0 6.0 8.0	—	—	mA
	High-level DC Input Voltage with 1.8 V, 3.3 V NVCC (for digital cells in input mode)	VIH	—	0.7 × NVCC	—	NVCC	V
	Low-level DC Input Voltage with 1.8 V, 3.3 V NVCC (for digital cells in input mode	VIL	—	–0.3 V	—	0.3 × NVCC	V
	Input Hysteresis	VHYS	OVDD = 3.3 V OVDD = 1.8 V	—	410 330	—	mV
	Schmitt trigger VT+	VT+	—	0.5 × NVCC	—		V
	Schmitt trigger VT–	VT–	—	—	—	0.5 × NVCC	V
	Pull-up resistor (22 kΩ PU)	Rpu	Vi = 0	—	22	—	kΩ
	Pull-up resistor (47 kΩ PU)	Rpu	Vi = 0	—	47	—	kΩ
	Pull-up resistor (100 kΩ PU)	Rpu	Vi = 0	—	100	—	kΩ
	Pull-down resistor (100 kΩ PD)	Rpd	Vi = NVCC	—	100	—	kΩ
	External resistance to pull keeper up when enabled	Rkpu	Ipu > 620 μA @ min Vddio = 3.0 V	—	—	4.8	kΩ
	External resistance to pull keeper down when enabled	Rkpd	Ipu > 510 μA @min Vddio = 3.0 V	—	—	5.9	kΩ

Table 19. AC Electrical Characteristics, GPIO Pins in Fast Slew Rate Mode [NVCC = 1.65 V–1.95 V]

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	—	60	%
Output pin slew rate (max. drive)	tps	25 pF 50 pF	0.40/0.57 0.25/0.36	0.72/0.97 0.43/0.61	1.2/1.5 0.72/0.95	V/ns
Output pin slew rate (high drive)	tps	25 pF 50 pF	0.38/0.48 0.20/0.30	0.59/0.81 0.34/0.50	0.98/1.27 0.56/0.72	V/ns
Output pin slew rate (standard drive)	tps	25 pF 50 pF	0.23/0.32 0.13/0.20	0.40/0.55 0.23/0.34	0.66/0.87 0.38/0.52	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	7 7	43 46	112 118	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	11 12	31 33	81 85	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	9 10	27 28	71 74	mA/ns

Table 20. AC Electrical Characteristics of GPIO Pins in Slow Slew Rate Mode [NVCC = 2.25 V–2.75 V]

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	—	60	%
Output pin slew rate (max. drive)	tps	25 pF 40 pF 50 pF	0.63/0.85 0.52/0.67 0.41/0.59	1.10/1.40 0.90/1.10 0.73/0.99	1.86/2.20 1.53/1.73 1.20/1.50	V/ns
Output pin slew rate (high drive)	tps	25 pF 40 pF 50 pF	0.40/0.58 0.33/0.43 0.25/0.37	0.71/0.98 0.56/0.70 0.43/0.60	1.16/1.40 0.93/1.07 0.68/0.90	V/ns
Output pin slew rate (standard drive)	tps	25 pF 40 pF 50 pF	0.24/0.36 0.19/0.25 0.13/0.21	0.41/0.59 0.32/0.35 0.23/0.33	0.66/0.87 0.51/0.59 0.36/0.48	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	22 23	62 65	148 151	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	15 16	42 44	102 107	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	7 8	21 22	52 54	mA/ns

4.9.5 EMI Electrical Specifications

This section provides electrical parametrics and timing for the EMI module.

4.9.5.1 NAND Flash Controller Interface (NFC)

The i.MX35 NFC supports normal timing mode, using two flash clock cycles for one access of $\overline{RE}$ and $\overline{WE}$. AC timings are provided as multiplications of the clock cycle and fixed delay. Figure 11, Figure 12, Figure 13, and Figure 14 depict the relative timing requirements among different signals of the NFC at module level for normal mode. Table 32 lists the timing parameters.

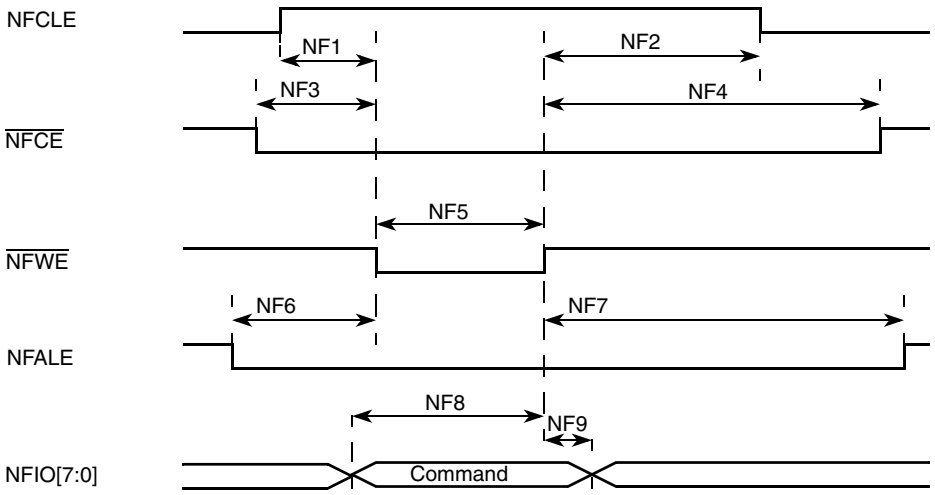

Figure 11. Command Latch Cycle Timing Diagram

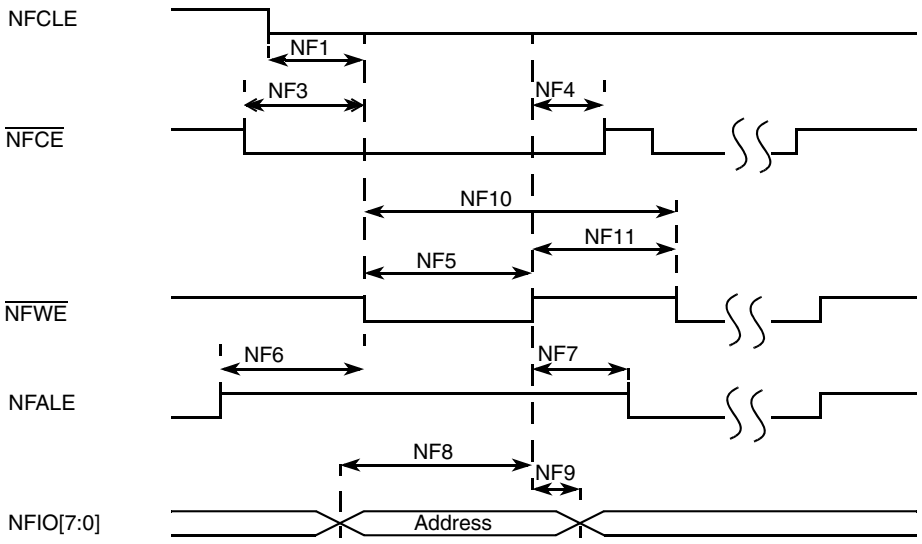

Figure 12. Address Latch Cycle Timing Diagram

Table 33. WEIM Bus Timing Parameters[1]

ID	Parameter	Min.	Max.	Unit
WE1	BCLK cycle time[2]	14.5	—	ns
WE2	BCLK low-level width[2]	7	—	ns
WE3	BCLK high-level width[2]	7	—	ns
WE4	Address valid to Clock rise/fall	15	21	ns
WE5	Clock rise/fall to address invalid	22	25	ns
WE6	Clock rise/fall to CSx_B valid	15	19	ns
WE7	Clock rise/fall to CSx_B invalid	3.6	5	ns
WE8	Clock rise/fall to RW_B valid	8	12	ns
WE9	Clock rise/fall to RW_B invalid	3	8	ns
WE10	Clock rise/fall to OE_B valid	7	12	ns
WE11	Clock rise/fall to OE_B invalid	3.8	5.5	ns
WE12	Clock rise/fall to EBy_B valid	6	11.5	ns
WE13	Clock rise/fall to EBy_B invalid	6	10	ns
WE14	Clock rise/fall to LBA_B valid	17.5	20	ns
WE15	Clock rise/fall to LBA_B invalid	0	1	ns
WE16	Clock rise/fall to Output Data valid	5	10	ns
WE17	Clock rise to Output Data invalid	0	2.5	ns
WE18	Input Data Valid to Clock rise[3]	1	—	ns
WE19	Input Data Valid to Clock rise, FCE=0 (in the case there is ECB_B asserted during access)	(BCLK/2) + 3.01	—	ns
WE19	Input Data Valid to Clock rise, FCE=0 (in the case there is NO ECB_B asserted during access)	6.9	—	ns
WE20	Clock rise to Input Data invalid[3]	1	—	ns
WE22	ECB_B setup time[3]	5	—	ns
WE24	ECB_B hold time[3]	0	—	ns
WE26	DTACK_B setup time	5.4	—	ns
WE27	DTACK_B hold time	–3.2	—	ns

1 "High" is defined as 80% of signal value, and "low" is defined as 20% of signal value.

2 BCLK parameters are measured from the 50% point. For example, "high" is defined as 50% of signal value and "low" is defined as 50% of signal value.

3 Parameters W18, W20, W22, and W24 are tested when FCE=1. i.MX35 does not support FCE=0.

NOTE

Test conditions: load capacitance, 25 pF. Recommended drive strength for all controls, address, and BCLK is set to maximum drive.

NOTE

Test conditions are: pin voltage 1.7 V–1.95 V, capacitance 15 pF for all pins (both DDR and non-DDR pins), drive strength is high (7.2 mA). “High” is defined as 80% of signal value and “low” is defined as 20% of signal value.

SDR SDRAM CLK parameters are measured from the 50% point—that is, “high” is defined as 50% of signal value, and “low” is defined as 50% of signal value. tCH + tCL will not exceed 7.5 ns for 133 MHz. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and SDCLK (inverted clock).

The timing parameters are similar to the ones used in SDRAM data sheets. Table 36 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK, and the parameters are measured at maximum memory frequency.

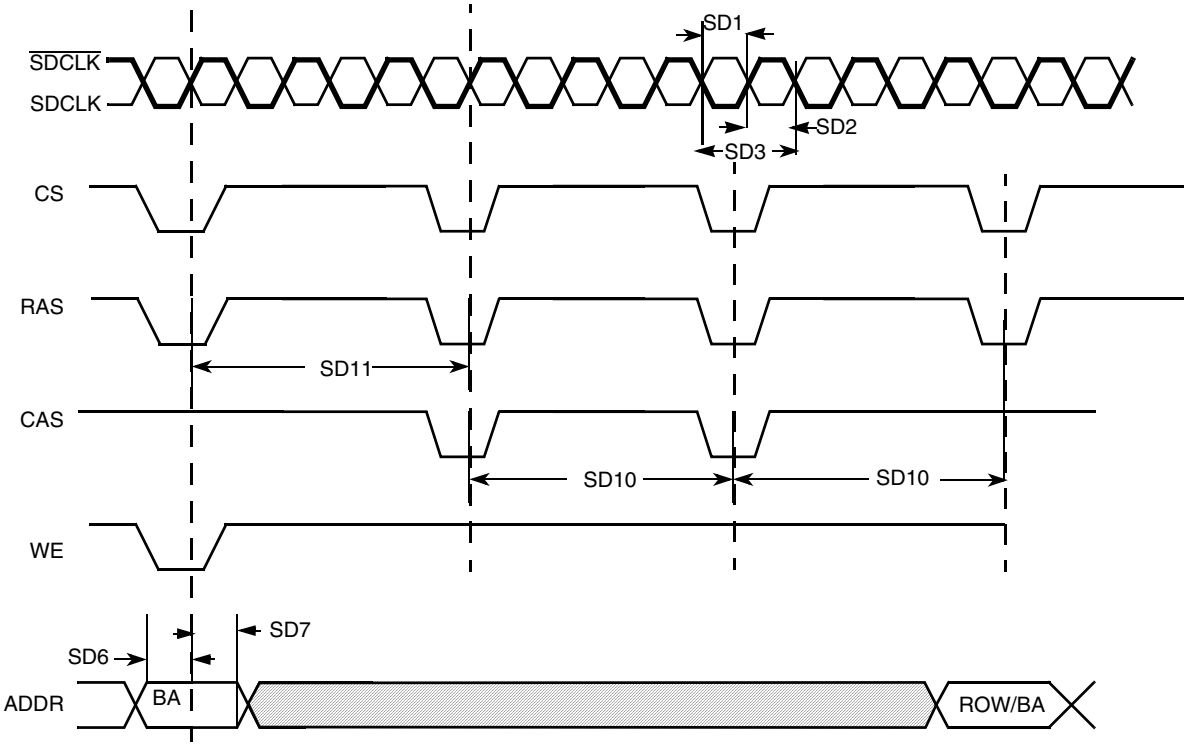

Figure 29. SDRAM Refresh Timing Diagram

Table 37. SDRAM Refresh Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD1	SDRAM clock high-level width	tCH	3.4	4.1	ns
SD2	$\overline{\text{SDRAM}}$ clock low-level width	tCL	3.4	4.1	ns
SD3	SDRAM clock cycle time	tCK	7.5	—	ns
SD6	Address setup time	tAS	1.8	—	ns

NOTE

The clock will continue to run unless both CKEs are low. Then the clock will be stopped in low state.

Table 38. SDRAM Self-Refresh Cycle Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD16	CKE output delay time	tCKS	1.8	—	ns

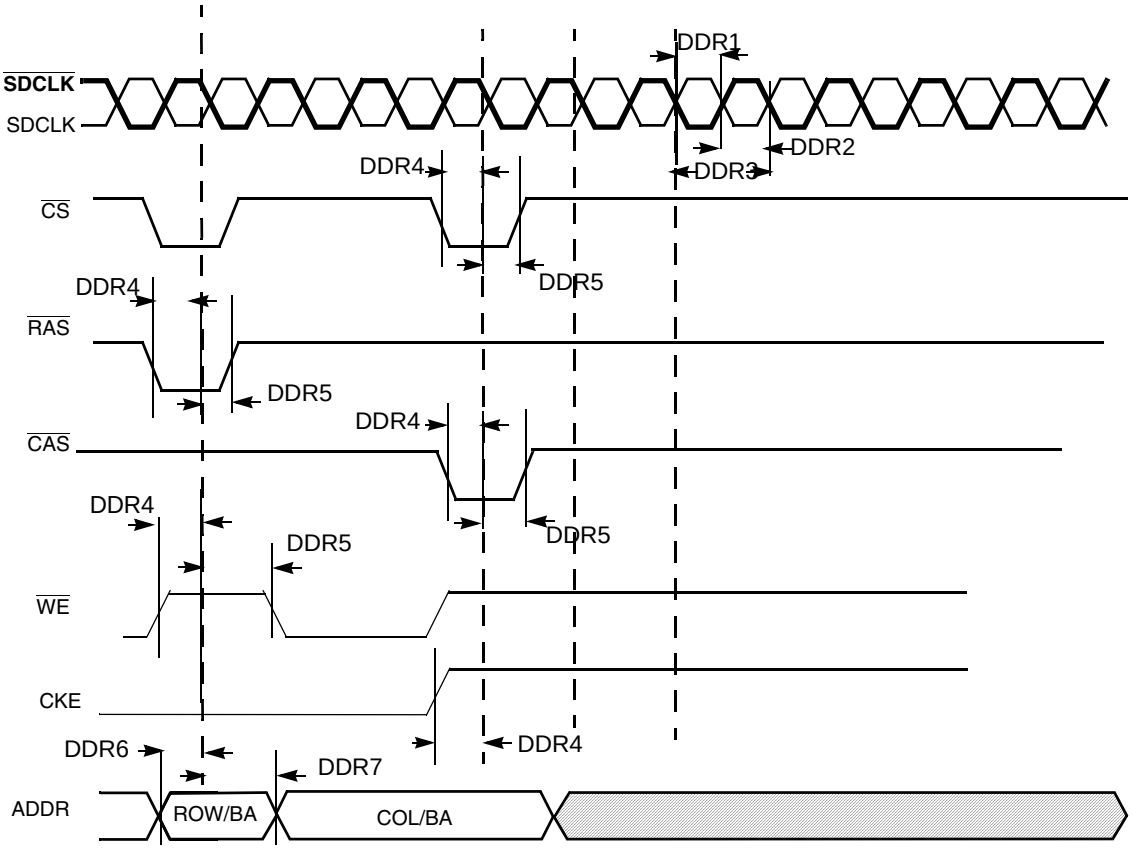

Figure 31. DDR2 SDRAM Basic Timing Parameters

Table 39. DDR2 SDRAM Timing Parameter Table

ID	PARAMETER	Symbol	DDR2-400		Unit
			Min	Max	
DDR1	SDRAM clock high-level width	t_{CH}	0.45	0.55	t_{CK}
DDR2	SDRAM clock low-level width	t_{CL}	0.45	0.55	t_{CK}
DDR3	SDRAM clock cycle time	t_{CK}	7.0	8.0	ns
DDR4	CS, RAS, CAS, CKE, WE setup time	t_{IS}[1]	1.5	—	ns

Table 39. DDR2 SDRAM Timing Parameter Table

ID	PARAMETER	Symbol	DDR2-400		Unit
			Min	Max	
DDR5	CS, RAS, CAS, CKE, WE hold time	t_{IH}[1]	1.25	—	ns
DDR6	Address output setup time	t_{IS}[1]	1.5	—	ns
DDR7	Address output hold time	t_{IH}[1]	1.5	—	ns

NOTE

These values are for command/address slew rate of 1 V/ns and SDCLK, SDCLK_B differential slew rate of 2 V/ns. For different values, use the derating table.

Table 40. Derating Values for DDR2–400, DDR2–533

Table 43. DDR2 SDRAM Read Cycle Parameter Table

ID	PARAMETER	Symbol	DDR2-400		Unit
			Min	Max	
DDR24	DQS – DQ Skew (defines the Data valid window in read cycles related to DQS).	t_{DQSQ}	—	0.35	ns
DDR25	DQS DQ in HOLD time from DQS[1]	t_{QH}	2.925	—	ns
DDR26	DQS output access time from SDCLK posedge	t_{DQSCK}	–0.5	0.5	ns

[1]The value was calculated for an SDCLK frequency of 133 MHz by the formula tQH = tHP – tQHS = min (tCL,tCH) – tQHS = 0.45 × tCK – tQHS = 0.45 × 7.5 – 0.45 = 2.925 ns.

NOTE

SDRAM CLK and DQS-related parameters are measured from the 50% point—that is, "high" is defined as 50% of signal value and "low" is defined as 50% of signal value. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and $\overline{\text{SDCLK}}$ (inverted clock).

Test conditions are: Capacitance 15 pF for DDR PADS. Recommended drive strength is Medium for SDCLK and High for Address and controls.

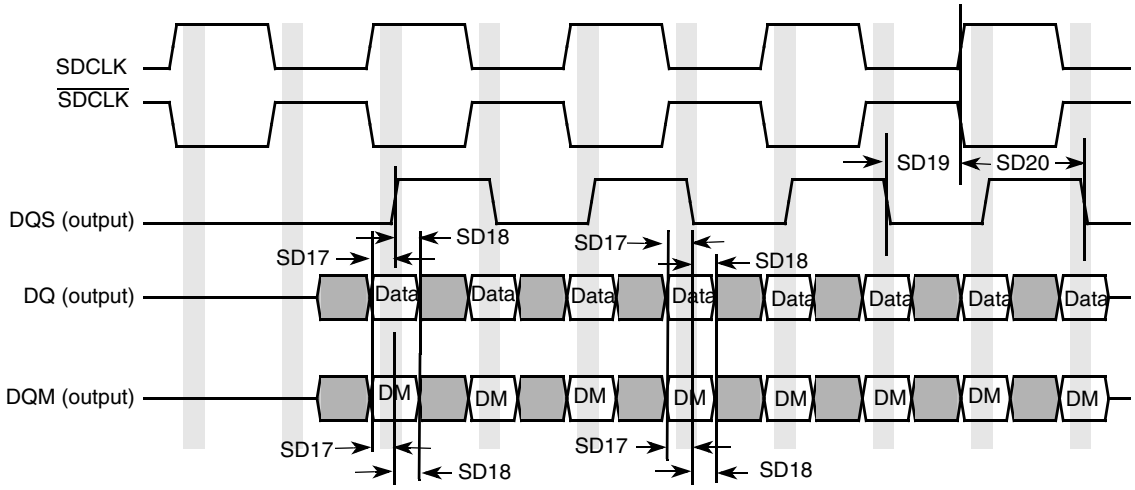

Figure 34. Mobile DDR SDRAM Write Cycle Timing Diagram

Table 44. Mobile DDR SDRAM Write Cycle Timing Parameters[1]

ID	Parameter	Symbol	Min.	Max.	Unit
SD17	DQ and DQM setup time to DQS	tDS	0.95	—	ns
SD18	DQ and DQM hold time to DQS	tDH	0.95	—	ns
SD19	Write cycle DQS falling edge to SDCLK output delay time.	tDSS	1.8	—	ns
SD20	Write cycle DQS falling edge to SDCLK output hold time.	tDSH	1.8	—	ns

[1] Test condition: Measured using delay line 5 programmed as follows: ESDCDLY5[15:0] = 0x0703.

NOTE

SDRAM CLK and DQS-related parameters are measured from the 50% point—that is, “high” is defined as 50% of signal value and “low” is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets. Table 44 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK, and the parameters are measured at maximum memory frequency.

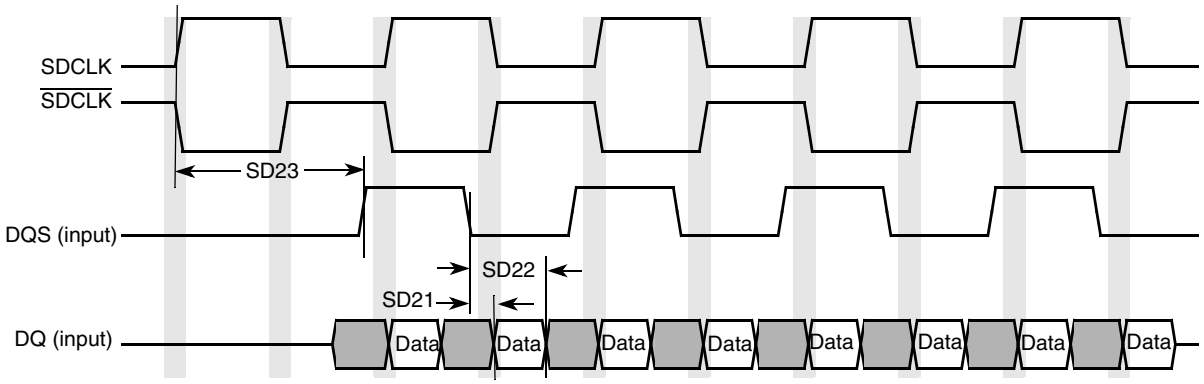

Figure 35. Mobile DDR SDRAM DQ versus DQS and SDCLK Read Cycle Timing Diagram

Table 45. Mobile DDR SDRAM Read Cycle Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD21	DQS – DQ Skew (defines the Data valid window in read cycles related to DQS).	tDQSQ	—	0.85	ns
SD22	DQS DQ HOLD time from DQS	tQH	2.3	—	ns
SD23	DQS output access time from SDCLK posedge	tDQSCK	—	6.7	ns

NOTE

SDRAM CLK and DQS-related parameters are measured from the 50% point—that is, “high” is defined as 50% of signal value, and “low” is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets. Table 45 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK, and the parameters are measured at maximum memory frequency.

4.9.6 Enhanced Serial Audio Interface (ESAI) Timing Specifications

The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. Table 46 shows the interface timing values. The number field in the table refers to timing signals found in Figure 36 and Figure 37.

Table 46. Enhanced Serial Audio Interface Timing

No.	Characteristics[1,2]	Symbol	Expression[2]	Min.	Max.	Condition[3]	Unit
62	Clock cycle[4]	t_{SSICC}	$4 \times T_C$ $4 \times T_C$	30.0 30.0	— —	i ck i ck	ns
63	Clock high period • For internal clock • For external clock	— —	$2 \times T_C - 9.0$ $2 \times T_C$	6 15	— —	— —	ns
64	Clock low period • For internal clock • For external clock	— —	$2 \times T_C - 9.0$ $2 \times T_C$	6 15	— —	— —	ns
65	SCKR rising edge to FSR out (bl) high	— —	— —	— —	17.0 7.0	x ck i ck a	ns
66	SCKR rising edge to FSR out (bl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
67	SCKR rising edge to FSR out (wr) high[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
68	SCKR rising edge to FSR out (wr) low[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
69	SCKR rising edge to FSR out (wl) high	— —	— —	— —	16.0 6.0	x ck i ck a	ns
70	SCKR rising edge to FSR out (wl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
71	Data in setup time before SCKR (SCK in synchronous mode) falling edge	— —	— —	12.0 19.0	— —	x ck i ck	ns
72	Data in hold time after SCKR falling edge	— —	— —	3.5 9.0	— —	x ck i ck	ns
73	FSR input (bl, wr) high before SCKR falling edge[5]	— —	— —	2.0 12.0	— —	x ck i ck a	ns
74	FSR input (wl) high before SCKR falling edge	— —	— —	2.0 12.0	— —	x ck i ck a	ns
75	FSR input hold time after SCKR falling edge	— —	— —	2.5 8.5	— —	x ck i ck a	ns
78	SCKT rising edge to FST out (bl) high	— —	— —	— —	18.0 8.0	x ck i ck	ns
79	SCKT rising edge to FST out (bl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns

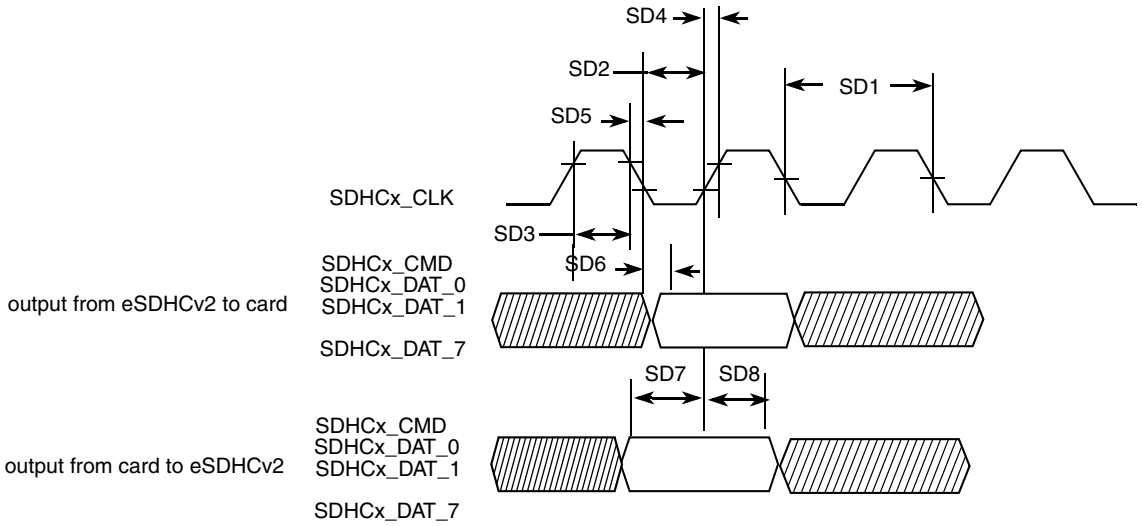

Figure 38. eSDHCv2 Timing

Table 47. eSDHCv2 Interface Timing Specification

ID	Parameter	Symbols	Min.	Max.	Unit
Card Input Clock					
SD1	Clock frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low time	t_{WL}	7	—	ns
SD3	Clock high time	t_{WH}	7	—	ns
SD4	Clock rise time	t_{TLH}	—	3	ns
SD5	Clock fall time	t_{THL}	—	3	ns
eSDHC Output/Card Inputs CMD, DAT (Reference to CLK)					
SD6	eSDHC output delay	t_{OD}	–3	3	ns
eSDHC Input/Card Outputs CMD, DAT (Reference to CLK)					
SD7	eSDHC input setup time	t_{ISU}	5	—	ns
SD8	eSDHC input hold time	t_{IH}[4]	2.5	—	ns

1 In low-speed mode, the card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal-speed mode for the SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.

3 In normal-speed mode for MMC card, clock frequency can be any value between 0 and 20 MHz. In high-speed mode, clock frequency can be any value between 0–52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

Figure 41 shows MII asynchronous input timings listed in Table 50.

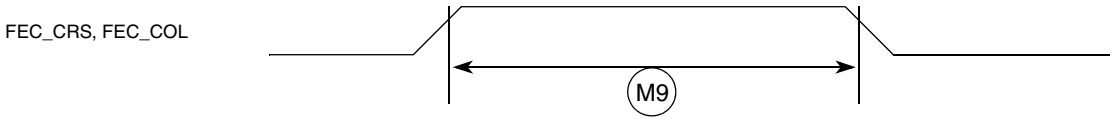

Figure 41. MII Asynch Inputs Timing Diagram

4.9.8.5 MII Serial Management Channel Timing

Serial management channel timing is accomplished using FEC_MDIO and FEC_MDC. The FEC functions correctly with a maximum MDC frequency of 2.5 MHz. Table 51 lists MII serial management channel timings.

The MDC frequency should be equal to or less than 2.5 MHz to be compliant with the IEEE 802.3 MII specification. However the FEC can function correctly with a maximum MDC frequency of 15 MHz.

Table 51. MII Transmit Signal Timing

Num	Characteristic	Min.	Max.	Units
M10	FEC_MDC falling edge to FEC_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	FEC_MDC falling edge to FEC_MDIO output valid (max. propagation delay)	—	5	ns
M12	FEC_MDIO (input) to FEC_MDC rising edge setup	18	—	ns
M13	FEC_MDIO (input) to FEC_MDC rising edge hold	0	—	ns
M14	FEC_MDC pulse width high	40%	60%	FEC_MDC period
M15	FEC_MDC pulse width low	40%	60%	FEC_MDC period

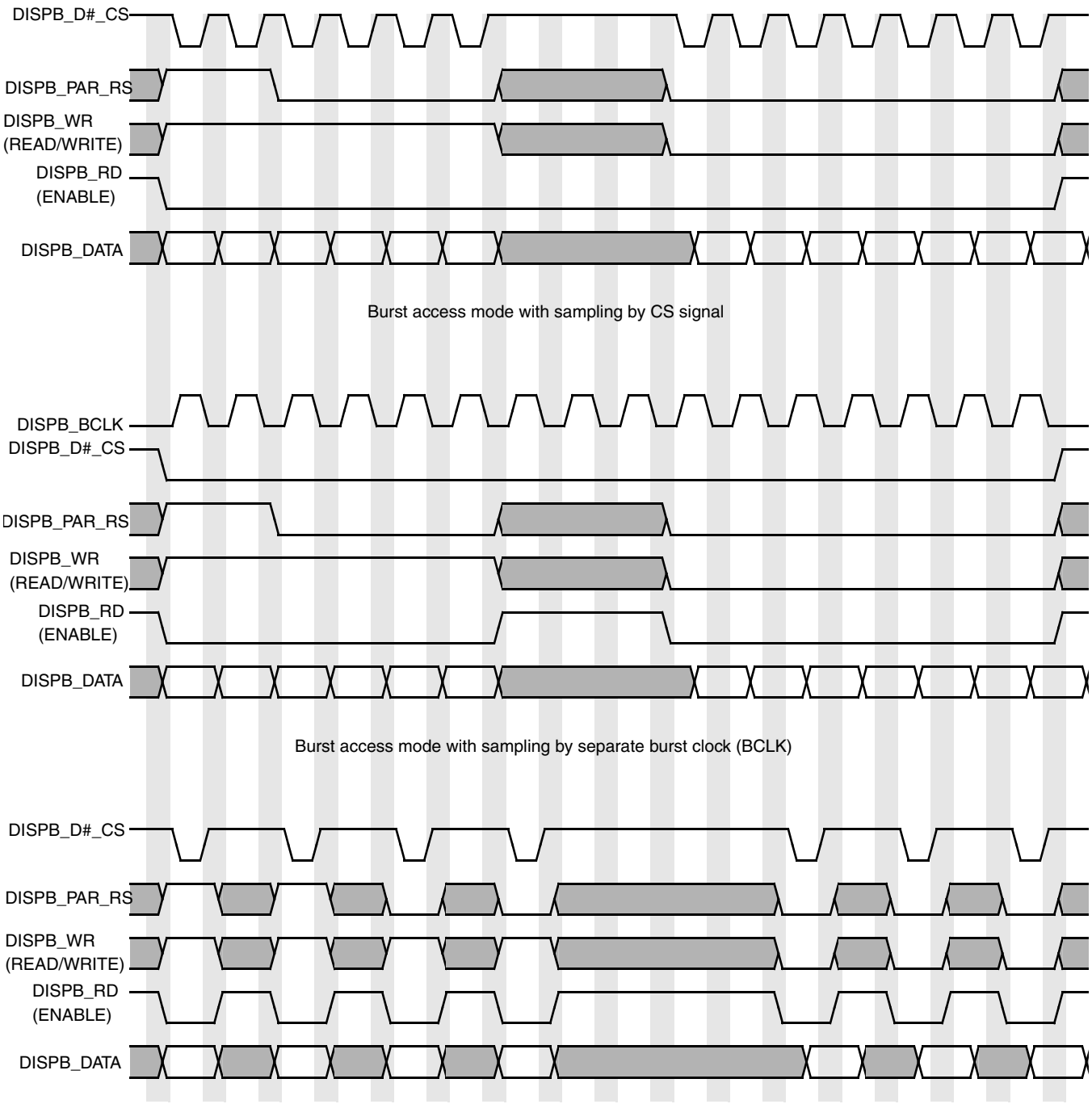

Figure 55. Asynchronous Parallel System 68k Interface (Type 1) Burst Mode Timing Diagram

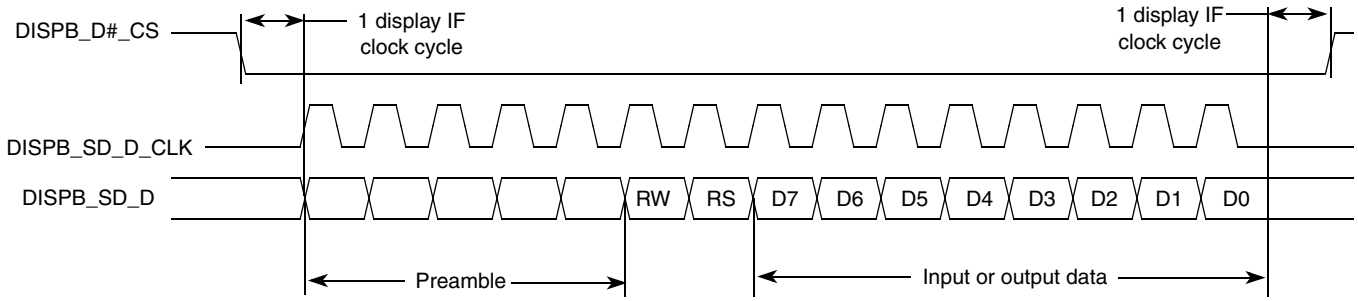

Figure 62. 3-Wire Serial Interface Timing Diagram

Figure 63 depicts timing of the 4-wire serial interface. For this interface, there are separate input and output data lines both inside and outside the device.

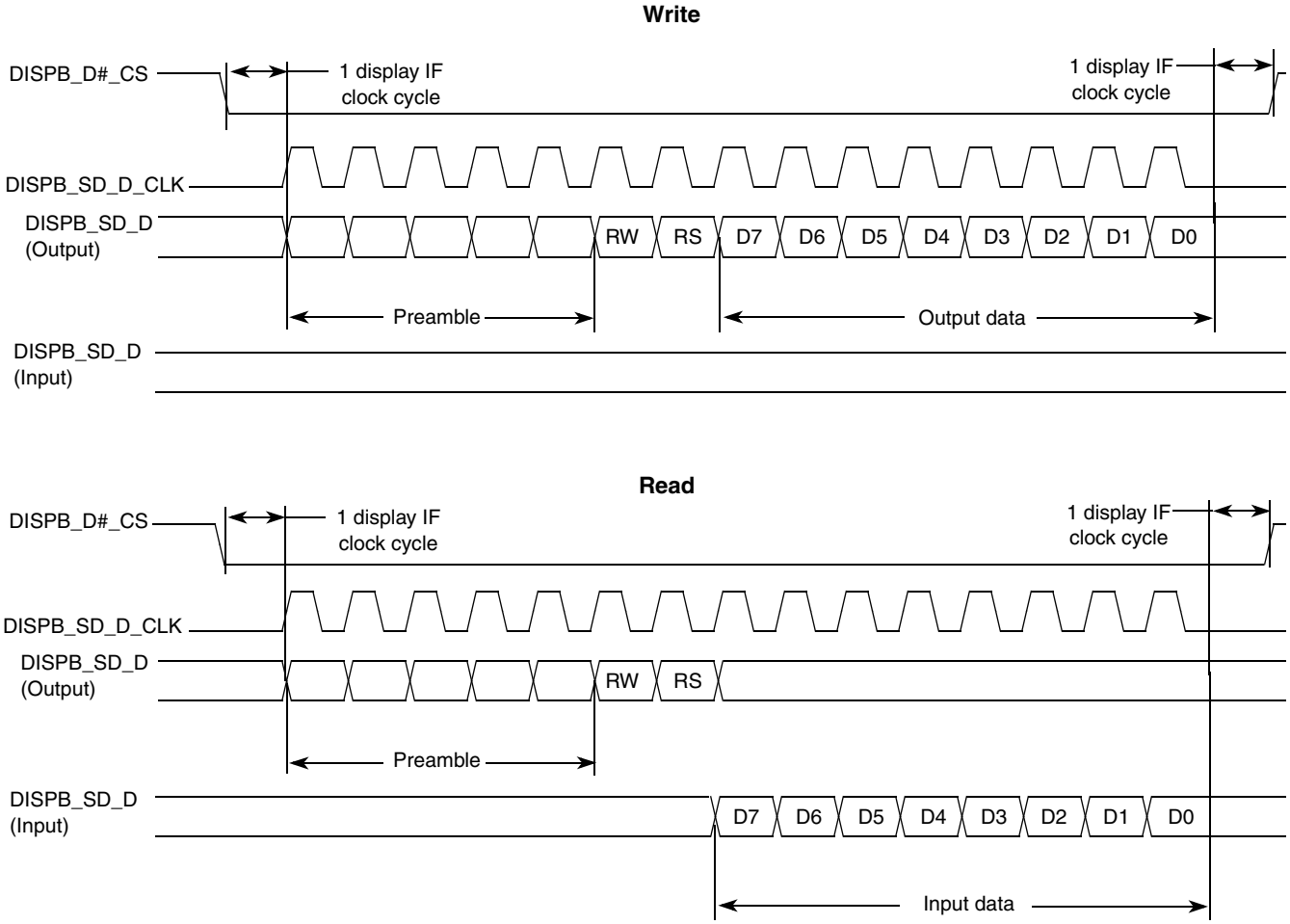

Figure 63. 4-Wire Serial Interface Timing Diagram

Figure 65 depicts timing of the 5-wire serial interface (Type 2). For this interface, a separate RS line is added. When a burst is transmitted within a single active chip select interval, the RS can be changed at boundaries of words.

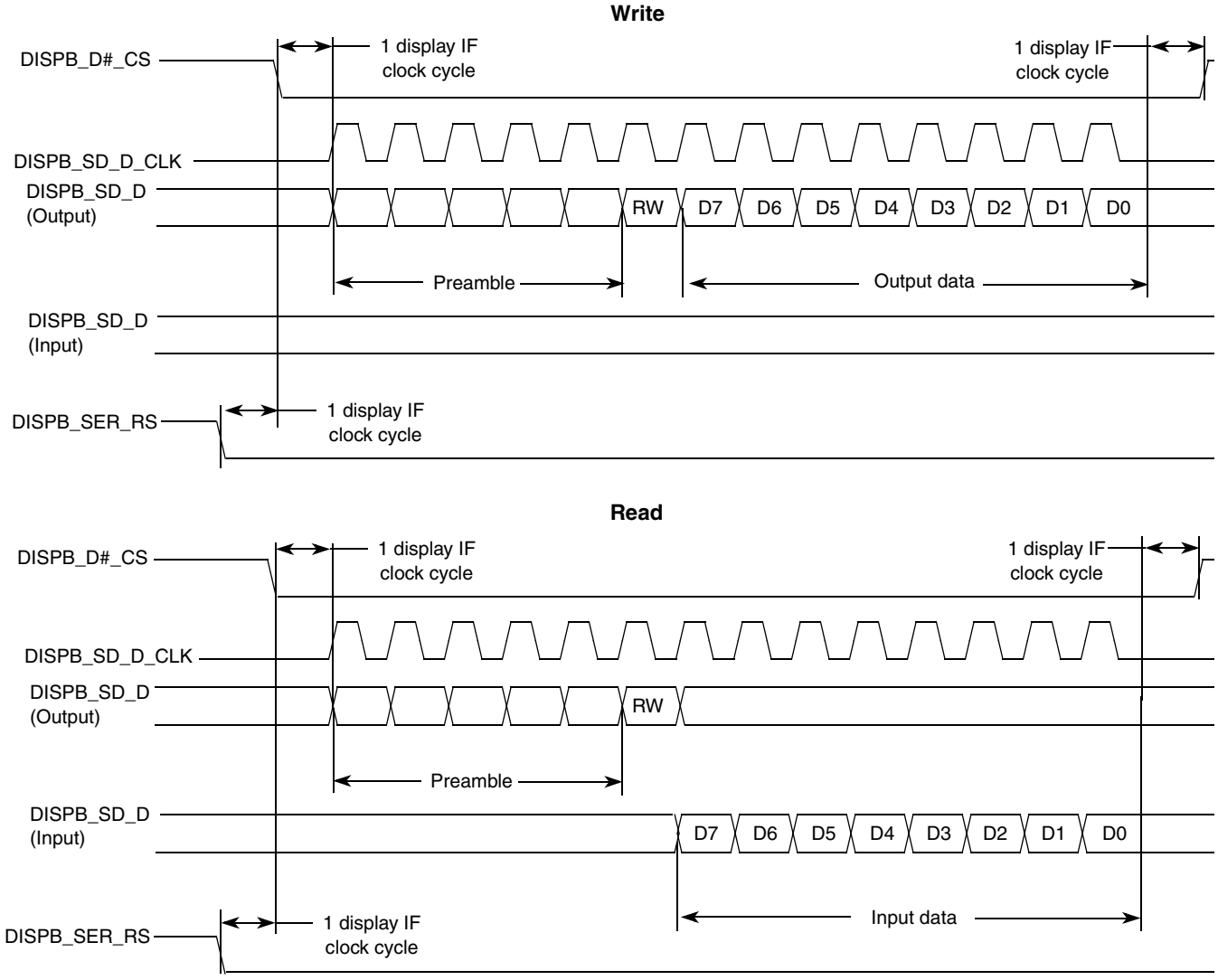

Figure 65. 5-Wire Serial Interface (Type 2) Timing Diagram

Table 59. Asynchronous Serial Interface Timing Parameters—Access Level (continued)

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP55	Controls hold time for read	Tdchr	Tdicpr – Tdicdr – 1.5	Tdicpr – Tdicdr	—	ns
IP56	Controls setup time for write	Tdcsw	Tdicuw – 1.5	Tdicuw	—	ns
IP57	Controls hold time for write	Tdchw	Tdicpw – Tdicdw – 1.5	Tdicpw – Tdicdw	—	ns
IP58	Slave device data delay[8]	Tracc	0	—	Tdrp[9] – Tlbd[10] – Tdicur – 1.5	ns
IP59	Slave device data hold time[8]	Troh	Tdrp – Tlbd – Tdicdr + 1.5	—	Tdicpr – Tdicdr – 1.5	ns
IP60	Write data setup time	Tds	Tdicdw – 1.5	Tdicdw	—	ns
IP61	Write data hold time	Tdh	Tdicpw – Tdicdw – 1.5	Tdicpw – Tdicdw	—	ns
IP62	Read period[2]	Tdicpr	Tdicpr – 1.5	Tdicpr	Tdicpr + 1.5	ns
IP63	Write period[3]	Tdicpw	Tdicpw – 1.5	Tdicpw	Tdicpw + 1.5	ns
IP64	Read down time[4]	Tdicdr	Tdicdr – 1.5	Tdicdr	Tdicdr + 1.5	ns
IP65	Read up time[5]	Tdicur	Tdicur – 1.5	Tdicur	Tdicur + 1.5	ns
IP66	Write down time[6]	Tdicdw	Tdicdw – 1.5	Tdicdw	Tdicdw + 1.5	ns
IP67	Write up time[7]	Tdicuw	Tdicuw – 1.5	Tdicuw	Tdicuw + 1.5	ns
IP68	Read time point[9]	Tdrp	Tdrp – 1.5	Tdrp	Tdrp + 1.5	ns

1 The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device specific.

2 Display interface clock period value for read:

$$Tdicpr = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_RD}{HSP\_CLK\_PERIOD}\right]$$

3 Display interface clock period value for write:

$$Tdicpw = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_WR}{HSP\_CLK\_PERIOD}\right]$$

4 Display interface clock down time for read:

$$Tdicdr = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_DOWN\_RD}{HSP\_CLK\_PERIOD}\right]$$

5 Display interface clock up time for read:

$$Tdicur = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_UP\_RD}{HSP\_CLK\_PERIOD}\right]$$

6 Display interface clock down time for write:

$$Tdicdw = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_DOWN\_WR}{HSP\_CLK\_PERIOD}\right]$$

7 Display interface clock up time for write:

$$Tdicuw = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_UP\_WR}{HSP\_CLK\_PERIOD}\right]$$

8 This parameter is a requirement to the display connected to the IPU.

4.9.17 Parallel ATA Module AC Electrical Specifications

The parallel ATA module can work on PIO/multiword DMA/ultra-DMA transfer modes (not available for the MCIMX351). Each transfer mode has a different data transfer rate, Ultra DMA mode 4 data transfer rate is up to 100 MBps.

The parallel ATA module interface consists of a total of 29 pins. Some pins have different functions in different transfer modes. There are various requirements for timing relationships among the function pins, in compliance with the ATA/ATAPI-6 specification, and these requirements are configurable by the ATA module registers.

4.9.17.1 General Timing Requirements

Table 67 and Figure 74 define the AC characteristics of the interface signals on all data transfer modes.

Table 67. AC Characteristics of All Interface Signals

ID	Parameter	Symbol	Min.	Max.	Unit
SI1	Rising edge slew rate for any signal on the ATA interface[1]	S_{rise}[1]	—	1.25	V/ns
SI2	Falling edge slew rate for any signal on the ATA interface[1]	S_{fall}[1]	—	1.25	V/ns
SI3	Host interface signal capacitance at the host connector	C_{host}	—	20	pF

[1] SRISE and SFALL meet this requirement when measured at the sender's connector from 10–90% of full signal amplitude with all capacitive loads from 15 pF through 40 pF, where all signals have the same capacitive load value.

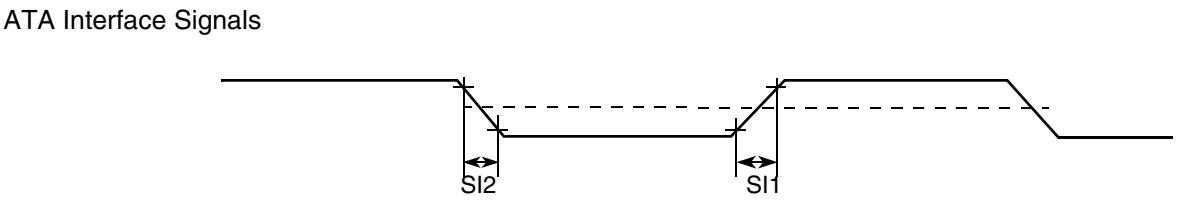

Figure 74. ATA Interface Signals Timing Diagram

4.9.17.2 ATA Electrical Specifications (ATA Bus, Bus Buffers)

This section discusses ATA parameters. For a detailed description, refer to the ATA-6 specification.

Level shifters are required for 3.3-V or 5.0-V compatibility on the ATA interface.

The use of bus buffers introduces delays on the bus and introduces skew between signal lines. These factors make it difficult to operate the bus at the highest speed (UDMA-5) when bus buffers are used. Use of bus buffers is not recommended if fast UDMA mode is required.

The ATA specification imposes a slew rate limit on the ATA bus. According to this limit, any signal driven on the bus should have a slew rate between 0.4 and 1.2 V/ns with a 40 pF load. Few vendors of bus buffers specify the slew rate of the outgoing signals.

When bus buffers are used the ata_data bus buffer is bidirectional, and uses the direction control signal ata_buffer_en. When ata_buffer_en is asserted, the bus should drive from host to device. When

4.9.24.1 DAT_SE0 Bidirectional Mode

Table 86 defines the signals for DAT_SE0 bidirectional mode. Figure 100 and Figure 101 show the transmit and receive waveforms respectively.

Table 86. Signal Definitions—DAT_SE0 Bidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out In	Tx data when USB_TXOE_B is low Differential Rx data when USB_TXOE_B is high
USB_SE0_VM	Out In	SE0 drive when USB_TXOE_B is low SE0 Rx indicator when USB_TXOE_B is high

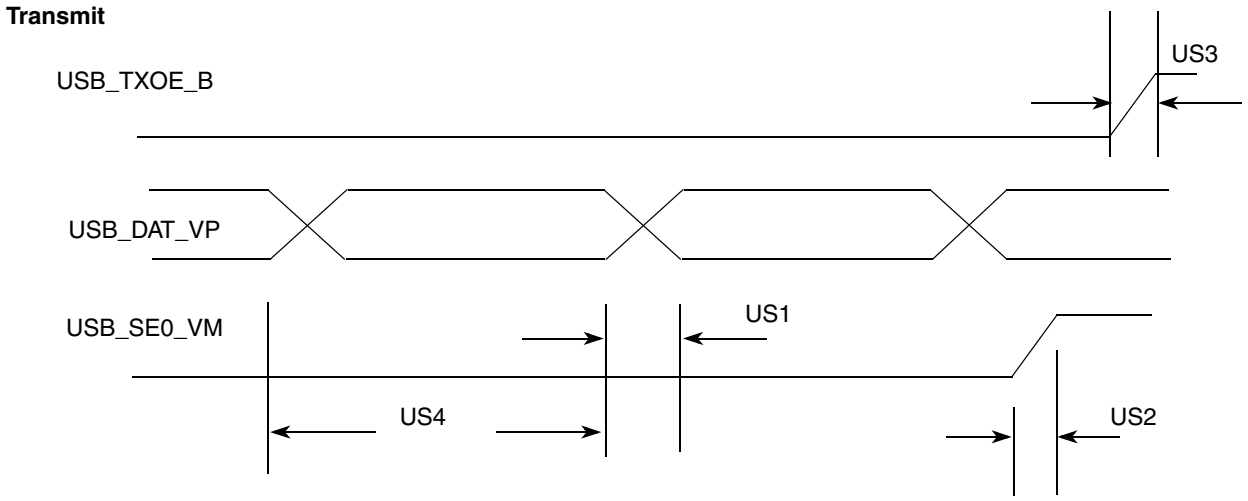

Figure 100. USB Transmit Waveform in DAT_SE0 Bidirectional Mode

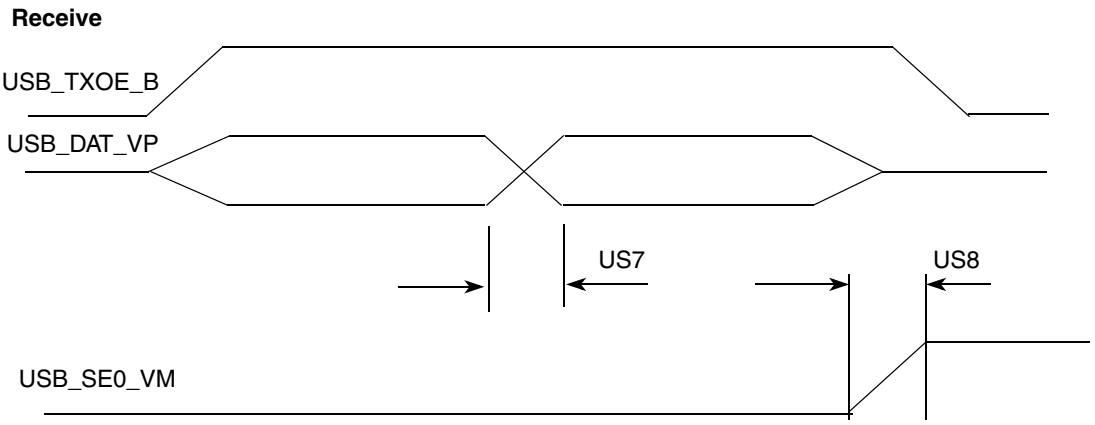

Figure 101. USB Receive Waveform in DAT_SE0 Bidirectional Mode

Table 87 describes the port timing specification in DAT_SE0 bidirectional mode.

Table 87. Port Timing Specification in DAT_SE0 Bidirectional Mode

No.	Parameter	Signal Name	Direction	Min.	Max.	Unit	Conditions/Reference Signal
US1	Tx rise/fall time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US2	Tx rise/fall time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US3	Tx rise/fall time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US4	Tx duty cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US7	Rx rise/fall time	USB_DAT_VP	In	—	3.0	ns	35 pF
US8	Rx rise/fall time	USB_SE0_VM	In	—	3.0	ns	35 pF

4.9.24.2 DAT_SE0 Unidirectional Mode

Table 88 defines the signals for DAT_SE0 unidirectional mode. Figure 102 and Figure 103 show the transmit and receive waveforms respectively.

Table 88. Signal Definitions—DAT_SE0 Unidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out	Tx data when USB_TXOE_B is low
USB_SE0_VM	Out	SE0 drive when USB_TXOE_B is low
USB_VP1	In	Buffered data on DP when USB_TXOE_B is high
USB_VM1	In	Buffered data on DM when USB_TXOE_B is high
USB_RCV	In	Differential Rx data when USB_TXOE_B is high

Transmit

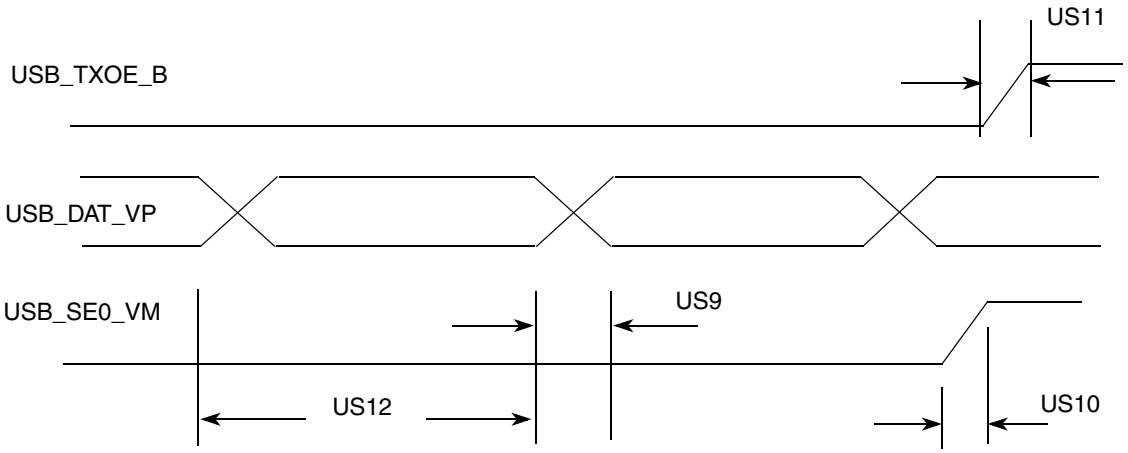

Figure 102. USB Transmit Waveform in DAT_SE0 Unidirectional Mode