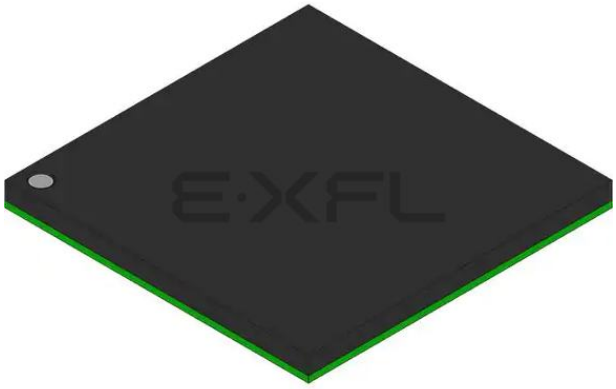

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Multimedia; IPU, VFP
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad, KPP, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Secure Fusebox, Secure JTAG
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx355avm4b

Table 4. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Domain[1]	Subsystem	Brief Description
I^2C(3)	I^2C module	ARM	ARM1136 platform peripherals	Inter-integrated circuit (I^2C) is an industry-standard, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. I^2C is suitable for applications requiring occasional communications over a short distance among many devices. The interface operates at up to 100 kbps with maximum bus loading and timing. The I^2C system is a true multiple-master bus, with arbitration and collision detection that prevent data corruption if multiple devices attempt to control the bus simultaneously. This feature supports complex applications with multiprocessor control and can be used for rapid testing and alignment of end products through external connections to an assembly-line computer.
IIM	IC identification module	ARM	Security modules	The IIM provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, and various control signals requiring a fixed value.
IOMUX	External signals and pin multiplexing	ARM	Pins	Each I/O multiplexer provides a flexible, scalable multiplexing solution with the following features: • Up to eight output sources multiplexed per pin • Up to four destinations for each input pin • Unselected input paths held at constant levels for reduced power consumption
IPUv1	Image processing unit	ARM	Multimedia peripherals	The IPU supports video and graphics processing functions. It also provides the interface for image sensors and displays. The IPU performs the following main functions: • Preprocessing of data from the sensor or from the external system memory • Postprocessing of data from the external system memory • Post-filtering of data from the system memory with support of the MPEG-4 (both deblocking and deringing) and H.264 post-filtering algorithms • Displaying video and graphics on a synchronous (dumb or memory-less) display • Displaying video and graphics on an asynchronous (smart) display • Transferring data between IPU sub-modules and to/from the system memory with flexible pixel reformatting
KPP	Keypin port	ARM	Connectivity peripherals	Can be used for either keypin matrix scanning or general purpose I/O.
MLB	Media local bus	ARM	Connectivity peripherals	The MLB is designed to interface to an automotive MOST ring.
OSCAUD	OSC audio reference oscillator	Analog	Clock	The OSCAUDIO oscillator provides a stable frequency reference for the PLLs. This oscillator is designed to work in conjunction with an external 24.576-MHz crystal.

Table 4. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Domain[1]	Subsystem	Brief Description
OSC24M	OSC24M 24-MHz reference oscillator	Analog	Clock	The signal from the external 24-MHz crystal is the source of the CLK24M signal fed into USB PHY as the reference clock and to the real time clock (RTC).
MPLL PPLL	Digital phase-locked loops	SDMA	Clocks	DPLLs are used to generate the clocks: MCU PLL (MPLL)—programmable Peripheral PLL (PPLL)—programmable
PWM	Pulse-width modulator	ARM	ARM1136 platform peripherals	The pulse-width modulator (PWM) is optimized to generate sound from stored sample audio images; it can also generate tones.
RTC	Real-time clock	ARM	Clocks	Provides the ARM1136 platform with a clock function (days, hours, minutes, seconds) and includes alarm, sampling timer, and minute stopwatch capabilities.
SDMA	Smart DMA engine	SDMA	System controls	The SDMA provides DMA capabilities inside the processor. It is a shared module that implements 32 DMA channels and has an interface to connect to the ARM1136 platform subsystem, EMI interface, and the peripherals.
SJC	Secure JTAG controller	ARM	Pins	The secure JTAG controller (SJC) provides debug and test control with maximum security.
SPBA	SDMA peripheral bus arbiter	SDMA	System controls	The SPBA controls access to the SDMA peripherals. It supports shared peripheral ownership and access rights to an owned peripheral.
S/PDIF	Serial audio interface	SDMA	Connectivity peripherals	Sony/Philips digital transceiver interface
SSI(2)	Synchronous serial interface	SDMA, ARM(2)	Connectivity peripherals	The SSI is a full-duplex serial port that allows the processor connected to it to communicate with a variety of serial protocols, including the Freescale Semiconductor SPI standard and the I^2C sound (I^2S) bus standard. The SSIs interface to the AUDMUX for flexible audio routing.
UART(3)	Universal asynchronous receiver/transmitters	ARM (UART1,2) SDMA (UART3)	Connectivity peripherals	Each UART provides serial communication capability with external devices through an RS-232 cable using the standard RS-232 non-return-to-zero (NRZ) encoding format. Each module transmits and receives characters containing either 7 or 8 bits (program-selectable). Each UART can also provide low-speed IrDA compatibility through the use of external circuitry that converts infrared signals to electrical signals (for reception) or transforms electrical signals to signals that drive an infrared LED (for transmission).

Table 12. Thermal Resistance Data (continued)

Rating	Condition	Symbol	Value	Unit
Junction to ambient[1] (at 200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	44	ºC/W
Junction to ambient[1] (at 200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	27	ºC/W
Junction to boards[2]	—	$R_{\theta JB}$	19	ºC/W
Junction to case (top)[3]	—	$R_{\theta JCtop}$	10	ºC/W
Junction to package top[4]	Natural convection	Ψ_{JT}	2	ºC/W

1 Junction-to-ambient thermal resistance determined per JEDC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

2 Junction-to-board thermal resistance determined per JEDC JESD51-8. Thermal test board meets JEDEC specification for this package.

3 Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

4 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, this thermal characterization parameter is written as Psi-JT.

4.7 I/O Pin DC Electrical Characteristics

I/O pins are of two types: GPIO and DDR. DDR pins can be configured in three different drive strength modes: mobile DDR, SDRAM, and DDR2. The SDRAM and mobile DDR modes can be further customized at three drive strength levels: normal, high, and max.

Table 13 shows currents for the different DDR pin drive strength modes.

Table 13. DDR Pin Drive Strength Mode Current Levels

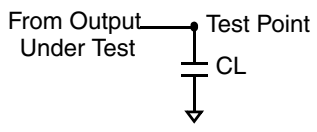
Drive Mode	Normal	High	Max.
Mobile DDR (1.8 V)	3.6 mA	7.2 mA	10.8 mA
SDRAM (1.8 V)	—	—	6.5 mA
SDRAM (3.3 V)	4 mA	8 mA	12 mA
DDR2 (1.8 V)	—	—	13.4 mA

Table 14. I/O Pin DC Electrical Characteristics (continued)

Pin	DC Electrical Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
SDR (1.8 V)	High-level output voltage	Voh	Ioh = 5.7 mA	OVDD – 0.28	—	—	V
	Low-level output voltage	Vol	Ioh = 5.7 mA	—	—	0.4	V
	High-level output current	Ioh	Max. drive	5.7	—	—	mA
	Low-level output current	Iol	Max. drive	7.3	—	—	mA
	High-level DC Input Voltage	VIH	—	1.4	—	1.98	V
	Low-level DC Input Voltage	VIL	—	–0.3	—	0.8	V
	Input current (no pull-up/down)	IIN	VI = 0 VI=NVCC	—	—	150 80	µA
	Tri-state I/O supply current	Icc (NVCC)	VI = OVDD or 0	—	—	1180	µA
	Tri-state core supply current	Icc (NVCC)	VI = VDD or 0	—	—	1220	µA
SDR (3.3 V)	High-level output voltage	Voh	Ioh=specified drive (Ioh = –4, –8, –12, –16 mA)	2.4	—	—	V
	Low-level output voltage	Vol	Ioh=specified drive (Ioh = 4, 8, 12, 16 mA)	—	—	0.4	V
	High-level output current	Ioh	Standard drive High drive Max. drive	–4.0 –8.0 –12.0	—	—	mA
	Low-level output current	Iol	Standard drive High drive Max. drive	4.0 8.0 12.0	—	—	mA
	High-level DC Input Voltage	VIH	—	2.0	—	3.6	V
	Low-level DC Input Voltage	VIL	—	–0.3V	—	0.8	V
	Input current (no pull-up/down)	IIN	VI = 0 VI = NVCC	—	—	±1	µA
	Tri-state I/O supply current	Icc (NVCC)	VI = NVCC or 0	—	—	±1	µA

4.8 I/O Pin AC Electrical Characteristics

Figure 5 shows the load circuit for output pins.



CL includes package, probe and jig capacitance

Figure 5. Load Circuit for Output Pin

Table 17. AC Electrical Characteristics of GPIO Pins in Slow Slew Rate Mode [NVCC = 1.65 V–1.95 V]

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	—	60	%
Output pin slew rate (max. drive)	tps	25 pF 50 pF	0.30/0.42 0.20/0.29	0.54/0.73 0.35/0.50	0.91/1.20 0.60/0.80	V/ns
Output pin slew rate (high drive)	tps	25 pF 50 pF	0.19/0.28 0.12/0.18	0.34/0.49 0.34/0.49	0.58/0/79 0.36/0.49	V/ns
Output pin slew rate (standard drive)	tps	25 pF 50 pF	0.12/0.18 0.07/0.11	0.20/0.30 0.11/0.17	0.34/0.47 0.20/0.27	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	7 7	21 22	56 58	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	5 5	14 15	38 40	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	2 2	7 7	18 19	mA/ns

Table 18. AC Electrical Characteristics of GPIO Pins in Fast Slew Rate Mode for [NVCC = 3.0 V–3.6 V]

Parameter	Symbol	Test Condition	Min. rise/fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	—	60	%
Output pin slew rate (max. drive)	tps	25 pF 50 pF	0.96/1.40 0.54/0.83	1.54/2.10 0.85/1.24	2.30/3.00 1.26/1.70	V/ns
Output pin slew rate (high drive)	tps	25 pF 50 pF	0.76/1.10 0.41/0.64	1.19/1.71 0.63/0.95	1.78/2.39 0.95/1.30	V/ns
Output pin slew rate (standard drive)	tps	25 pF 50 pF	0.52/0.78 0.28/0.44	0.80/1.19 0.43/0.64	1.20/1.60 0.63/0.87	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	46 49	108 113	250 262	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	35 37	82 86	197 207	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	22 23	52 55	116 121	mA/ns

Input data, $\overline{ECB}$ and $\overline{DTACK}$ all captured according to BCLK rising edge time. Figure 15 depicts the timing of the WEIM module, and Table 33 lists the timing parameters.

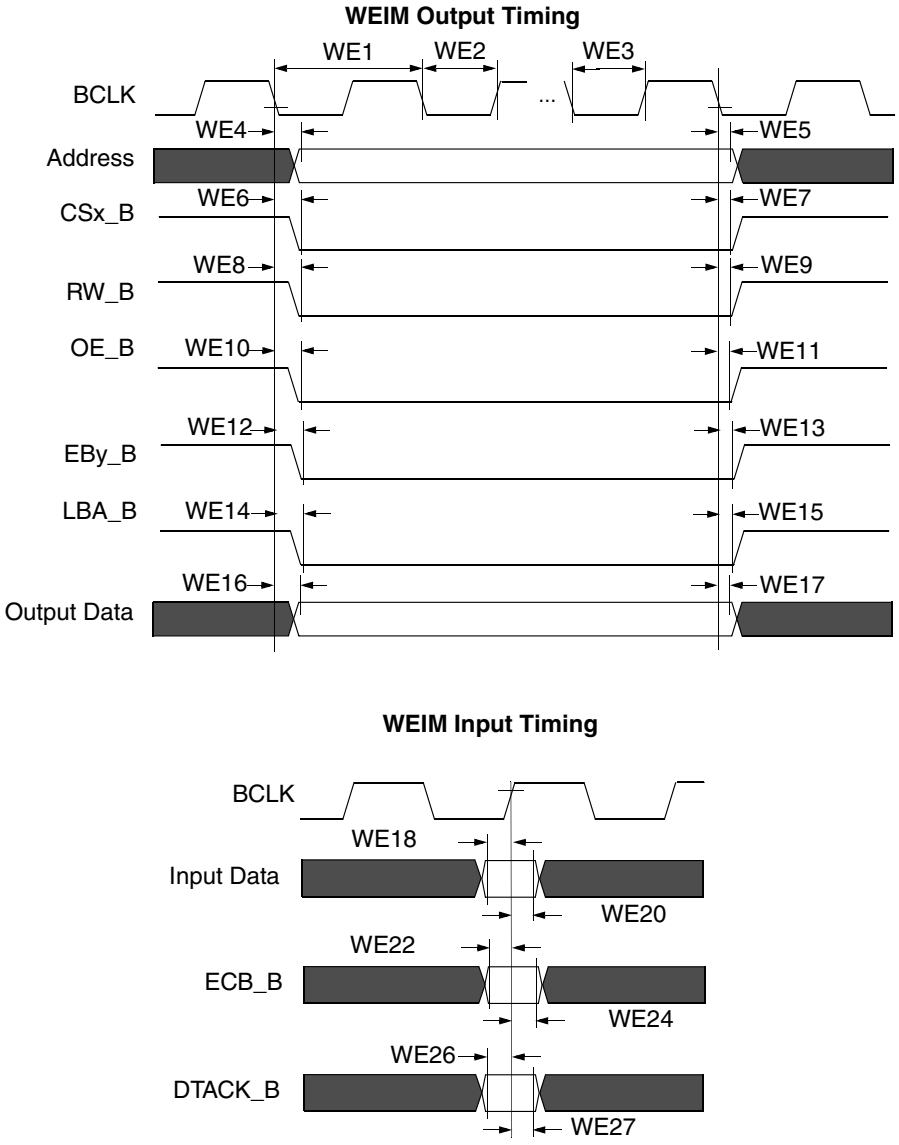


Figure 15. WEIM Bus Timing Diagram

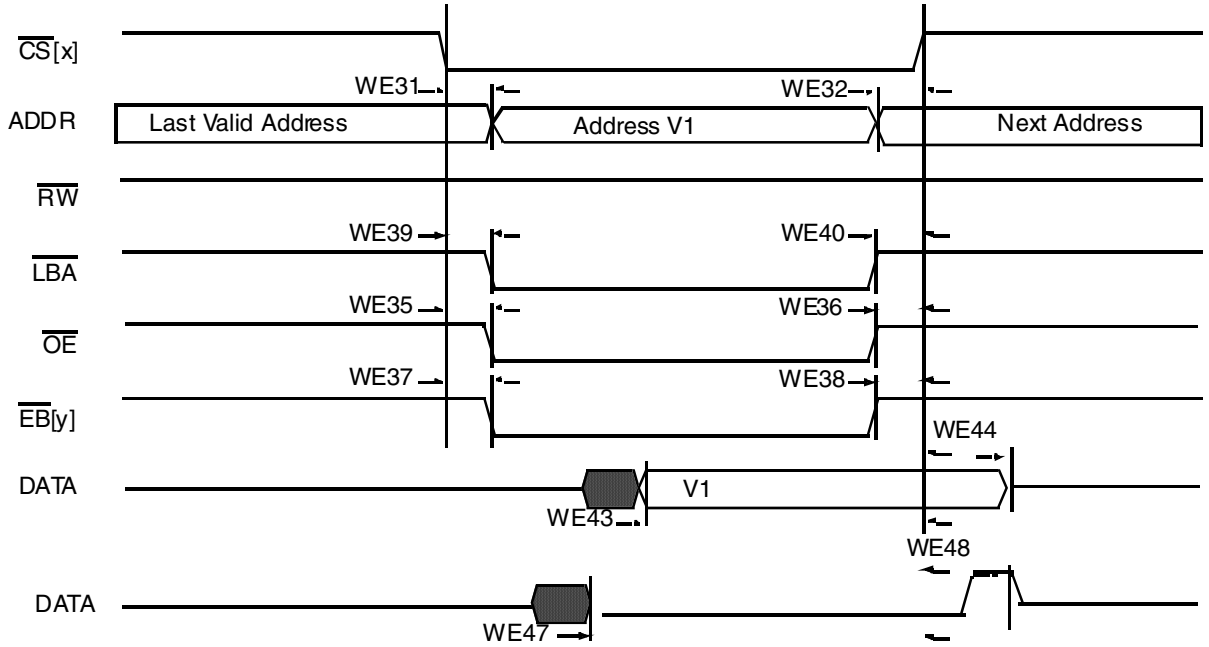


Figure 26. DTACK Read Access

Table 34. WEIM Asynchronous Timing Parameters Relative Chip Select Table

Ref No.	Parameter	Determination By Synchronous Measured Parameters[1]	Min	Max (If 133 MHz is supported by SoC)	Unit
WE31	$\overline{CS}$[x] valid to Address valid	WE4 – WE6 – CSA[2]	—	3 – CSA	ns
WE32	Address invalid to $\overline{CS}$[x] invalid	WE7 – WE5 – CSN[3]	—	3 – CSN	ns
WE32A(muxed A/D	$\overline{CS}$[x] valid to address invalid	WE4 – WE7 + (LBN + LBA + 1 – CSA[2])	–3 + (LBN + LBA + 1 – CSA)	—	ns
WE33	$\overline{CS}$[x] valid to $\overline{WE}$ valid	WE8 – WE6 + (WEA – CSA)	—	3 + (WEA – CSA)	ns
WE34	$\overline{WE}$ invalid to $\overline{CS}$[x] invalid	WE7 – WE9 + (WEN – CSN)	—	3 – (WEN_CSN)	ns
WE35	$\overline{CS}$[x] valid to $\overline{OE}$ valid	WE10 – WE6 + (OEA – CSA)	—	3 + (OEA – CSA)	ns
WE35A (muxed A/D)	$\overline{CS}$[x] valid to $\overline{OE}$ valid	WE10 – WE6 + (OEA + RLBN + RLBA + ADH + 1 – CSA)	–3 + (OEA + RLBN + RLBA + ADH + 1 – CSA)	3 + (OEA + RLBN + RLBA + ADH + 1 – CSA)	ns
WE36	$\overline{OE}$ invalid to $\overline{CS}$[x] invalid	WE7 – WE11 + (OEN – CSN)	—	3 – (OEN – CSN)	ns
WE37	$\overline{CS}$[x] valid to $\overline{BE}$[y] valid (read access)	WE12 – WE6 + (RBEA – CSA)	—	3 + (RBEA[4] – CSA)	ns
WE38	$\overline{BE}$[y] invalid to $\overline{CS}$[x] invalid (read access)	WE7 – WE13 + (RBEN – CSN)	—	3 – (RBEN[5] – CSN)	ns
WE39	$\overline{CS}$[x] valid to $\overline{LBA}$ valid	WE14 – WE6 + (LBA – CSA)	—	3 + (LBA – CSA)	ns
WE40	$\overline{LBA}$ invalid to $\overline{CS}$[x] invalid	WE7 – WE15 – CSN	—	3 – CSN	ns

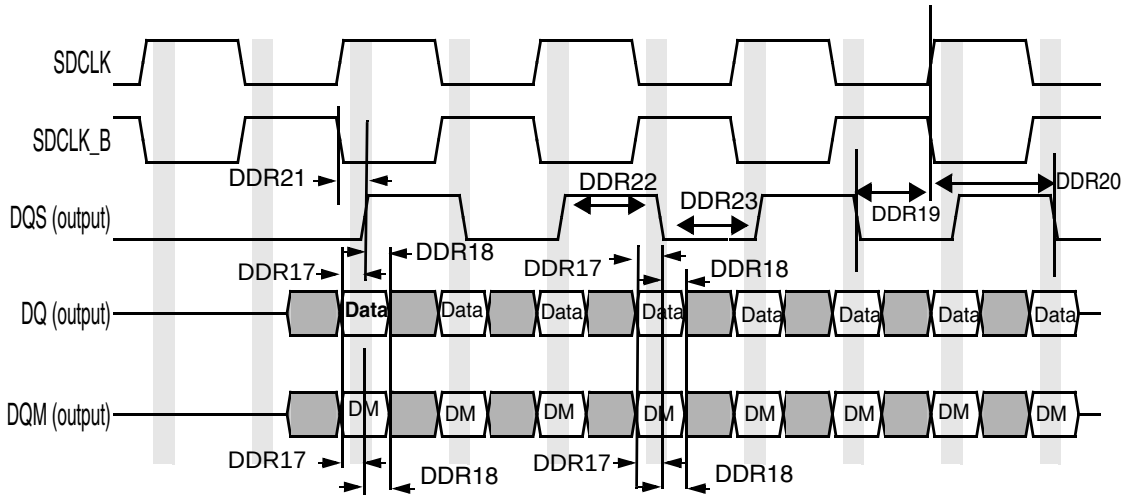


Figure 32. DDR2 SDRAM Write Cycle Timing Diagram

Table 41. DDR2 SDRAM Write Cycle Parameters

ID	PARAMETER	Symbol	DDR2-400		Unit
			Min	Max	
DDR17	DQ and DQM setup time to DQS (single-ended strobe)	$t_{DS1(base)}$	0.5	—	ns
DDR18	DQ and DQM hold time to DQS (single-ended strobe)	$t_{DH1(base)}$	0.5	—	ns
DDR19	Write cycle DQS falling edge to SDCLK output setup time.	t_{DSS}	0.2	—	tCK
DDR20	Write cycle DQS falling edge to SDCLK output hold time.	t_{DSH}	0.2	—	tCK
DDR21	DQS latching rising transitions to associated clock edges	t_{DQSS}	–0.25	0.25	tCK
DDR22	DQS high level width	t_{DQSH}	0.35	—	tCK
DDR23	DQS low level width	t_{DQSL}	0.35	—	tCK

NOTE

These values are for DQ/DM slew rate of 1 V/ns and DQS slew rate of 1 V/ns. For different values use the derating table.

4.9.6 Enhanced Serial Audio Interface (ESAI) Timing Specifications

The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. Table 46 shows the interface timing values. The number field in the table refers to timing signals found in Figure 36 and Figure 37.

Table 46. Enhanced Serial Audio Interface Timing

No.	Characteristics[1,2]	Symbol	Expression[2]	Min.	Max.	Condition[3]	Unit
62	Clock cycle[4]	t_{SSICC}	$4 \times T_C$ $4 \times T_C$	30.0 30.0	— —	i ck i ck	ns
63	Clock high period • For internal clock • For external clock	— —	$2 \times T_C - 9.0$ $2 \times T_C$	6 15	— —	— —	ns
64	Clock low period • For internal clock • For external clock	— —	$2 \times T_C - 9.0$ $2 \times T_C$	6 15	— —	— —	ns
65	SCKR rising edge to FSR out (bl) high	— —	— —	— —	17.0 7.0	x ck i ck a	ns
66	SCKR rising edge to FSR out (bl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
67	SCKR rising edge to FSR out (wr) high[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
68	SCKR rising edge to FSR out (wr) low[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
69	SCKR rising edge to FSR out (wl) high	— —	— —	— —	16.0 6.0	x ck i ck a	ns
70	SCKR rising edge to FSR out (wl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
71	Data in setup time before SCKR (SCK in synchronous mode) falling edge	— —	— —	12.0 19.0	— —	x ck i ck	ns
72	Data in hold time after SCKR falling edge	— —	— —	3.5 9.0	— —	x ck i ck	ns
73	FSR input (bl, wr) high before SCKR falling edge[5]	— —	— —	2.0 12.0	— —	x ck i ck a	ns
74	FSR input (wl) high before SCKR falling edge	— —	— —	2.0 12.0	— —	x ck i ck a	ns
75	FSR input hold time after SCKR falling edge	— —	— —	2.5 8.5	— —	x ck i ck a	ns
78	SCKT rising edge to FST out (bl) high	— —	— —	— —	18.0 8.0	x ck i ck	ns
79	SCKT rising edge to FST out (bl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns

inserted in between EAV and SAV code. The CSI decodes and filters out the timing coding from the data stream, thus recovering SENSB_VSYNC and SENSB_HSYNC signals for internal use.

4.9.12.2.2 Gated Clock Mode

The SENSB_VSYNC, SENSB_HSYNC, and SENSB_PIX_CLK signals are used in this mode. See Figure 44.

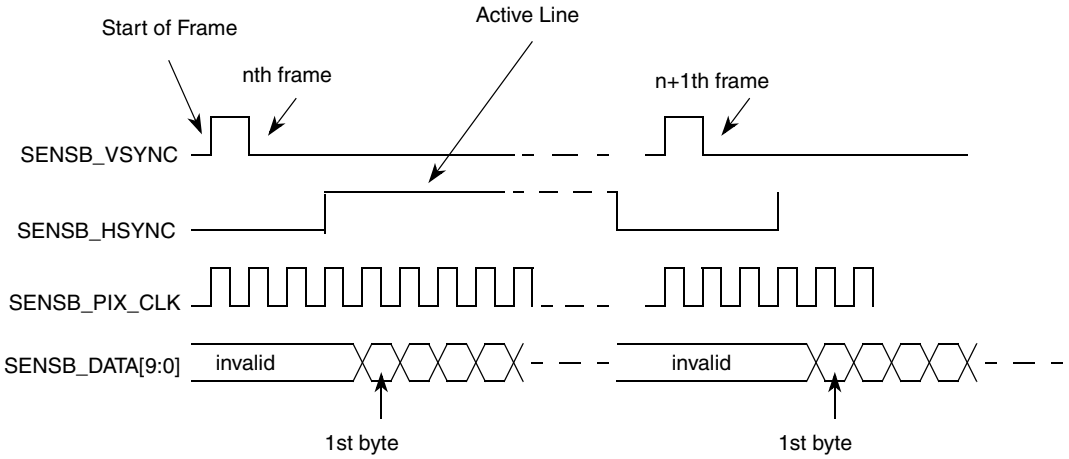


Figure 44. Gated Clock Mode Timing Diagram

A frame starts with a rising edge on SENSB_VSYNC (all the timing corresponds to straight polarity of the corresponding signals). Then SENSB_HSYNC goes to high and hold for the entire line. The pixel clock is valid as long as SENSB_HSYNC is high. Data is latched at the rising edge of the valid pixel clocks. SENSB_HSYNC goes to low at the end of the line. Pixel clocks then become invalid and the CSI stops receiving data from the stream. For the next line, the SENSB_HSYNC timing repeats. For the next frame, the SENSB_VSYNC timing repeats.

4.9.12.2.3 Non-Gated Clock Mode

The timing is the same as the gated-clock mode (described in Section 4.9.12.2.2, “Gated Clock Mode”), except for the SENSB_HSYNC signal, which is not used. See Figure 45. All incoming pixel clocks are valid and will cause data to be latched into the input FIFO. The SENSB_PIX_CLK signal is inactive (states low) until valid data is going to be transmitted over the bus.

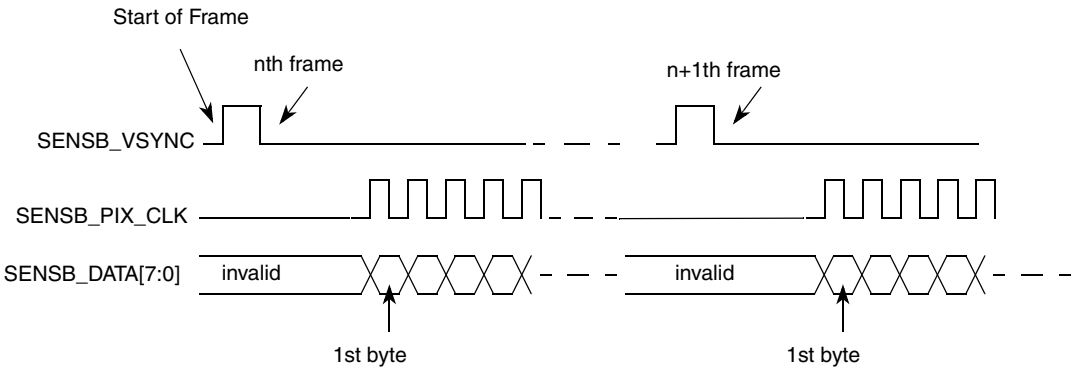


Figure 45. Non-Gated Clock Mode Timing Diagram

4.9.13.1 Synchronous Interfaces

This section discusses the interfaces to active matrix TFT LCD panels, Sharp HR-TFT, and dual-port smart displays.

4.9.13.1.4 Interface to Active Matrix TFT LCD Panels, Functional Description

Figure 47 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure, signals are shown with negative polarity. The sequence of events for active matrix interface timing is as follows:

- DISPB_D3_CLK latches data into the panel on its negative edge (when positive polarity is selected). In active mode, DISPB_D3_CLK runs continuously.
- DISPB_D3_HSYNC causes the panel to start a new line.
- DISPB_D3_VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse.
- DISPB_D3_DRDY acts like an output enable signal to the CRT display. This output enables the data to be shifted to the display. When disabled, the data is invalid and the trace is off.

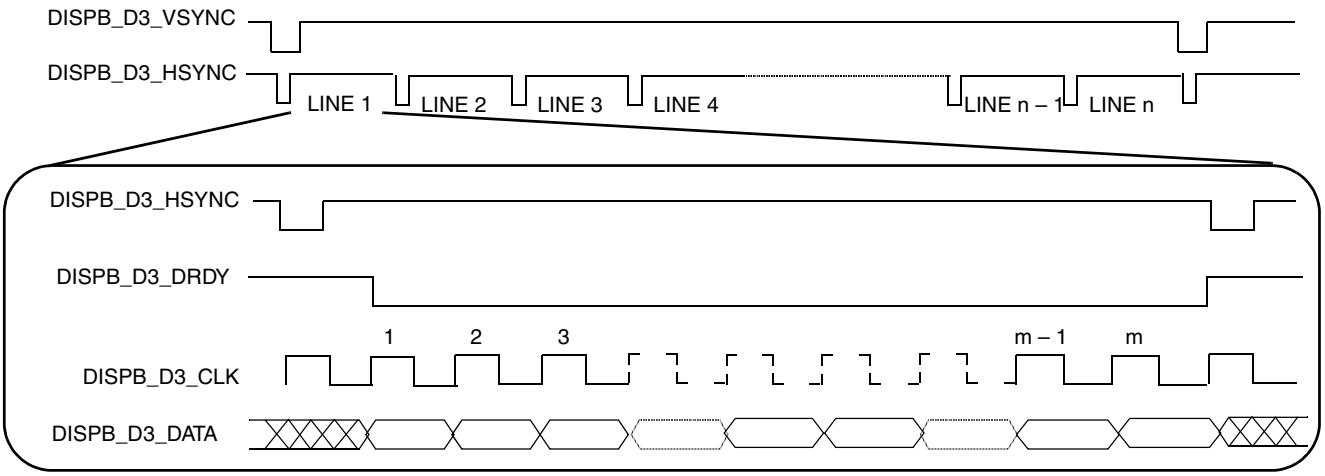


Figure 47. Interface Timing Diagram for TFT (Active Matrix) Panels

4.9.13.1.5 Interface to Active Matrix TFT LCD Panels, Electrical Characteristics

Figure 48 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and the data. All figure parameters shown are programmable. The timing images correspond to inverse polarity

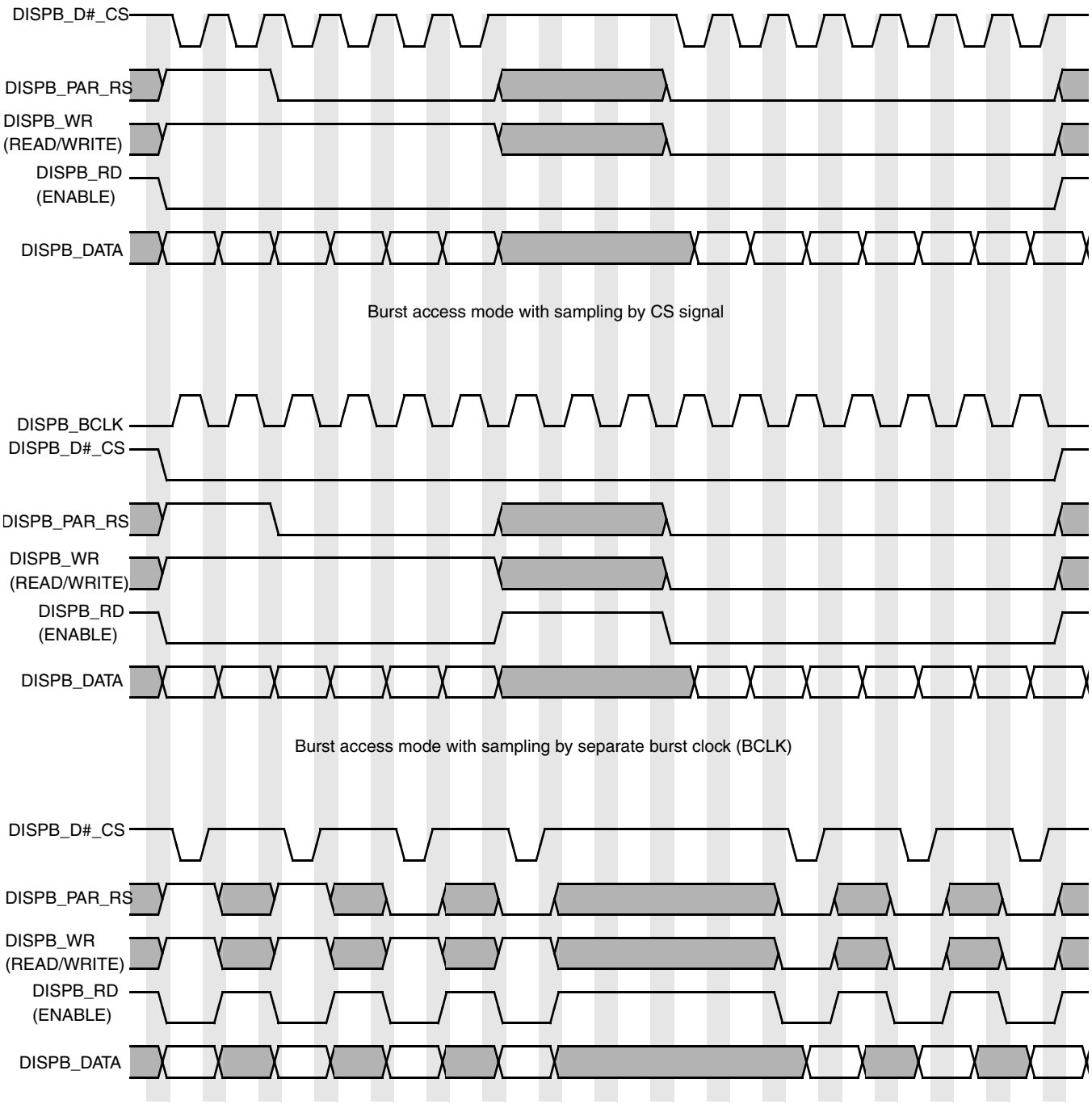


Figure 55. Asynchronous Parallel System 68k Interface (Type 1) Burst Mode Timing Diagram

Figure 71 depicts write 0 sequence timing, and Table 65 lists the timing parameters.

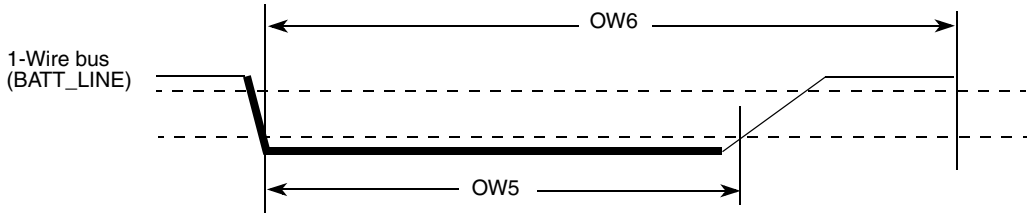


Figure 71. Write 0 Sequence Timing Diagram

Table 65. WR0 Sequence Timing Parameters

ID	Parameter	Symbol	Min.	Typ.	Max.	Units
OW5	Write 0 low time	t_{WR0_low}	60	100	120	µs
OW6	Transmission time slot	t_{SLOT}	OW5	117	120	µs

Figure 72 shows write 1 sequence timing, and Figure 73 depicts the read sequence timing. Table 66 lists the timing parameters.

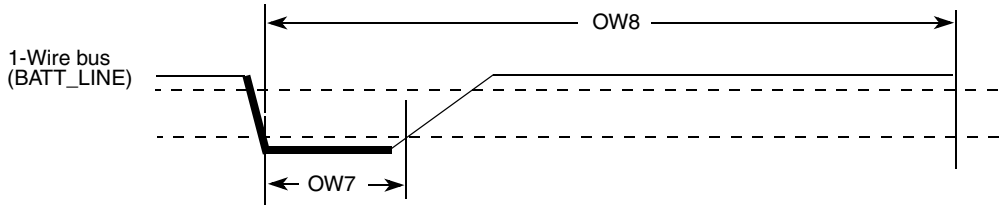


Figure 72. Write 1 Sequence Timing Diagram

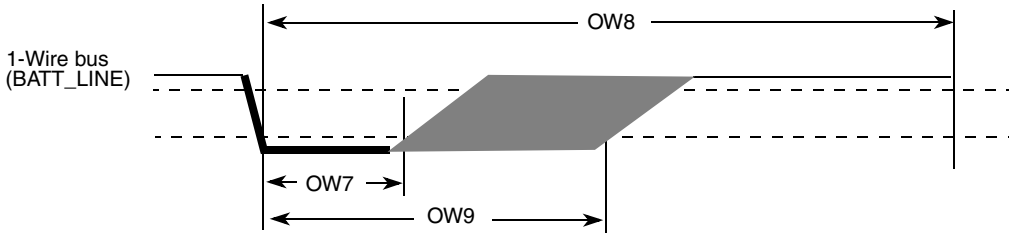


Figure 73. Read Sequence Timing Diagram

Table 66. WR1/RD Timing Parameters

ID	Parameter	Symbol	Min.	Typ.	Max.	Units
OW7	Write 1/read low time	t_{LOW1}	1	5	15	µs
OW8	Transmission time slot	t_{SLOT}	60	117	120	µs
OW9	Release time	$t_{RELEASE}$	15	—	45	µs

4.9.17.6 UDMA-Out Timing

Figure 82 shows timing when the UDMA-out transfer starts, Figure 83 shows timing when the UDMA-out host terminates transfer, Figure 84 shows timing when the UDMA-out device terminates transfer, and Table 73 lists the timing parameters for the UDMA-out burst.

Figure 82. UDMA-Out Transfer Starts Timing Diagram

Figure 83. UDMA-Out Host Terminates Transfer Timing Diagram

Table 84. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA3	Transmit bit time in IrDA mode	t_{TIRbit}	$1/F_{baud\_rate}$[1] – T_{ref_clk}[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—
UA4	Transmit IR pulse duration	$t_{TIRpulse}$	$(3/16) \times (1/F_{baud\_rate}) - T_{ref\_clk}$	$(3/16) \times (1/F_{baud\_rate}) + T_{ref\_clk}$	—

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.9.23.2.14 UART IrDA Mode Receiver

Figure 99 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 85 lists the receive timing characteristics.

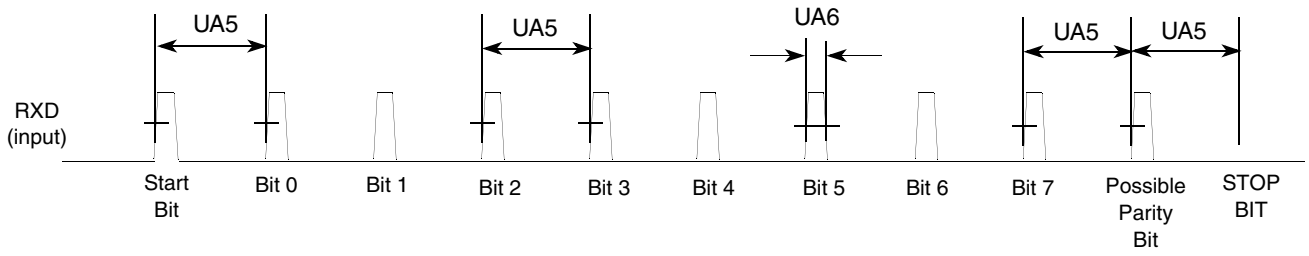


Figure 99. UART IrDA Mode Receive Timing Diagram

Table 85. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA5	Receive bit time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud\_rate}$[2] – $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—
UA6	Receive IR pulse duration	$t_{RIRpulse}$	1.41 us	$(5/16) \times (1/F_{baud\_rate})$	—

1 The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency) ÷ 16.

4.9.24 USB Electrical Specifications

In order to support four different serial interfaces, the USB serial transceiver can be configured to operate in one of four modes:

- DAT_SE0 bidirectional, 3-wire mode
- DAT_SE0 unidirectional, 6-wire mode
- VP_VM bidirectional, 4-wire mode
- VP_VM unidirectional, 6-wire mode

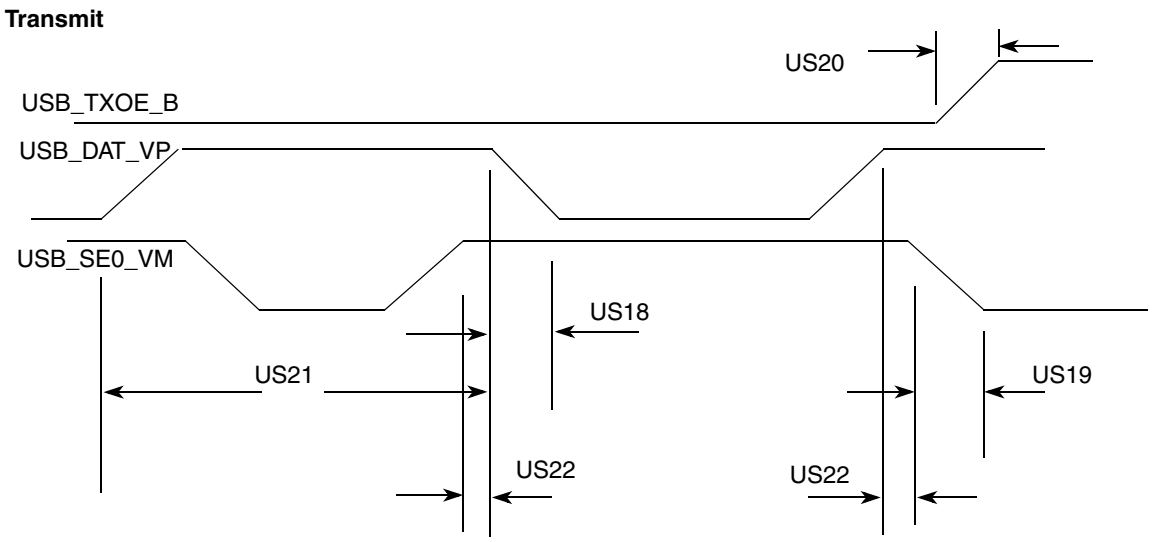


Figure 104. USB Transmit Waveform in VP_VM Bidirectional Mode

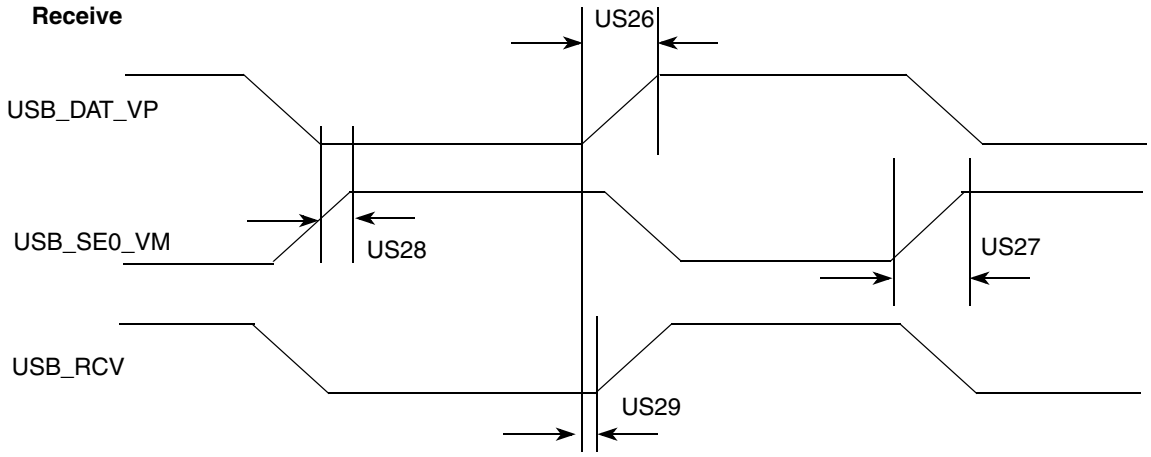


Figure 105. USB Receive Waveform in VP_VM Bidirectional Mode

Table 91 describes the port timing specification in VP_VM bidirectional mode.

Table 91. USB Port Timing Specification in VP_VM Bidirectional Mode

No.	Parameter	Signal Name	Direction	Min.	Max.	Unit	Condition/ Reference Signal
US18	Tx rise/fall time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US19	Tx rise/fall time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US20	Tx rise/fall time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US21	Tx duty cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US22	Tx overlap	USB_SE0_VM	Out	–3.0	+3.0	ns	USB_DAT_VP
US26	Rx rise/fall time	USB_DAT_VP	In	—	3.0	ns	35 pF
US27	Rx rise/fall time	USB_SE0_VM	In	—	3.0	ns	35 pF

Table 91. USB Port Timing Specification in VP_VM Bidirectional Mode (continued)

No.	Parameter	Signal Name	Direction	Min.	Max.	Unit	Condition/ Reference Signal
US28	Rx skew	USB_DAT_VP	In	–4.0	+4.0	ns	USB_SE0_VM
US29	Rx skew	USB_RCV	In	–6.0	+2.0	ns	USB_DAT_VP

4.9.24.4 VP_VM Unidirectional Mode

Table 92 defines the signals for VP_VM unidirectional mode. Figure 106 and Figure 107 show the transmit and receive waveforms respectively.

Table 92. Signal Definitions—VP_VM Unidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out	Tx VP data when USB_TXOE_B is low
USB_SE0_VM	Out	Tx VM data when USB_TXOE_B is low
USB_VP1	In	Rx VP data when USB_TXOE_B is high
USB_VM1	In	Rx VM data when USB_TXOE_B is high
USB_RCV	In	Differential Rx data

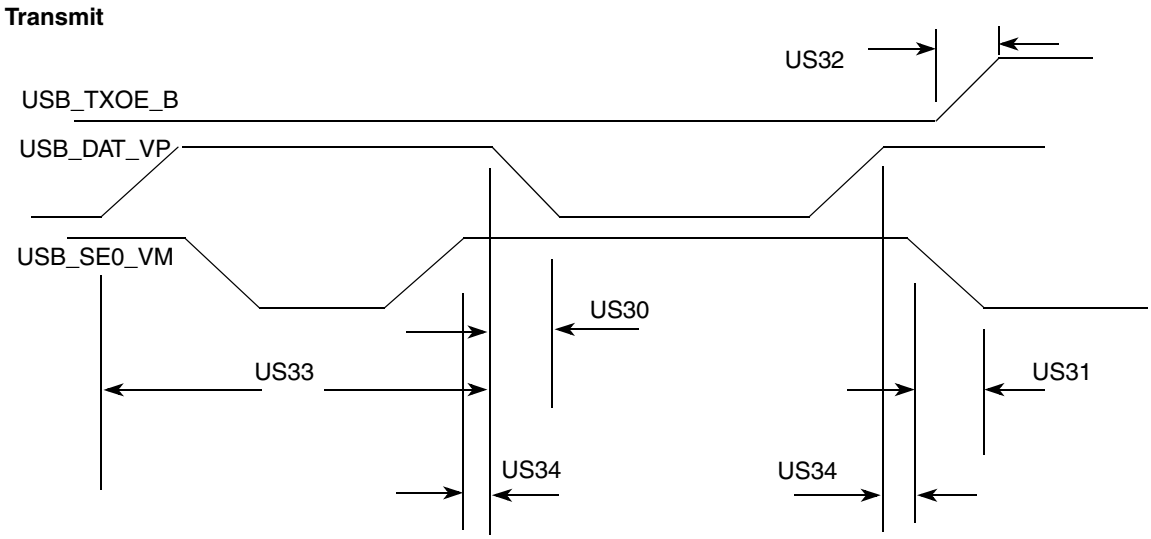


Figure 106. USB Transmit Waveform in VP_VM Unidirectional Mode

5.2 MAPBGA Signal Assignments

Table 94 and Table 95 list MAPBGA signals, alphabetized by signal name, for silicon revisions 2.0 and 2.1, respectively. Table 96 and Table 97 show the signal assignment on the i.MX35 ball map for silicon revisions 2.0 and 2.1, respectively. The ball map for silicon revision 2.1 is different than the ballmap for silicon revision 2.0. The layout for each revision is not compatible, so it is important that the correct ballmap be used to implement the layout.

Table 94. Silicon Revision 2.0 Signal Ball Map Locations

Signal ID	Ball Location
A0	A5
A1	D7
A10	F15
A11	D5
A12	F6
A13	B3
A14	D14
A15	D15
A16	D13
A17	D12
A18	E11
A19	D11
A2	E7
A20	D10
A21	E10
A22	D9
A23	E9
A24	D8
A25	E8
A3	C6
A4	D6
A5	B5
A6	C5
A7	A4
A8	B4
A9	A3
ATA_BUFF_EN[1]	T5
ATA_CS0[1]	V7
ATA_CS1[1]	T7
ATA_DA0[1]	R4
ATA_DA1[1]	V1
ATA_DA2[1]	R5
ATA_DATA0[1]	Y5
ATA_DATA1[1]	W5
ATA_DATA10[1]	V3
ATA_DATA11[1]	Y2
ATA_DATA12[1]	U3

Signal ID	Ball Location
ATA_DATA7[1]	Y3
ATA_DATA8[1]	U4
ATA_DATA9[1]	W3
ATA_DIOR[1]	Y6
ATA_DIOW[1]	W6
ATA_DMACK[1]	V6
ATA_DMARQ[1]	T3
ATA_INTRQ[1]	V2
ATA_IORDY[1]	U6
ATA_RESET_B[1]	T6
BCLK	E14
BOOT_MODE0	W10
BOOT_MODE1	U9
CAPTURE	V12
CAS	E16
CLK_MODE0	Y10
CLK_MODE1	T10
CLKO	V10
COMPARE	T12
CONTRAST[1]	L16
CS0	F17
CS1	E19
CS2	B20
CS3	C19
CS4	E18
CS5	F19
CSI_D10[1]	V16
CSI_D11[1]	T15
CSI_D12[1]	W16
CSI_D13[1]	V15
CSI_D14[1]	U14
CSI_D15[1]	Y16
CSI_D8[1]	U15
CSI_D9[1]	W17
CSI_HSYNC[1]	V14
CSI_MCLK[1]	W15
CSI_PIXCLK[1]	Y15

Table 96. Silicon Revision 2.0 Ball Map—17 x 17, 0.8 mm Pitch[1]

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	VSS	D0	A9	A7	A0	SDBA0	SD30	SD27	SD24	SDQS2	SD21	SD18	SDQS1	SD14	SD10	SD9	SD6	SD4	SD1	VSS	A
B	D5	D2	A13	A8	A5	SDBA1	SD31	SD28	SD26	SD23	SD20	SD19	SD15	SD13	SD11	SD7	SDQS0	SD2	DQM0	CS2	B
C	D8	D7	D4	MA10	A6	A3	SDQS3	SD29	SD25	SD22	SD17	SD16	SD12	SD8	SD5	SD3	SD0	DQM3	CS3	RW	C
D	D14	D10	D6	D1	A11	A4	A1	A24	A22	A20	A19	A17	A16	A14	A15	DQM2	DQM1	SDCKE0	ECB	LBA	D
E	NFCLE	D15	D12	D9	D3	D11	A2	A25	A23	A21	A18	SDCLK	SDCLK_B	BCLK	RAS	CAS	SDCKE1	CS4	CS1	OE	E
F	NFRE_B	NFALE	NFRB	NFWP_B	D13	A12	VDD	VDD	VDD	NVCC_EMI1	NVCC_EMI1	VDD	NVCC_EMI2	NVCC_EMI2	A10	EB1	CS0	EB0	CS5	LD0	F
G	RTS2	NFWE_B	NF_CE0	TX0	CTS2	NVCC_NFC	NVCC_EMI1	NVCC_EMI1	NVCC_EMI1	NVCC_EMI1	NVCC_EMI1	NVCC_EMI2	VDD	NVCC_EMI3	SDWE	LD3	LD2	LD1	LD4	LD7	G
H	TX1	TXD2	RXD2	TX4_RX1	TX2_RX3	NVCC_NFC	NVCC_NFC	NGND_EMI1	NVCC_EMI1	NGND_EMI1	VSS	VSS	VSS	NVCC_LCDC	VDD	LD5	LD8	LD6	LD9	LD10	H
J	FST	TX3_RX2	TX5_RX0	SCKT	HCKT	STXFS5	VDD	VSS	VSS	NGND_EMI1	NGND_EMI2	NGND_EMI3	VSS	NVCC_LCDC	VDD	LD12	LD14	LD11	LD13	LD15	J
K	STXD5	HCKR	SCKR	SRXD5	FSR	NVCC_MISC	NVCC_MISC	NGND_MISC	NGND_NFC	VSS	NGND_LCDC	NGND_EMI3	VSS	LD16	LD22	LD20	LD21	LD18	LD17	LD19	K
L	SRXD4	STXFS4	I2C2_CLK	SCK4	SCK5	FEC_TDATA3	VDD	NVCC_MISC	VSS	NGND_ATA	NGND_CRM	NGND_LCDC	VSS	NVCC_LCDC	D3_FPSHIFT	CONTRAST	D3_CLS	D3_HSYNC	LD23	D3_DRDY	L
M	I2C2_DAT	STXD4	FEC_RDATA2	FEC_TDATA1	FEC_TDATA2	VDD	NGND_MISC	VSS	NGND_ATA	NGND_MLB	FUSE_VSS	PGND	NGND_JTAG	NVCC_LCDC	PHY1_VDDA	TTM_PIN	D3_REV	D3_SPL	D3_VSYNC	I2C1_CLK	M
N	FEC_RDATA3	FEC_RDATA1	FEC_RX_ERR	FEC_TX_ERR	FEC_CRS	NVCC_ATA	VDD	VSS	VSS	NGND_CSI	MGND	NGND_SDIO	PVDD	USBPHY1_UPLLGND	USBPHY1_UPLLVDD	PHY1_VSSA	I2C1_DAT	USBPHY1_UID	USBPHY1_DM	PHY1_VDDA	N
P	FEC_MDIO	FEC_RDATA0	FEC_COL	FEC_TX_CLK	FEC_TDATA0	NVCC_ATA	NVCC_ATA	NVCC_ATA	NGND_ATA	VSS	MVDD	PHY2_VSS	FUSE_VDD	NVCC_SDIO	TDI	NVCC_JTAG	USBPHY1_UPLLVDD	USBPHY1_VBUS	USBPHY1_DP	PHY1_VSSA	P
R	FEC_MDC	FEC_RX_CLK	CTS1	ATA_DA0	ATA_DA2	TXD1	VDD	VDD	NVCC_CRM	NVCC_MLB	NVCC_CSI	VDD	PHY2_VDD	SD1_DATA0	TDO	TMS	TCK	USBPHY1_VSSA_BIAS	USBPHY1_RREF	USBPHY1_VDDA_BIAS	R
T	FEC_TX_EN	FEC_RX_DV	ATA_DMARQ	ATA_DATA15	ATA_BUFF_EN	ATA_RESET_B	ATA_CS1	CSPI1_SPI_RDY	VSTBY	CLK_MODE1	GPIO1_0	COMPARE	SD2_DATA1	CSI_VSYNC	CSI_D11	TRSTB	VSS	OSC24M_VSS	OSC24M_VDD	EXTAL24M	T
U	RTS1	RXD1	ATA_DATA12	ATA_DATA8	ATA_DATA3	ATA_IORDY	USBOTG_OC	CSPI1_SS1	BOOT_MODE1	RESET_IN_B	GPIO2_0	SD2_DATA3	SD2_CMD	CSI_D14	CSI_D8	SD1_DATA1	SJC_MOD	RTCK	OSC_AUDIO_VSS	XTAL24M	U

Table 97. Silicon Revision 2.1 Ball Map—17 x 17, 0.8 mm Pitch (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
P	FEC_MDIO	FEC_RDATA0	FEC_COL	FEC_TX_CLK	FEC_TDATA0	NVCC_ATA	NVCC_ATA	NVCC_ATA	GND	GND	MVDD	PHY2_VSS	FUSE_VDD	NVCC_SDIO	TDI	NVCC_JTAG	USBPHY1_UPLLVDD	USBPHY1_VBUS	USBPHY1_DP	PHY1_VSSA	P
R	FEC_MDC	FEC_RX_CLK	CTS1	ATA_DA0	ATA_DA2	TXD1	VDD3	VDD3	NVCC_CRM	NVCC_MLB	NVCC_CSI	VDD4	PHY2_VDD	SD1_DATA0	TDO	TMS	TCK	USBPHY1_VSSA_BIAS	USBPHY1_REF	USBPHY1_VDDA_BIAS	R
T	FEC_TX_EN	FEC_RX_DV	ATA_DMARQ	ATA_DATA15	ATA_BUFF_EN	ATA_RESET_B	ATA_CS1	CSPI1_SPI_RDY	VSTBY	CLK_MODE1	GPIO1_0	COMPARE	SD2_DATA1	CSI_VSYNC	CSI_D11	TRSTB	GND	OSC24M_VSS	OSC24M_VDD	EXTAL24M	T
U	RTS1	RXD1	ATA_DATA12	ATA_DATA8	ATA_DATA3	ATA_IORDY	USBOTG_OC	CSPI1_SS1	BOOT_MODE1	RESET_IN_B	GPIO2_0	SD2_DATA3	SD2_CMD	CSI_D14	CSI_D8	SD1_DATA1	SJC_MOD	RTCK	OSC_AUDIO_VSS	XTAL24M	U
V	ATA_DA1	ATA_INTRQ	ATA_DATA10	ATA_DATA6	ATA_DATA2	ATA_DMACK	ATA_CS0	EXT_ARMCLK	CSPI1_MISO	CLKO	GPIO3_0	CAPTURE	SD2_DATA0	CSI_HSYNC	CSI_D13	CSI_D10	SD1_DATA3	SD1_CLK	XTAL_AUDIO	OSC_AUDIO_VDD	V
W	ATA_DATA14	ATA_DATA13	ATA_DATA9	ATA_DATA5	ATA_DATA1	ATA_DIOW	USBOTG_PWR	CSPI1_SCLK	CSPI1_MOSI	BOOT_MODE0	POR_B	MLB_SIG	MLB_CLK	SD2_CLK	CSI_MCLK	CSI_D12	CSI_D9	SD1_DATA2	DE_B	EXTAL_AUDIO	W
Y	GND	ATA_DATA11	ATA_DATA7	ATA_DATA4	ATA_DATA0	ATA_DIOR	TEST_MODE	CSPI1_SS0	POWER_FAIL	CLK_MODE0	GPIO1_1	WDOG_RST	MLB_DAT	SD2_DATA2	CSI_PIXCLK	CSI_D15	USBPHY2_DM	USBPHY2_DP	SD1_CMD	GND	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

6 Product Documentation

All related product documentation for the i.MX35 processor is located at http://www.freescale.com/imx.