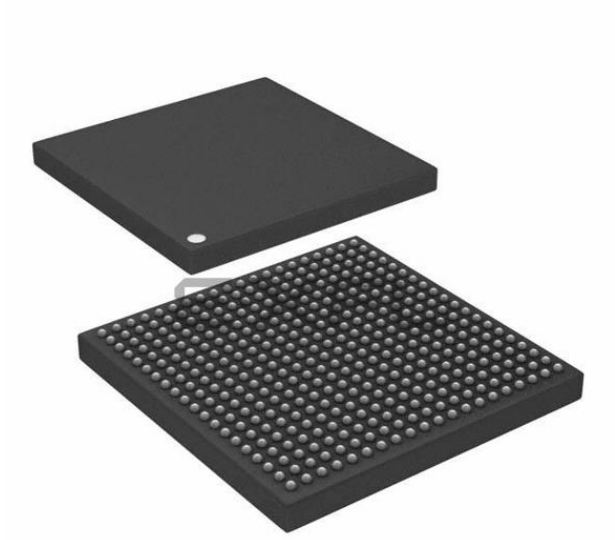

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Multimedia; IPU, VFP
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad, KPP, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Secure Fusebox, Secure JTAG
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx355avm4br2

- Branch prediction with return stack
- Low-interrupt latency
- Instruction and data memory management units (MMUs), managed using micro TLB structures backed by a unified main TLB
- Instruction and data L1 caches, including a non-blocking data cache with hit-under-miss
- Virtually indexed/physically addressed L1 caches
- 64-bit interface to both L1 caches
- Write buffer (bypassable)
- High-speed Advanced Micro Bus Architecture (AMBA)™ L2 interface
- Vector floating point co-processor (VFP) for 3D graphics and hardware acceleration of other floating-point applications
- ETM™ and JTAG-based debug support

Table 3 summarizes information about the i.MX35 core.

Table 3. i.MX35 Core

Core Acronym	Core Name	Brief Description	Integrated Memory Features
ARM11 or ARM1136	ARM1136 Platform	The ARM1136™ platform consists of the ARM1136JF-S core, the ETM real-time debug modules, a 6 × 5 multi-layer AHB crossbar switch (MAX), and a vector floating processor (VFP). The i.MX35 provides a high-performance ARM11 microprocessor core and highly integrated system functions. The ARM Application Processor (AP) and other subsystems address the needs of the personal, wireless, and portable product market with integrated peripherals, advanced processor core, and power management capabilities.	• 16-Kbyte instruction cache • 16-Kbyte data cache • 128-Kbyte L2 cache • 32-Kbyte ROM • 128-Kbyte RAM

2.5 Module Inventory

Table 4 shows an alphabetical listing of the modules in the MCIMX35. For extended descriptions of the modules, see the MCIMX35 reference manual.

Table 4. Digital and Analog Modules

Block Mnemonic	Block Name	Domain[1]	Subsystem	Brief Description
1-WIRE	1-Wire interface	ARM	ARM1136 platform peripherals	1-Wire provides the communication line to a 1-Kbit add-only memory. the interface can send or receive 1 bit at a time.
ASRC	Asynchronous sample rate converter	SDMA	Connectivity peripherals	The ASRC is designed to convert the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. It supports a concurrent sample rate conversion of about –120 dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates.

4 Electrical Characteristics

The following sections provide the device-level and module-level electrical characteristics for the i.MX35 processor.

4.1 i.MX35 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

Table 6. i.MX35 Chip-Level Conditions

Characteristics	Table/Location
Absolute Maximum Ratings	Table 7 on page 13
i.MX35 Operating Ranges	Table 8 on page 14
Interface Frequency	Table 9 on page 15

Stresses beyond those listed in Table 7 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in Table 8 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 7. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply voltage (core)	VDD_{max}[1]	–0.5	1.47	V
Supply voltage (I/O)	$NVCC_{max}$	–0.5	3.6	V
Input voltage range	V_{Imax}	–0.5	3.6	V
Storage temperature	$T_{storage}$	–40	125	°C
ESD damage immunity:	V_{esd}			V
Human Body Model (HBM)		—	2000[2]	
Charge Device Model (CDM)		—	500[3]	

1 VDD is also known as QVCC.

2 HBM ESD classification level according to the AEC-Q100-002 standard

3 Corner pins max. 750 V

4.1.2 Interface Frequency Limits

Table 9 provides information on interface frequency limits.

Table 9. Interface Frequency

ID	Parameter	Symbol	Min.	Typ.	Max.	Units
1	JTAG TCK Frequency	f_{JTAG}	DC	5	10	MHz

4.2 Power Modes

Table 10 provides descriptions of the power modes of the i.MX35 processor.

Table 10. i.MX35 Power Modes

Power Mode	Description	QVCC (ARM/L2 Peripheral)		MVDD/PVDD		OSC24M_VDD OSC_AUDO_VDD	
		Typ.	Max.	Typ.	Max.	Typ.	Max.
Wait	VDD1,2,3,4 = 1.1 V (min.) ARM is in wait for interrupt mode. MAX is active. L2 cache is kept powered. MCU PLL is on (400 MHz) PER PLL is off (can be configured) (default: 300 MHz) Module clocks are gated off (can be configured by CGR register). OSC 24M is ON. OSC audio is off (can be configured). RNGC internal osc is off.	16 mA	170 mA	7.2 mA	14 mA	1.2 mA	3 mA
Doze	VDD1,2,3,4 = 1.1 V (min.) ARM is in wait for interrupt mode. MAX is halted. L2 cache is kept powered. L2 cache control logic off. AWB enabled. MCU PLL is on(400 MHz) PER PLL is off (can be configured). (300 Mhz). Module clocks are gated off (can be configured by CGR register). OSC 24M is ON. OSC audio is off (can be configured) RNGC internal osc is off	12.4 mA	105 mA	7.2 mA	14 mA	1.2 mA	3 mA

Table 11. Power Consumption

Power Supply	Voltage (V)	Max Current (mA)
QVCC	1.47	400
MVDD, PVDD	1.65	20
NVCC_EMI1, NVCC_EMI2, NVCC_EMI3, NVCC_LCDC, NVCC_NFC	1.9	90
FUSE_VDD[1]	3.6	62
NVCC_MISC, NVCC_CSI, NVCC_SDIO, NVCC_CRM, NVCC_ATA, NVCC_MLB, NVCC_JTAG	3.6	60
OSC24M_VDD, OSC_AUDIO_VDD, PHY1_VDDA, PHY2_VDD, USBPHY1_UPLLVDD, USBPHY1_VDDA_BIAS	3.6	25

1 This rail is connected to ground; it only needs a voltage if eFuses are to be programmed. FUSE_VDD should be supplied by following the power up sequence given in Section 4.3.1, “Powering Up.”

The method for obtaining max current is as follows:

1. Measure worst case power consumption on individual rails using directed test on i.MX35.
2. Correlate worst case power consumption power measurements with worst case power consumption simulations.
3. Combine common voltage rails based on power supply sequencing requirements
4. Guard band worst case numbers for temperature and process variation. Guard band is based on process data and correlated with actual data measured on i.MX35.
5. The sum of individual rails is greater than real world power consumption, as a real system does not typically maximize power consumption on all peripherals simultaneously.

4.6 Thermal Characteristics

The thermal resistance characteristics for the device are given in Table 12. These values were measured under the following conditions:

- Two-layer substrate
- Substrate solder mask thickness: 0.025 mm
- Substrate metal thicknesses: 0.016 mm
- Substrate core thickness: 0.200 mm
- Core via I.D: 0.168 mm, Core via plating 0.016 mm.
- Full array map design, but nearly all balls under die are power or ground.
- Die Attach: 0.033 mm non-conductive die attach, k = 0.3 W/m K
- Mold compound: k = 0.9 W/m K

Table 12. Thermal Resistance Data

Rating	Condition	Symbol	Value	Unit
Junction to ambient[1] natural convection	Single layer board (1s)	$R_{\theta JA}$	53	ºC/W
Junction to ambient[1] natural convection	Four layer board (2s2p)	$R_{\theta JA}$	30	ºC/W

Table 12. Thermal Resistance Data (continued)

Rating	Condition	Symbol	Value	Unit
Junction to ambient[1] (at 200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	44	ºC/W
Junction to ambient[1] (at 200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	27	ºC/W
Junction to boards[2]	—	$R_{\theta JB}$	19	ºC/W
Junction to case (top)[3]	—	$R_{\theta JCtop}$	10	ºC/W
Junction to package top[4]	Natural convection	Ψ_{JT}	2	ºC/W

1 Junction-to-ambient thermal resistance determined per JEDC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

2 Junction-to-board thermal resistance determined per JEDC JESD51-8. Thermal test board meets JEDEC specification for this package.

3 Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

4 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, this thermal characterization parameter is written as Psi-JT.

4.7 I/O Pin DC Electrical Characteristics

I/O pins are of two types: GPIO and DDR. DDR pins can be configured in three different drive strength modes: mobile DDR, SDRAM, and DDR2. The SDRAM and mobile DDR modes can be further customized at three drive strength levels: normal, high, and max.

Table 13 shows currents for the different DDR pin drive strength modes.

Table 13. DDR Pin Drive Strength Mode Current Levels

Drive Mode	Normal	High	Max.
Mobile DDR (1.8 V)	3.6 mA	7.2 mA	10.8 mA
SDRAM (1.8 V)	—	—	6.5 mA
SDRAM (3.3 V)	4 mA	8 mA	12 mA
DDR2 (1.8 V)	—	—	13.4 mA

Table 21. AC Electrical Characteristics of GPIO Pins in Fast Slew Rate Mode [NVCC = 2.25 V–2.75 V]

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units	Notes
Duty cycle	Fduty	—	40	—	60	%	—
Output pin slew rate (max. drive)	tps	25 pF 40 pF 50 pF	0.84/1.10 0.68/0.83 0.58/0.72	1.45/1.80 1.14/1.34 0.86/1.10	2.40/2.80 1.88/2.06 1.40/1.70	V/ns	2
Output pin slew rate (high drive)	tps	25 pF 40 pF 50 pF	0.69/0.96 0.55/0.69 0.40/0.59	1.18/1.50 0.92/1.10 0.67/0.95	1.90/2.30 1.49/1.67 1.10/1.30	V/ns	
Output pin slew rate (standard drive)	tps	25 pF 40 pF 50 pF	0.24/0.36 0.37/0.47 0.13/0.21	0.80/1.00 0.62/0.76 0.45/0.65	1.30/1.60 1.00/1.14 0.70/0.95	V/ns	
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	46 49	124 131	310 324	mA/ns	3
Output pin di/dt (high drive)	tdit	25 pF 50 pF	33 35	89 94	290 304	mA/ns	
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	28 29	75 79	188 198	mA/ns	

4.8.2 AC Electrical Characteristics for DDR Pins (DDR2, Mobile DDR, and SDRAM Modes)

Table 22. AC Electrical Characteristics of DDR Type IO Pins in DDR2 Mode

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	45	50	55	%
Clock frequency	f	—	—	133	—	MHz
Output pin slew rate	tps	25 pF 50 pF	0.86/0.98 0.46/054	1.35/1.5 0.72/0.81	2.15/2.19 1.12/1.16	V/ns
Output pin di/dt	tdit	25 pF 50 pF	65 70	157 167	373 396	mA/ns

Table 23. AC Requirements of DDR2 Pins

Parameter[1]	Symbol	Min.	Max.	Units
AC input logic high	VIH(ac)	NVCC ÷ 2 + 0.25	NVCC + 0.3	V
AC input logic low	VIL(ac)	–0.3	NVCC ÷ 2 – 0.25	V
AC differential cross point voltage for output[2]	Vox(ac)	NVCC ÷ 2 – 0.125	NVCC ÷ 2 + 0.125	V

[1] The Jedec SSTL_18 specification (JESD8-15a) for an SSTL interface for class II operation supersedes any specification in this document.

[2] The typical value of Vox(ac) is expected to be about 0.5 × NVCC and Vox(ac) is expected to track variation in NVCC. Vox(ac) indicates the voltage at which the differential output signal must cross. Cload = 25 pF.

Table 24. AC Electrical Characteristics of DDR Type IO Pins in mDDR Mode

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	45	50	55	%
Clock frequency	f	—	—	133	—	MHz
Output pin slew rate (max. drive)	tps	25 pF 50 pF	0.80/0.92 0.43/0.50	1.35/1.50 0.72/0.81	2.23/2.27 1.66/1.68	V/ns
Output pin slew rate (high drive)	tps	25 pF 50 pF	0.37/0.43 0.19/0.23	0.62/0.70 0.33/0.37	1.03/1.05 0.75/0.77	V/ns
Output pin slew rate (standard drive)	tps	25 pF 50 pF	0.18/0.22 0.10/0.12	0.31/0.35 0.16/0.18	0.51/0.53 0.38/0.39	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	64 69	171 183	407 432	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	37 39	100 106	232 246	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	18 20	50 52	116 123	mA/ns

Table 25. AC Electrical Characteristics of DDR Type IO Pins in SDRAM Mode

Parameter	Symbol	Test Condition	Min. Rise/Fall	Min. Clock Frequency	Max. Rise/Fall	Units
Clock frequency	f	—	—	125	—	MHz
Output pin slew rate (max. drive)	tps	25 pF 50 pF	1.11/1.20 0.97/0.65	1.74/1.75 0.92/0.94	2.42/2.46 1.39/1.30	V/ns
Output pin slew rate (high drive)	tps	25 pF 50 pF	0.76/0.80 0.40/0.43	1.16/1.19 0.61/0.63	1.76/1.66 0.93/0.87	V/ns
Output pin slew rate (standard drive)	tps	25 pF 50 pF	0.38/0.41 0.20/0.22	0.59/0.60 0.31/0.32	0.89/0.82 0.47/0.43	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	89 94	198 209	398 421	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	59 62	132 139	265 279	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	29 31	65 69	132 139	mA/ns

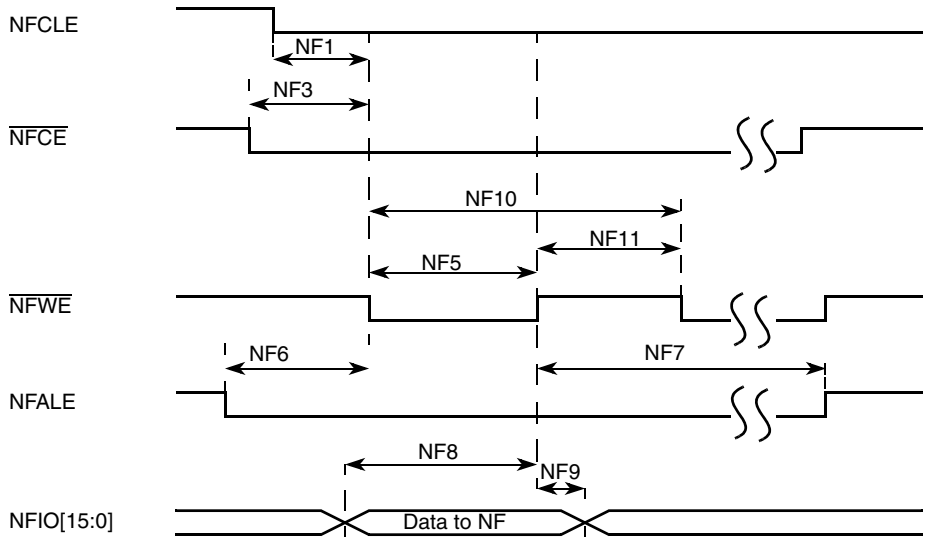


Figure 13. Write Data Latch Cycle Timing Diagram

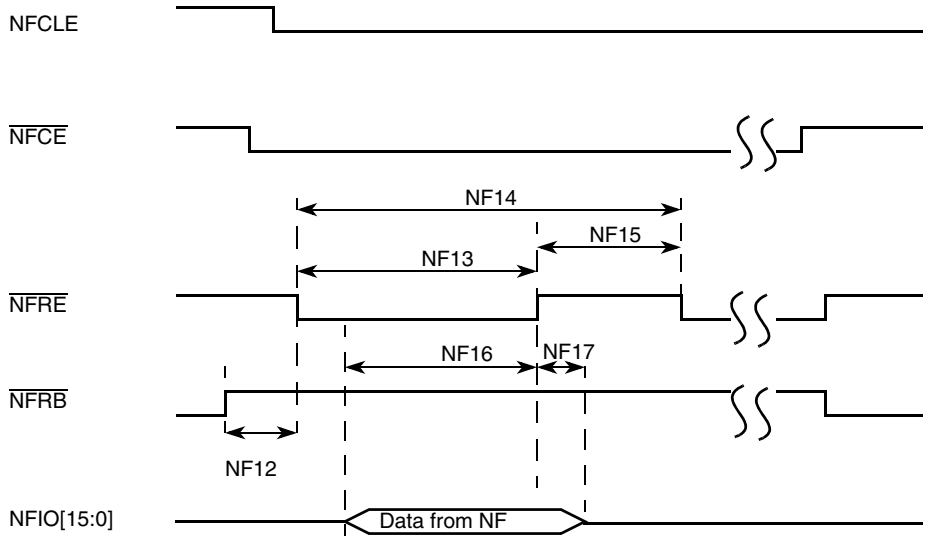


Figure 14. Read Data Latch Cycle Timing Diagram

Table 32. NFC Timing Parameters[1]

ID	Parameter	Symbol	Timing T = NFC Clock Cycle[2]		Example Timing for NFC Clock ≈ 33 MHz T = 30 ns		Unit
			Min.	Max.	Min.	Max.	
NF1	NFCLE setup time	tCLS	T – 4.0 ns	—	26	—	ns
NF2	NFCLE hold time	tCLH	T – 5.0 ns	—	25	—	ns
NF3	$\overline{\text{NFCE}}$ setup time	tCS	T – 2.0 ns	—	28	—	ns
NF4	$\overline{\text{NFCE}}$ hold time	tCH	T – 1.0 ns	—	29	—	ns

Table 35. DDR/SDR SDRAM Read Cycle Timing Parameters (continued)

ID	Parameter	Symbol	Min.	Max.	Unit
SD7	Address hold time	tAH	1.8	—	ns
SD8	SDRAM access time	tAC	—	6.47	ns
SD9	Data out hold time[1]	tOH	1.2	—	ns
SD10	Active to read/write command period	tRC	10	—	clock

[1] Timing parameters are relevant only to SDR SDRAM. For the specific DDR SDRAM data related timing parameters, see Table 44 and Table 45.

NOTE

SDR SDRAM CLK parameters are measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value. SD1 + SD2 does not exceed 7.5 ns for 133 MHz.

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 35 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

Table 39. DDR2 SDRAM Timing Parameter Table

ID	PARAMETER	Symbol	DDR2-400		Unit
			Min	Max	
DDR5	CS, RAS, CAS, CKE, WE hold time	t_{IH}[1]	1.25	—	ns
DDR6	Address output setup time	t_{IS}[1]	1.5	—	ns
DDR7	Address output hold time	t_{IH}[1]	1.5	—	ns

NOTE

These values are for command/address slew rate of 1 V/ns and SDCLK, SDCLK_B differential slew rate of 2 V/ns. For different values, use the derating table.

Table 40. Derating Values for DDR2–400, DDR2–533

Table 43. DDR2 SDRAM Read Cycle Parameter Table

ID	PARAMETER	Symbol	DDR2-400		Unit
			Min	Max	
DDR24	DQS – DQ Skew (defines the Data valid window in read cycles related to DQS).	t_{DQSQ}	—	0.35	ns
DDR25	DQS DQ in HOLD time from DQS[1]	t_{QH}	2.925	—	ns
DDR26	DQS output access time from SDCLK posedge	t_{DQSCK}	–0.5	0.5	ns

[1]The value was calculated for an SDCLK frequency of 133 MHz by the formula tQH = tHP – tQHS = min (tCL,tCH) – tQHS = 0.45 × tCK – tQHS = 0.45 × 7.5 – 0.45 = 2.925 ns.

NOTE

SDRAM CLK and DQS-related parameters are measured from the 50% point—that is, "high" is defined as 50% of signal value and "low" is defined as 50% of signal value. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and $\overline{\text{SDCLK}}$ (inverted clock).

Test conditions are: Capacitance 15 pF for DDR PADS. Recommended drive strength is Medium for SDCLK and High for Address and controls.

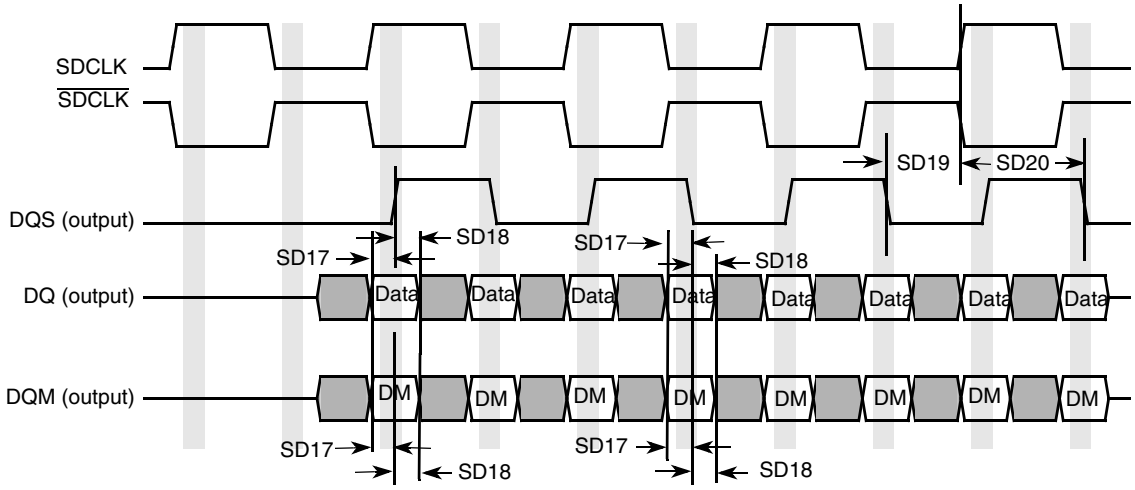


Figure 34. Mobile DDR SDRAM Write Cycle Timing Diagram

Table 44. Mobile DDR SDRAM Write Cycle Timing Parameters[1]

ID	Parameter	Symbol	Min.	Max.	Unit
SD17	DQ and DQM setup time to DQS	tDS	0.95	—	ns
SD18	DQ and DQM hold time to DQS	tDH	0.95	—	ns
SD19	Write cycle DQS falling edge to SDCLK output delay time.	tDSS	1.8	—	ns
SD20	Write cycle DQS falling edge to SDCLK output hold time.	tDSH	1.8	—	ns

[1] Test condition: Measured using delay line 5 programmed as follows: ESDCDLY5[15:0] = 0x0703.

The timing described in Figure 45 is that of a Motorola sensor. Some other sensors may have slightly different timing. The CSI can be programmed to support rising/falling-edge triggered SENSB_VSYNC; active-high/low SENSB_HSYNC; and rising/falling-edge triggered SENSB_PIX_CLK.

4.9.12.3 Electrical Characteristics

Figure 46 depicts the sensor interface timing, and Table 54 lists the timing parameters.

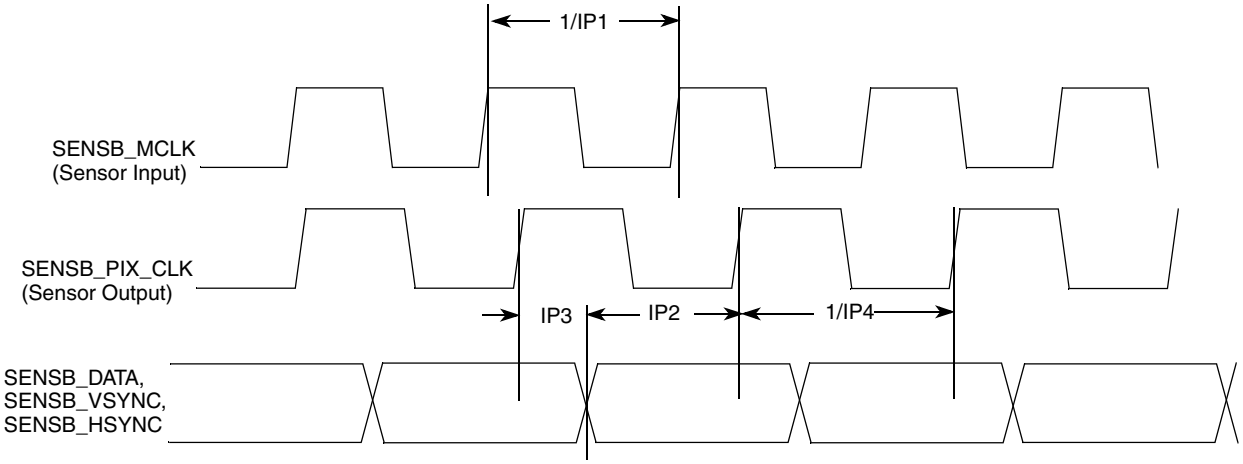


Figure 46. Sensor Interface Timing Diagram

Table 54. Sensor Interface Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
IP1	Sensor input clock frequency	Fmck	0.01	133	MHz
IP2	Data and control setup time	Tsu	5	—	ns
IP3	Data and control holdup time	Thd	3	—	ns
IP4	Sensor output (pixel) clock frequency	Fpck	0.01	133	MHz

4.9.13 IPU—Display Interfaces

This section describes the following types of display interfaces:

- Section 4.9.13.1, “Synchronous Interfaces”
- Section 4.9.13.2, “Interface to Sharp HR-TFT Panels”
- Section 4.9.13.3, “Synchronous Interface to Dual-Port Smart Displays”
- Section 4.9.13.4, “Asynchronous Interfaces”
- Section 4.9.13.5, “Serial Interfaces, Functional Description”

Table 56. Synchronous Display Interface Timing Parameters—Access Level

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP16	Display interface clock low time	Tckl	Tdicd – Tdicu – 1.5	Tdicd[2] – Tdicu[3]	Tdicd – Tdicu + 1.5	ns
IP17	Display interface clock high time	Tckh	Tdicp – Tdicd + Tdicu – 1.5	Tdicp – Tdicd + Tdicu	Tdicp – Tdicd + Tdicu + 1.5	ns
IP18	Data setup time	Tdsu	Tdicd – 3.5	Tdicu	—	ns
IP19	Data holdup time	Tdhd	Tdicp – Tdicd – 3.5	Tdicp – Tdicu	—	ns
IP20	Control signals setup time to display interface clock	Tcsu	Tdicd – 3.5	Tdicu	—	ns

1 The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device specific.

2 Display interface clock down time

$$Tdicd = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP3\_IF\_CLK\_DOWN\_WR}{HSP\_CLK\_PERIOD}\right]$$

3 Display interface clock up time

$$Tdicu = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP3\_IF\_CLK\_UP\_WR}{HSP\_CLK\_PERIOD}\right]$$

where CEIL(X) rounds the elements of X to the nearest integers toward infinity.

4.9.13.2 Interface to Sharp HR-TFT Panels

Figure 51 depicts the Sharp HR-TFT panel interface timing, and Table 57 lists the timing parameters. The CLS_RISE_DELAY, CLS_FALL_DELAY, PS_FALL_DELAY, PS_RISE_DELAY, REV_TOGGLE_DELAY parameters are defined in the SDC_SHARP_CONF_1 and SDC_SHARP_CONF_2 registers. For other Sharp interface timing characteristics, refer to

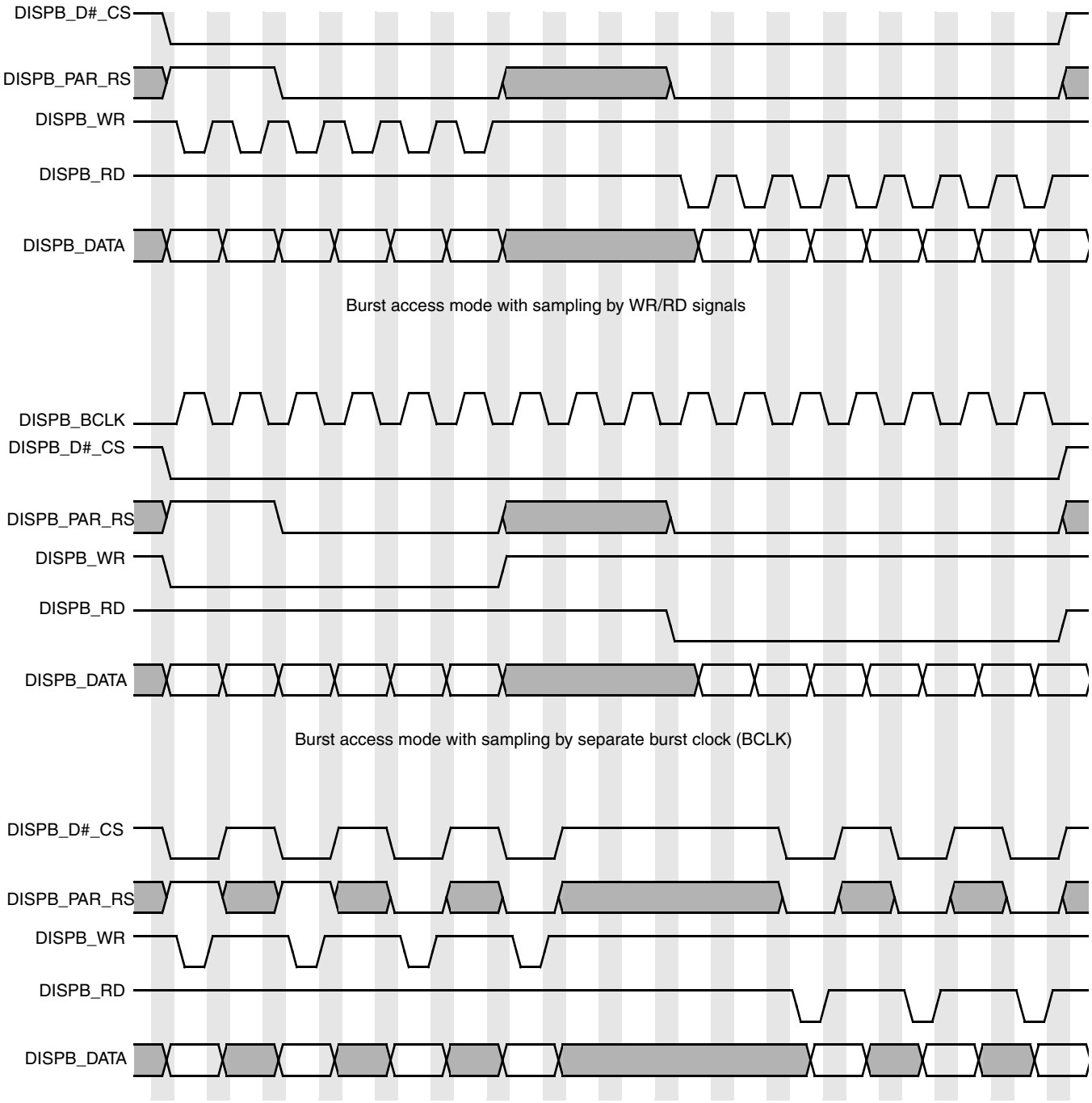


Figure 54. Asynchronous Parallel System 80 Interface (Type 2) Burst Mode Timing Diagram

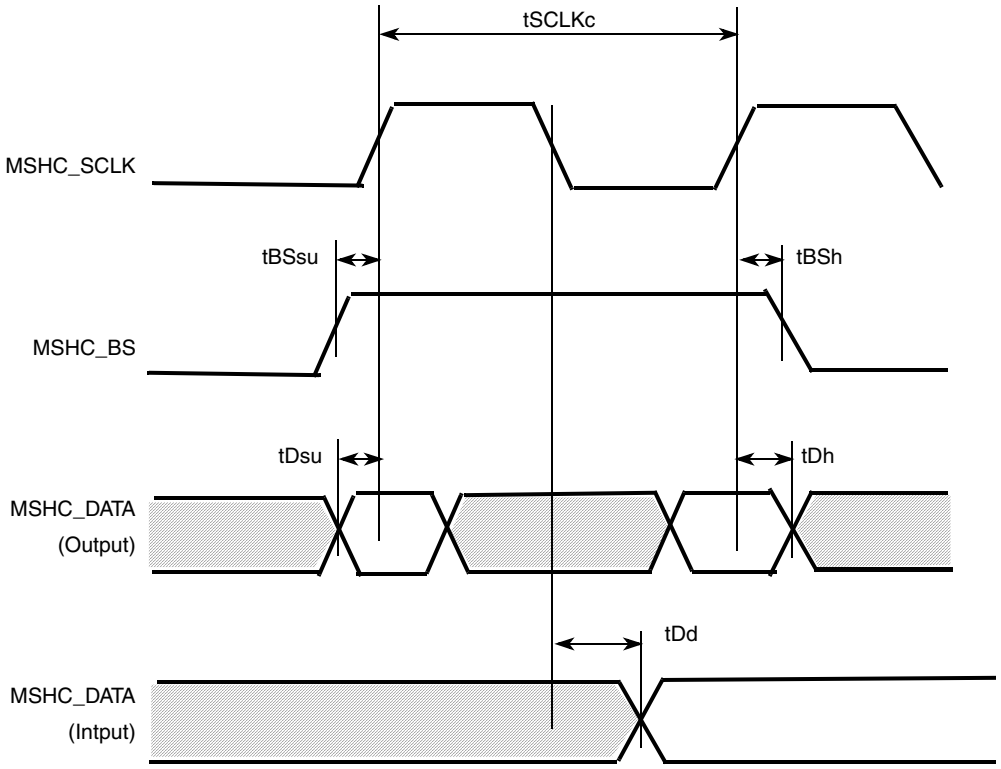


Figure 68. Transfer Operation Timing Diagram (Serial)

4.9.17 Parallel ATA Module AC Electrical Specifications

The parallel ATA module can work on PIO/multiword DMA/ultra-DMA transfer modes (not available for the MCIMX351). Each transfer mode has a different data transfer rate, Ultra DMA mode 4 data transfer rate is up to 100 MBps.

The parallel ATA module interface consists of a total of 29 pins. Some pins have different functions in different transfer modes. There are various requirements for timing relationships among the function pins, in compliance with the ATA/ATAPI-6 specification, and these requirements are configurable by the ATA module registers.

4.9.17.1 General Timing Requirements

Table 67 and Figure 74 define the AC characteristics of the interface signals on all data transfer modes.

Table 67. AC Characteristics of All Interface Signals

ID	Parameter	Symbol	Min.	Max.	Unit
SI1	Rising edge slew rate for any signal on the ATA interface[1]	S_{rise}[1]	—	1.25	V/ns
SI2	Falling edge slew rate for any signal on the ATA interface[1]	S_{fall}[1]	—	1.25	V/ns
SI3	Host interface signal capacitance at the host connector	C_{host}	—	20	pF

[1] SRISE and SFALL meet this requirement when measured at the sender's connector from 10–90% of full signal amplitude with all capacitive loads from 15 pF through 40 pF, where all signals have the same capacitive load value.

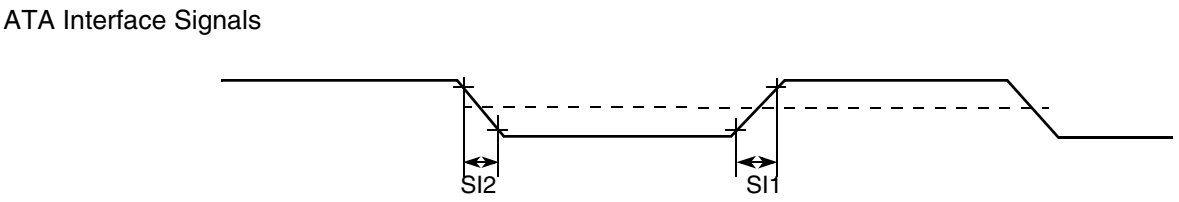


Figure 74. ATA Interface Signals Timing Diagram

4.9.17.2 ATA Electrical Specifications (ATA Bus, Bus Buffers)

This section discusses ATA parameters. For a detailed description, refer to the ATA-6 specification.

Level shifters are required for 3.3-V or 5.0-V compatibility on the ATA interface.

The use of bus buffers introduces delays on the bus and introduces skew between signal lines. These factors make it difficult to operate the bus at the highest speed (UDMA-5) when bus buffers are used. Use of bus buffers is not recommended if fast UDMA mode is required.

The ATA specification imposes a slew rate limit on the ATA bus. According to this limit, any signal driven on the bus should have a slew rate between 0.4 and 1.2 V/ns with a 40 pF load. Few vendors of bus buffers specify the slew rate of the outgoing signals.

When bus buffers are used the ata_data bus buffer is bidirectional, and uses the direction control signal ata_buffer_en. When ata_buffer_en is asserted, the bus should drive from host to device. When

4.9.17.6 UDMA-Out Timing

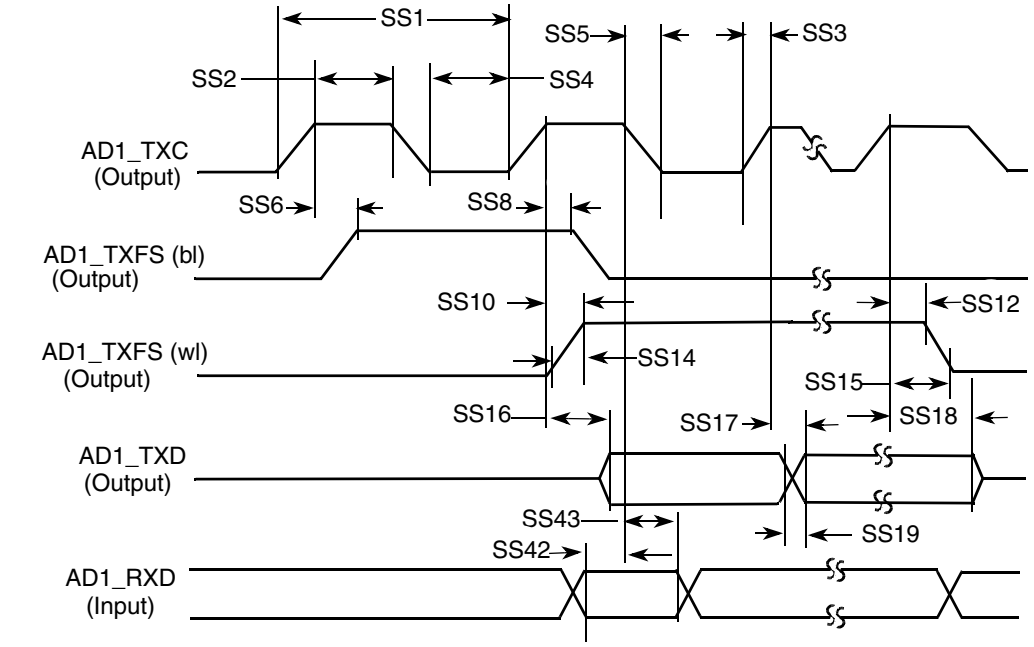
Figure 82 shows timing when the UDMA-out transfer starts, Figure 83 shows timing when the UDMA-out host terminates transfer, Figure 84 shows timing when the UDMA-out device terminates transfer, and Table 73 lists the timing parameters for the UDMA-out burst.

Figure 82. UDMA-Out Transfer Starts Timing Diagram

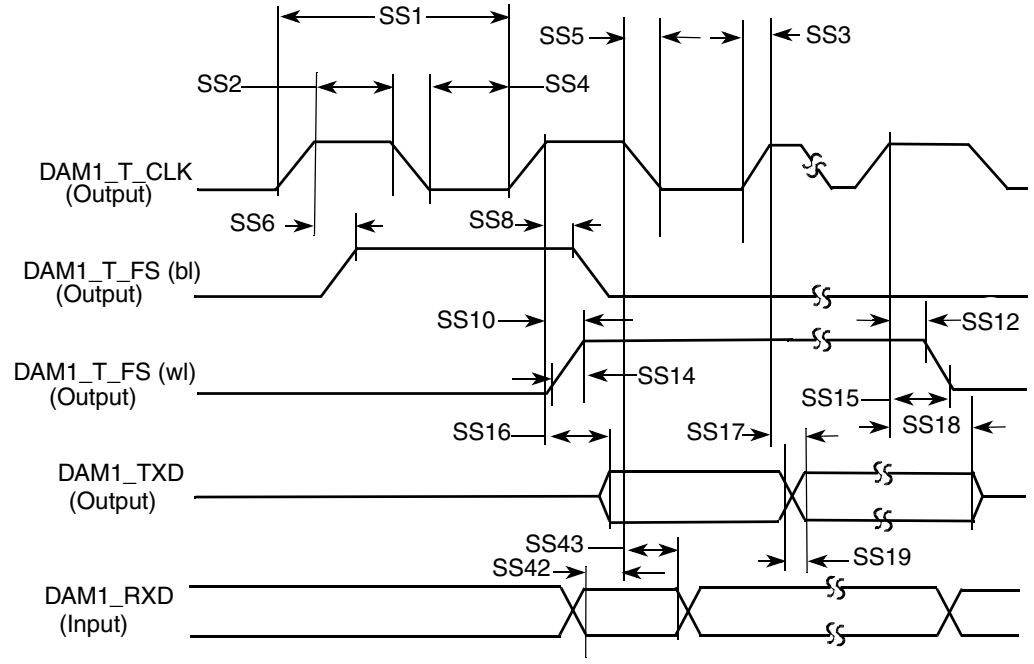
Figure 83. UDMA-Out Host Terminates Transfer Timing Diagram

4.9.22.1 SSI Transmitter Timing with Internal Clock

Figure 92 depicts the SSI transmitter timing with internal clock, and Table 78 lists the timing parameters.



Note: SRXD Input in Synchronous mode only



Note: SRXD Input in Synchronous mode only

Figure 92. SSI Transmitter with Internal Clock Timing Diagram

Table 84. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA3	Transmit bit time in IrDA mode	t_{TIRbit}	$1/F_{baud\_rate}$[1] – T_{ref_clk}[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—
UA4	Transmit IR pulse duration	$t_{TIRpulse}$	$(3/16) \times (1/F_{baud\_rate}) - T_{ref\_clk}$	$(3/16) \times (1/F_{baud\_rate}) + T_{ref\_clk}$	—

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.9.23.2.14 UART IrDA Mode Receiver

Figure 99 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 85 lists the receive timing characteristics.

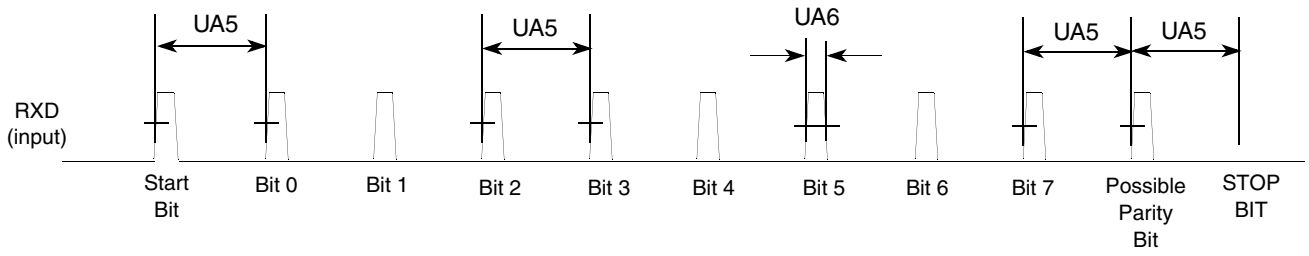


Figure 99. UART IrDA Mode Receive Timing Diagram

Table 85. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA5	Receive bit time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud\_rate}$[2] – $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—
UA6	Receive IR pulse duration	$t_{RIRpulse}$	1.41 us	$(5/16) \times (1/F_{baud\_rate})$	—

1 The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency) ÷ 16.

4.9.24 USB Electrical Specifications

In order to support four different serial interfaces, the USB serial transceiver can be configured to operate in one of four modes:

- DAT_SE0 bidirectional, 3-wire mode
- DAT_SE0 unidirectional, 6-wire mode
- VP_VM bidirectional, 4-wire mode
- VP_VM unidirectional, 6-wire mode

Table 96. Silicon Revision 2.0 Ball Map—17 x 17, 0.8 mm Pitch[1] (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
V	ATA_DA1	ATA_INTRQ	ATA_DATA10	ATA_DATA6	ATA_DATA2	ATA_DMACK	ATA_CS0	EXT_ARMCLK	CSPI1_MISO	CLKO	GPIO3_0	CAPTURE	SD2_DATA0	CSI_HSYNC	CSI_D13	CSI_D10	SD1_DATA3	SD1_CLK	XTAL_AUDIO	OSC_AUDIO_VDD	V
W	ATA_DATA14	ATA_DATA13	ATA_DATA9	ATA_DATA5	ATA_DATA1	ATA_DIOW	USBOTG_PWR	CSPI1_SCLK	CSPI1_MOSI	BOOT_MODE0	POR_B	MLB_SIG	MLB_CLK	SD2_CLK	CSI_MCLK	CSI_D12	CSI_D9	SD1_DATA2	DE_B	EXTAL_AUDIO	W
Y	VSS	ATA_DATA11	ATA_DATA7	ATA_DATA4	ATA_DATA0	ATA_DIOR	TEST_MODE	CSPI1_SS0	POWER_FAIL	CLK_MODE0	GPIO1_1	WDOG_RST	MLB_DAT	SD2_DATA2	CSI_PIXCLK	CSI_D15	USBPHY2_DM	USBPHY2_DP	SD1_CMD	VSS	Y

[1] See Table 95 for pins unavailable in the MCIMX351 SoC.

Table 97. Silicon Revision 2.1 Ball Map—17 x 17, 0.8 mm Pitch

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	GND	D0	A9	A7	A0	SDBA0	SD30	SD27	SD24	SD23	SD21	SD18	SD15	SD14	SD10	SD9	SD6	SD4	SD1	GND	A
B	D5	D2	A13	A8	A5	SDBA1	SD31	SD28	SD26	SD22	SD20	SD19	SD12	SD13	SD11	SD7	SD0	SD2	DQM0	CS2	B
C	D8	D7	D4	MA10	A6	A3	A23	SD29	SD25	A20	SD17	SD16	A17	SD8	SD5	SD3	DQM1	DQM3	CS3	RW	C
D	D14	D10	D6	D1	A11	A4	A1	A24	A22	A21	A19	A18	A16	A14	A15	DQM2	SDCKE1	SDCKE0	ECB	LBA	D
E	NFCLE	D15	D12	D9	D3	D11	A2	A25	SDQS3	SDQS2	SDQS1	SDCLK	SDCLK_B	SDQS0	BCLK	RAS	CAS	CS4	CS1	OE	E
F	NFRE_B	NFALE	NFRB	NFWP_B	D13	A12	VDD7	VDD7	VDD7	GND	NVCC_EMI1	VDD7	NVCC_EMI2	GND	A10	EB1	CS0	EB0	CS5	LD0	F
G	RTS2	NFWE_B	NF_CE0	TX0	CTS2	NVCC_NFC	NVCC_EMI1	NVCC_EMI1	NVCC_EMI1	NVCC_EMI1	NVCC_EMI1	NVCC_EMI2	VDD6	NVCC_EMI3	SDWE	LD3	LD2	LD1	LD4	LD7	G
H	TX1	TXD2	RXD2	TX4_RX1	TX2_RX3	NVCC_NFC	NVCC_NFC	GND	NVCC_EMI1	NVCC_EMI1	GND	GND	NVCC_EMI2	NVCC_LCDC	VDD5	LD5	LD8	LD6	LD9	LD10	H
J	FST	TX3_RX2	TX5_RX0	SCKT	HCKT	STXFS5	VDD1	GND	GND	GND	GND	GND	GND	NVCC_LCDC	VDD5	LD12	LD14	LD11	LD13	LD15	J
K	STXD5	HCKR	SCKR	SRXD5	FSR	NVCC_MISC	NVCC_MISC	GND	GND	GND	GND	GND	GND	LD16	LD22	LD20	LD21	LD18	LD17	LD19	K
L	SRXD4	STXFS4	I2C2_CLK	SCK4	SCK5	FEC_TDATA3	VDD2	NVCC_MISC	GND	GND	GND	GND	GND	NVCC_LCDC	D3_FPSHIFT	CONTRAST	D3_CLS	D3_HSYNC	LD23	D3_DRDY	L
M	I2C2_DAT	STXD4	FEC_RDATA2	FEC_TDATA1	FEC_TDATA2	VDD2	GND	GND	GND	GND	FUSE_VSS	PGND	GND	NVCC_LCDC	PHY1_VDDA	TTM_PAD	D3_REV	D3_SPL	D3_VSYNC	I2C1_CLK	M
N	FEC_RDATA3	FEC_RDATA1	FEC_RX_ERR	FEC_TX_ERR	FEC_CRS	NVCC_ATA	VDD3	GND	GND	GND	MGND	GND	PVDD	USBPHY1_UPLLGND	USBPHY1_UPLLVDD	PHY1_VSSA	I2C1_DAT	USBPHY1_UID	USBPHY1_DM	PHY1_VDDA	N