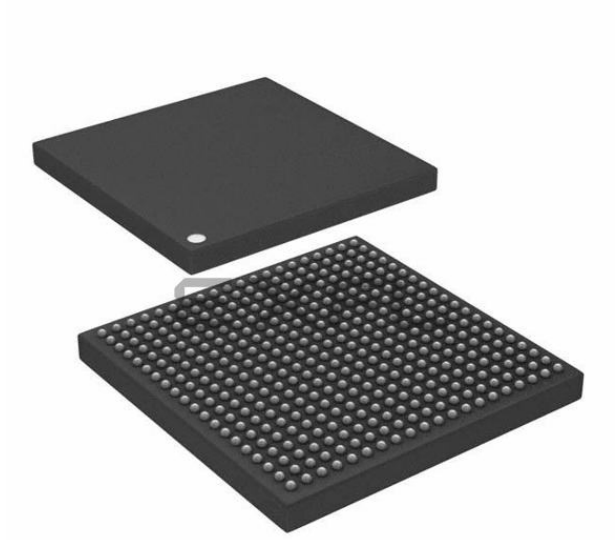

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	532MHz
Co-Processors/DSP	Multimedia; IPU, VFP
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad, KPP, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Secure Fusebox, Secure JTAG
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx355avm5br2

Figure 7 and Figure 8 depict the master mode and slave mode timings of the CSPI, and Table 27 lists the timing parameters.

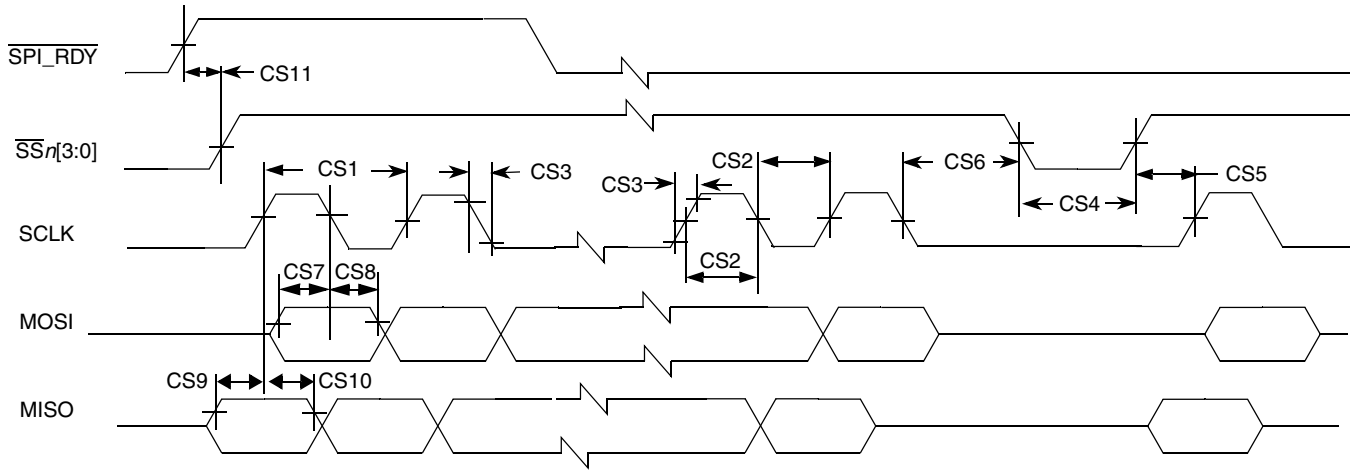


Figure 7. CSPI Master Mode Timing Diagram

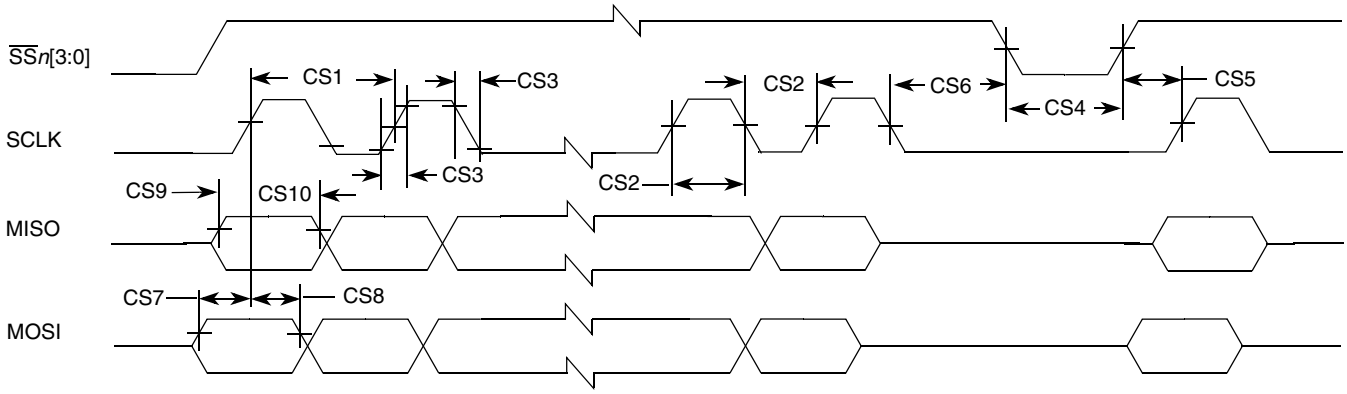


Figure 8. CSPI Slave Mode Timing Diagram

Table 27. CSPI Interface Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
CS1	SCLK cycle time	t_{clk}	60	—	ns
CS2	SCLK high or low time	t_{SW}	30	—	ns
CS3	SCLK rise or fall	$t_{RISE/FALL}$	—	7.6	ns
CS4	$\overline{SS}n$[3:0] pulse width	t_{CSLH}	30	—	ns
CS5	$\overline{SS}n$[3:0] lead time (CS setup time)	t_{SCS}	30	—	ns
CS6	$\overline{SS}n$[3:0] lag time (CS hold time)	t_{HCS}	30	—	ns
CS7	MOSI setup time	t_{Smosi}	5	—	ns
CS8	MOSI hold time	t_{Hmosi}	5	—	ns
CS9	MISO setup time	t_{Smiso}	5	—	ns

Recommended drive strength for all controls, address and BCLK is set to maximum drive.

Figure 16 through Figure 21 depict some examples of basic WEIM accesses to external memory devices with the timing parameters mentioned in Table 33 for specific control parameter settings.

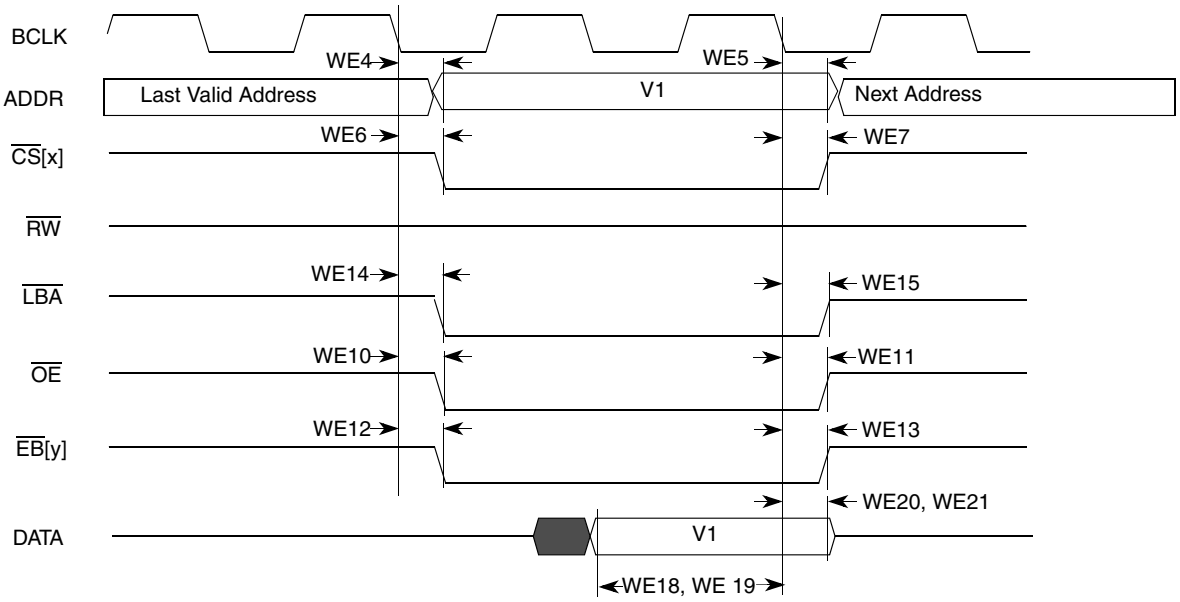


Figure 16. Synchronous Memory Timing Diagram for Read Access—WSC = 1

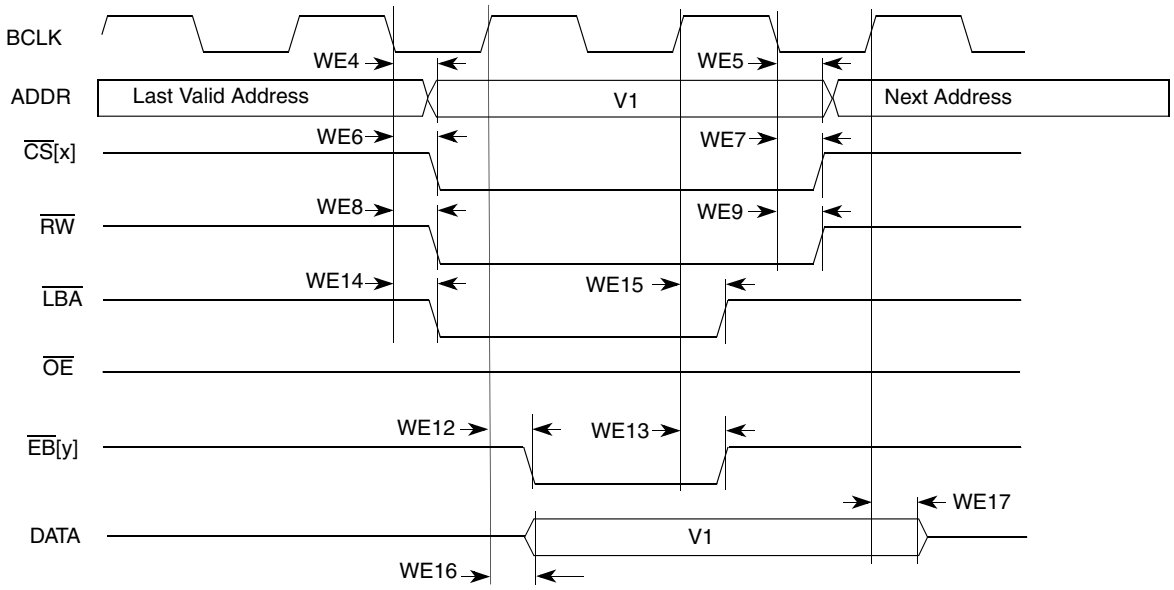


Figure 17. Synchronous Memory Timing Diagram for Write Access—WSC = 1, EBWA = 1, EBWN = 1, LBN = 1

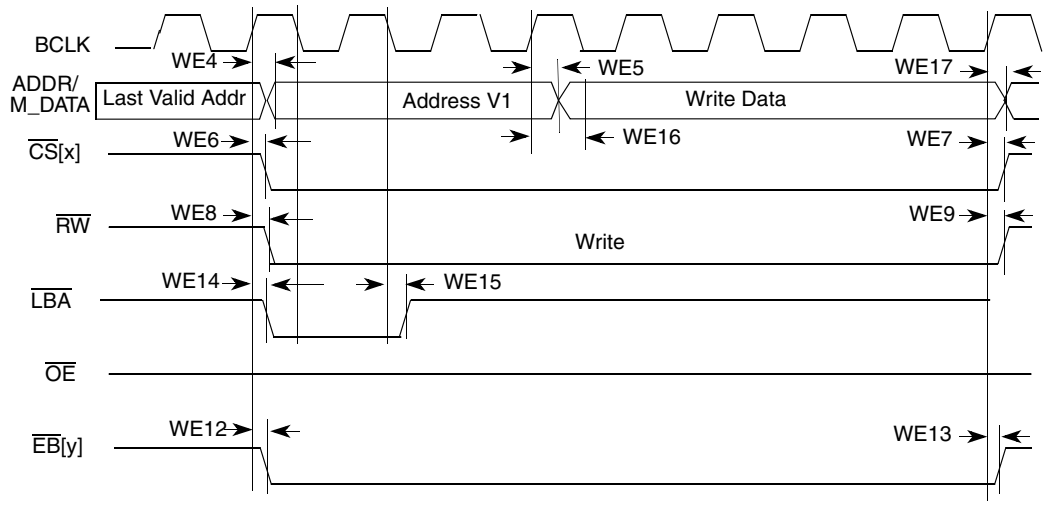


Figure 20. Muxed A/D Mode Timing Diagram for Synchronous Write Access—WSC = 7, LBA = 1, LBN = 1, LAH = 1

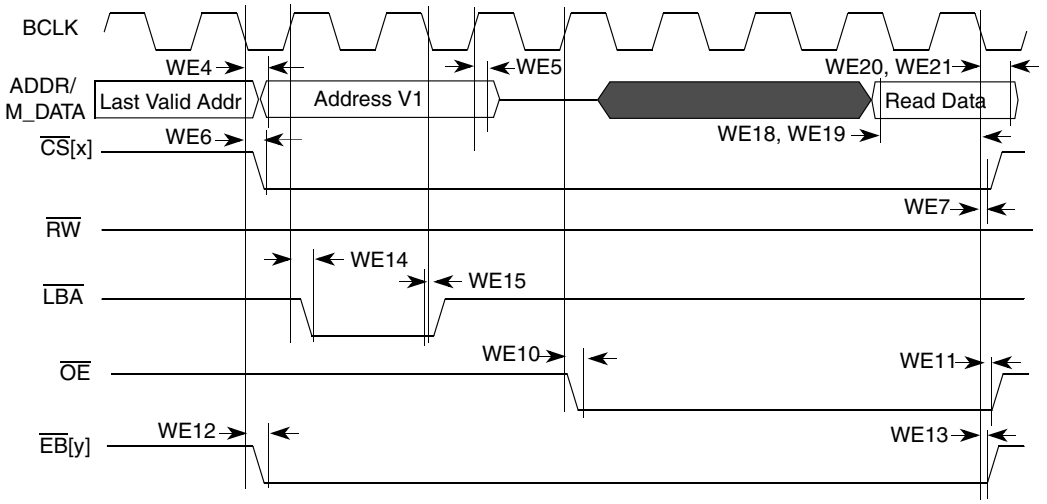


Figure 21. Muxed A/D Mode Timing Diagram for Synchronous Read Access—WSC = 7, LBA = 1, LBN = 1, LAH = 1, OEA = 7

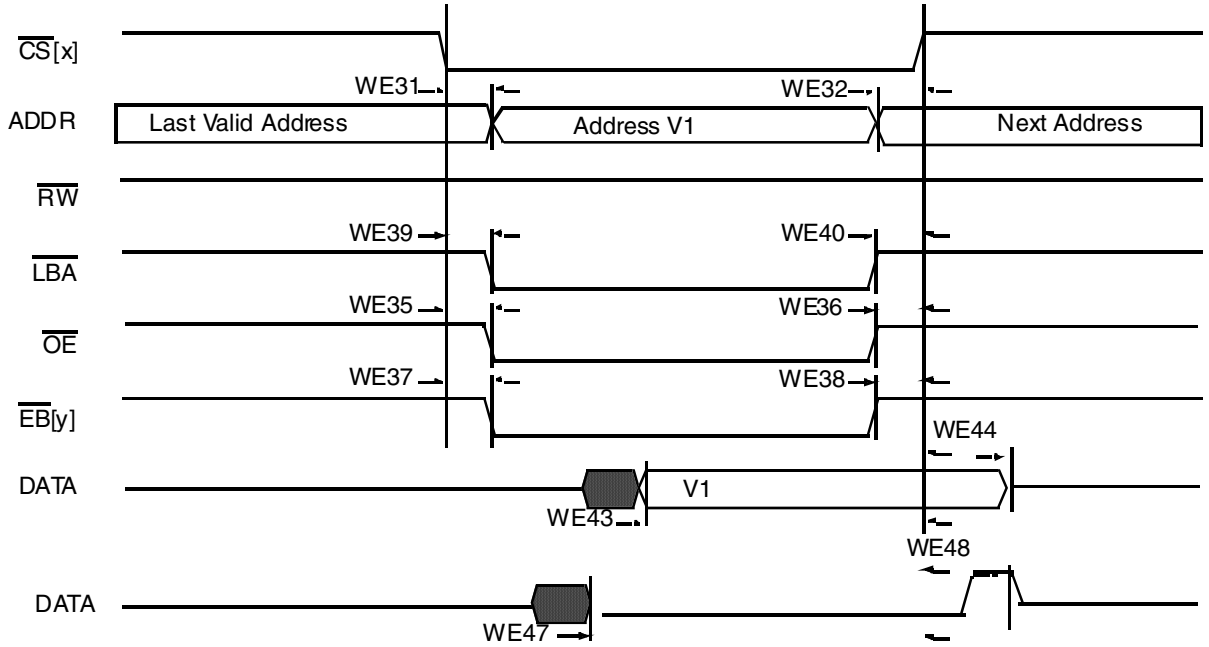


Figure 26. DTACK Read Access

Table 34. WEIM Asynchronous Timing Parameters Relative Chip Select Table

Ref No.	Parameter	Determination By Synchronous Measured Parameters[1]	Min	Max (If 133 MHz is supported by SoC)	Unit
WE31	$\overline{CS}$[x] valid to Address valid	WE4 – WE6 – CSA[2]	—	3 – CSA	ns
WE32	Address invalid to $\overline{CS}$[x] invalid	WE7 – WE5 – CSN[3]	—	3 – CSN	ns
WE32A(muxed A/D	$\overline{CS}$[x] valid to address invalid	WE4 – WE7 + (LBN + LBA + 1 – CSA[2])	–3 + (LBN + LBA + 1 – CSA)	—	ns
WE33	$\overline{CS}$[x] valid to $\overline{WE}$ valid	WE8 – WE6 + (WEA – CSA)	—	3 + (WEA – CSA)	ns
WE34	$\overline{WE}$ invalid to $\overline{CS}$[x] invalid	WE7 – WE9 + (WEN – CSN)	—	3 – (WEN_CSN)	ns
WE35	$\overline{CS}$[x] valid to $\overline{OE}$ valid	WE10 – WE6 + (OEA – CSA)	—	3 + (OEA – CSA)	ns
WE35A (muxed A/D)	$\overline{CS}$[x] valid to $\overline{OE}$ valid	WE10 – WE6 + (OEA + RLBN + RLBA + ADH + 1 – CSA)	–3 + (OEA + RLBN + RLBA + ADH + 1 – CSA)	3 + (OEA + RLBN + RLBA + ADH + 1 – CSA)	ns
WE36	$\overline{OE}$ invalid to $\overline{CS}$[x] invalid	WE7 – WE11 + (OEN – CSN)	—	3 – (OEN – CSN)	ns
WE37	$\overline{CS}$[x] valid to $\overline{BE}$[y] valid (read access)	WE12 – WE6 + (RBEA – CSA)	—	3 + (RBEA[4] – CSA)	ns
WE38	$\overline{BE}$[y] invalid to $\overline{CS}$[x] invalid (read access)	WE7 – WE13 + (RBEN – CSN)	—	3 – (RBEN[5] – CSN)	ns
WE39	$\overline{CS}$[x] valid to $\overline{LBA}$ valid	WE14 – WE6 + (LBA – CSA)	—	3 + (LBA – CSA)	ns
WE40	$\overline{LBA}$ invalid to $\overline{CS}$[x] invalid	WE7 – WE15 – CSN	—	3 – CSN	ns

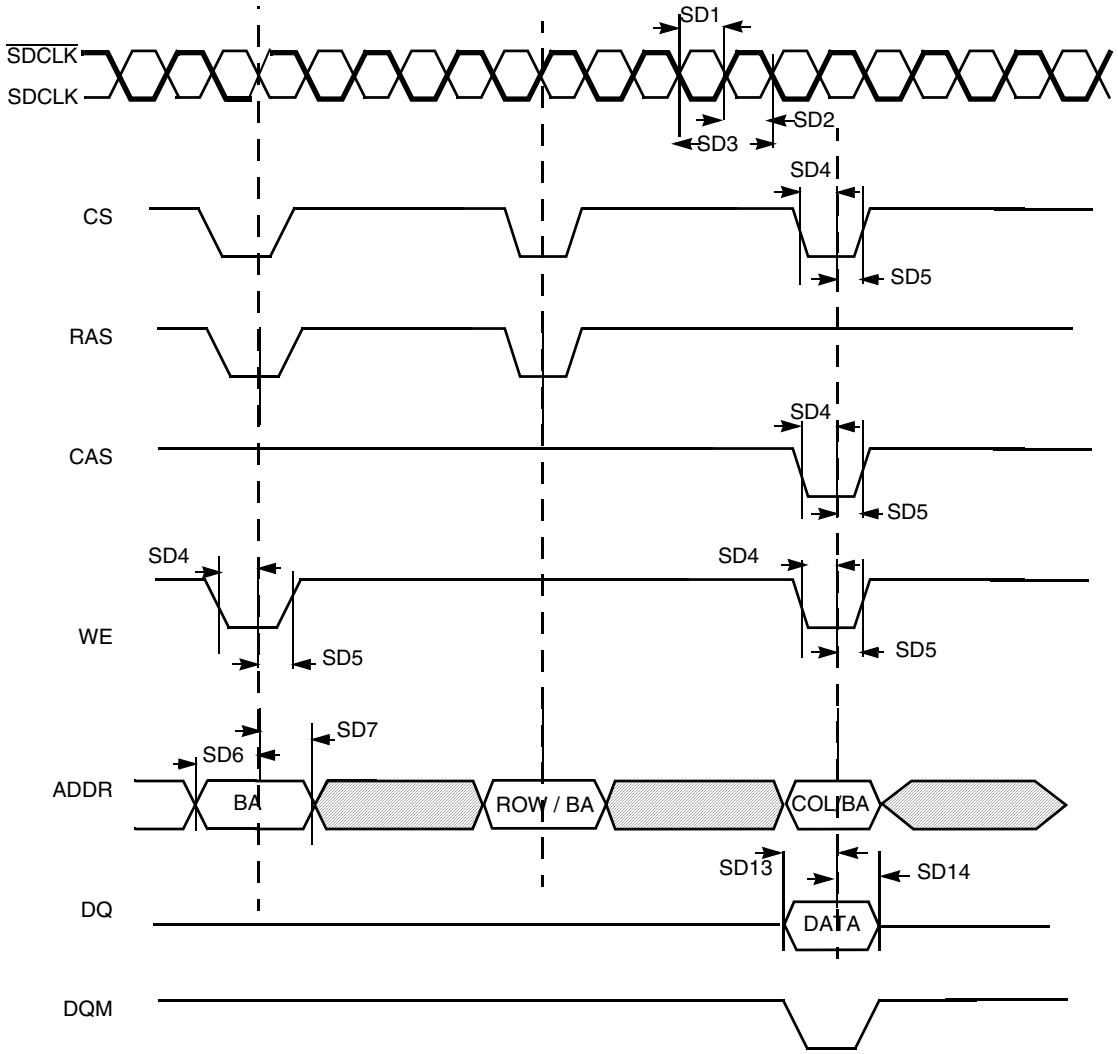


Figure 28. SDR SDRAM Write Cycle Timing Diagram

Table 36. SDR SDRAM Write Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD1	SDRAM clock high-level width	tCH	0.45	0.55	ns
SD2	$\overline{\text{SDRAM}}$ clock low-level width	tCL	0.45	0.55	ns
SD3	SDRAM clock cycle time	tCK	7.0	—	ns
SD4	CS, RAS, CAS, WE, DQM, CKE setup time	tCMS	2.4	—	ns
SD5	CS, RAS, CAS, WE, DQM, CKE hold time	tCMH	1.4	—	ns
SD6	Address setup time	tAS	2.4	—	ns
SD7	Address hold time	tAH	1.4	—	ns
SD13	Data setup time	tDS	2.4	—	ns
SD14	Data hold time	tDH	1.4	—	ns

4.9.8.3 MII Transmit Signal Timing

The transmitter timing signals consist of FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER, and FEC_TX_CLK. The transmitter functions correctly up to a FEC_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the FEC_TX_CLK frequency. Table 49 lists MII transmit channel timings.

Table 49. MII Transmit Signal Timing

Num	Characteristic[1]	Min.	Max.	Unit
M5	FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER invalid	5	—	ns
M6	FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER valid	—	20	ns
M7	FEC_TX_CLK pulse width high	35%	65%	FEC_TX_CLK period
M8	FEC_TX_CLK pulse width low	35%	65%	FEC_TX_CLK period

[1] FEC_TX_EN, FEC_TX_CLK, and FEC_TXD0 have the same timing when in 10 Mbps 7-wire interface mode.

Figure 40 shows the MII transmit signal timings listed in Table 49.

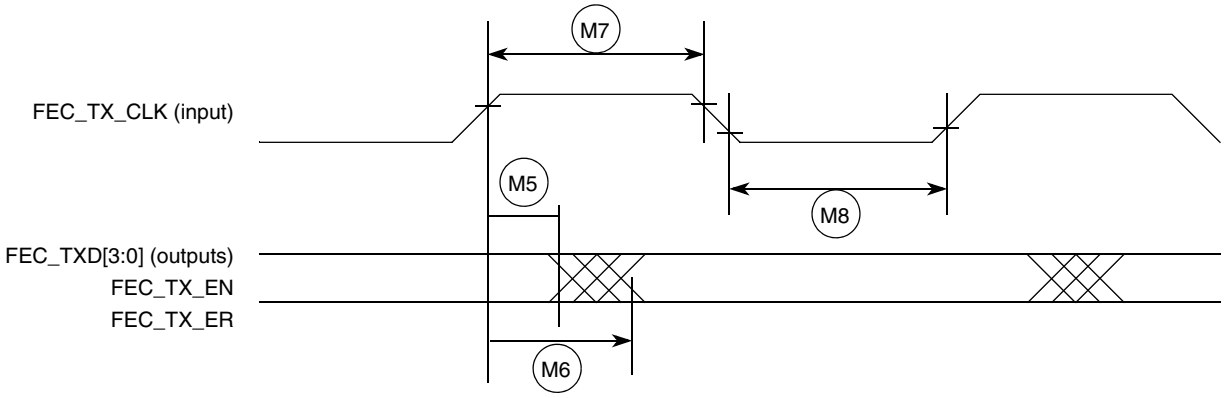


Figure 40. MII Transmit Signal Timing Diagram

4.9.8.4 MII Asynchronous Inputs Signal Timing

The MII asynchronous timing signals are FEC_CRS and FEC_COL. Table 50 lists MII asynchronous inputs signal timing.

Table 50. MII Asynch Inputs Signal Timing

Num	Characteristic	Min.	Max.	Unit
M9[1]	FEC_CRS to FEC_COL minimum pulse width	1.5	—	FEC_TX_CLK period

[1] FEC_COL has the same timing in 10 Mbit 7-wire interface mode.

4.9.12 IPU—Sensor Interfaces

This section contains a list of supported camera sensors, a functional description, and the electrical characteristics.

4.9.12.1 Supported Camera Sensors

Table 53 lists the known supported camera sensors at the time of publication.

Table 53. Supported Camera Sensors[1]

Vendor	Model
Conexant	CX11646, CX20490[2], CX20450[2]
Agilant	HDCP–2010, ADCS–1021[2], ADCS–1021[2]
Toshiba	TC90A70
ICMedia	ICM202A, ICM102[2]
iMagic	IM8801
Transchip	TC5600, TC5600J, TC5640, TC5700, TC6000
Fujitsu	MB86S02A
Micron	MI-SOC–0133
Matsushita	MN39980
STMicro	W6411, W6500, W6501[2], W6600[2], W6552[2], STV0974[2]
OmniVision	OV7620, OV6630, OV2640
Sharp	LZ0P3714 (CCD)
Motorola	MC30300 (Python)[2], SCM20014[2], SCM20114[2], SCM22114[2], SCM20027[2]
National Semiconductor	LM9618[2]

1 Freescale Semiconductor does not recommend one supplier over another and in no way suggests that these are the only camera suppliers.

2 These sensors have not been validated at the time of publication.

4.9.12.2 Functional Description

There are three timing modes supported by the IPU.

4.9.12.2.1 Pseudo BT.656 Video Mode

Smart camera sensors, which typically include image processing capability, support video mode transfer operations. They use an embedded timing syntax to replace the SENSB_VSYNC and SENSB_HSYNC signals. The timing syntax is defined by the BT.656 standard.

This operation mode follows the recommendations of the ITU BT.656 specifications. The only control signal used is SENSB_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with an EAV code. In some cases, digital blanking is

4.9.13.1 Synchronous Interfaces

This section discusses the interfaces to active matrix TFT LCD panels, Sharp HR-TFT, and dual-port smart displays.

4.9.13.1.4 Interface to Active Matrix TFT LCD Panels, Functional Description

Figure 47 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure, signals are shown with negative polarity. The sequence of events for active matrix interface timing is as follows:

- DISPB_D3_CLK latches data into the panel on its negative edge (when positive polarity is selected). In active mode, DISPB_D3_CLK runs continuously.
- DISPB_D3_HSYNC causes the panel to start a new line.
- DISPB_D3_VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse.
- DISPB_D3_DRDY acts like an output enable signal to the CRT display. This output enables the data to be shifted to the display. When disabled, the data is invalid and the trace is off.

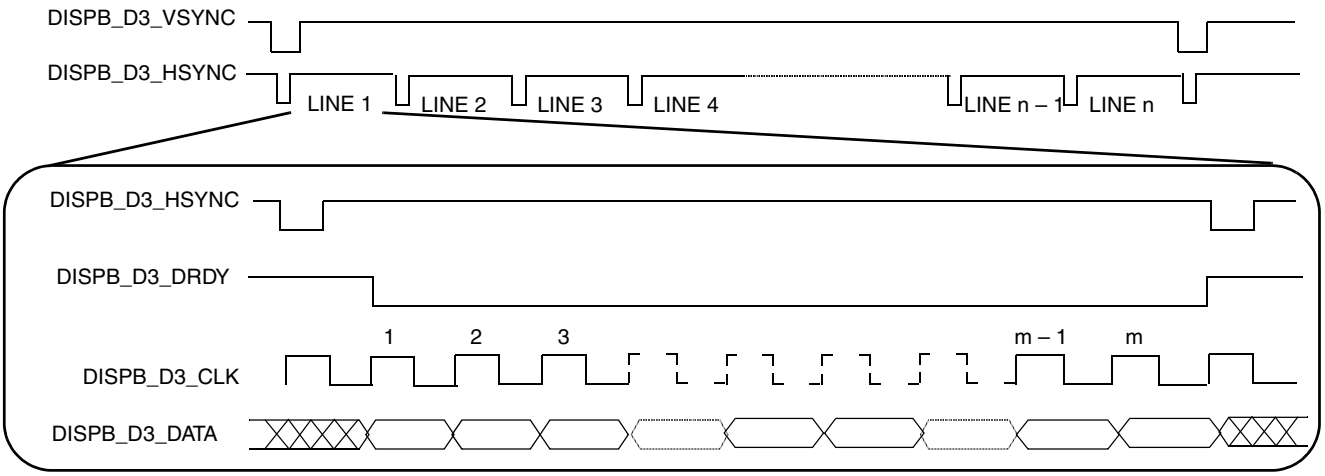
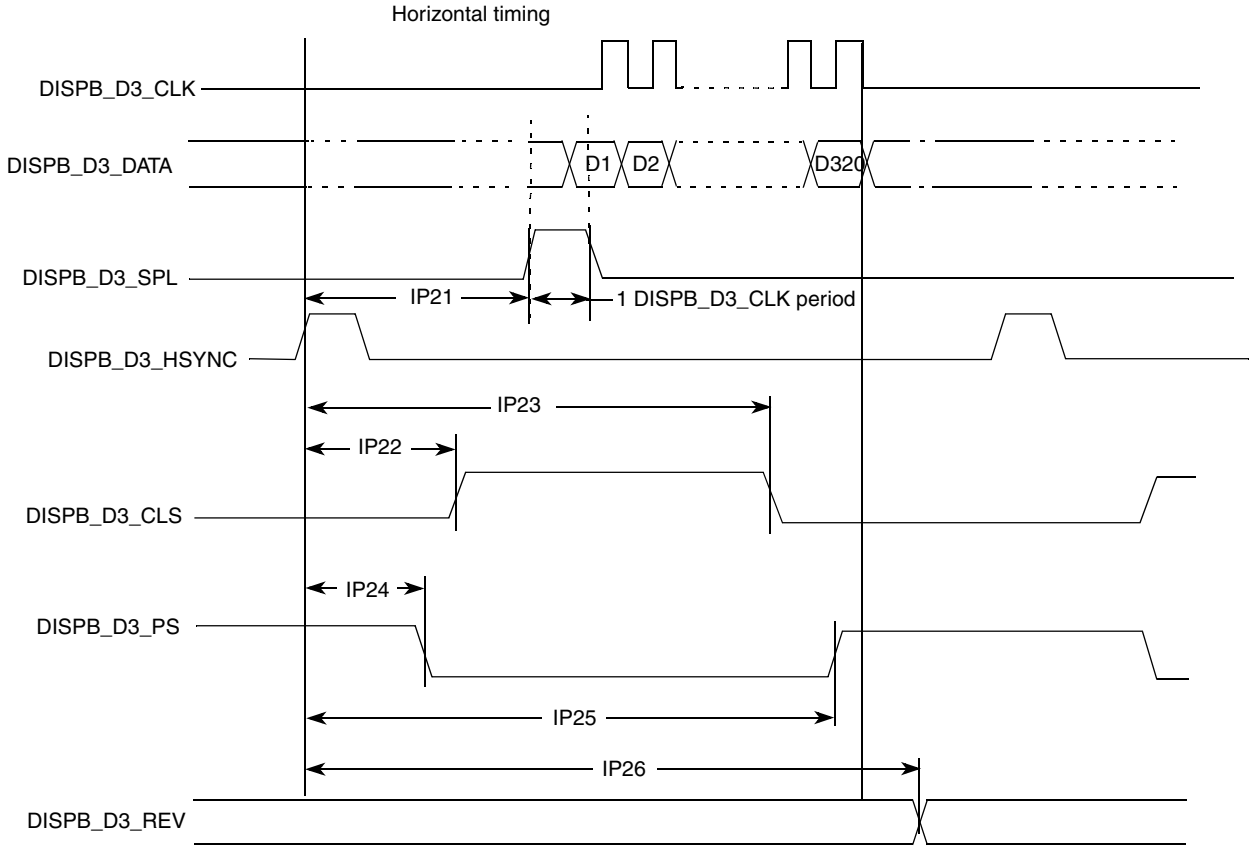


Figure 47. Interface Timing Diagram for TFT (Active Matrix) Panels

4.9.13.1.5 Interface to Active Matrix TFT LCD Panels, Electrical Characteristics

Figure 48 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and the data. All figure parameters shown are programmable. The timing images correspond to inverse polarity

Section 4.9.13.1.5, “Interface to Active Matrix TFT LCD Panels, Electrical Characteristics.” The timing images correspond to straight polarity of the Sharp signals.



Example is drawn with FW + 1 = 320 pixel/line, FH + 1 = 240 lines.
SPL pulse width is fixed and aligned to the first data of the line.
REV toggles every HSYNC period.

Figure 51. Sharp HR-TFT Panel Interface Timing Diagram—Pixel Level

Table 57. Sharp Synchronous Display Interface Timing Parameters—Pixel Level

ID	Parameter	Symbol	Value	Units
IP21	SPL rise time	Tsplr	(BGXP – 1) × Tdpcp	ns
IP22	CLS rise time	Tclsr	CLS_RISE_DELAY × Tdpcp	ns
IP23	CLS fall time	Tclsf	CLS_FALL_DELAY × Tdpcp	ns
IP24	CLS rise and PS fall time	Tpsf	PS_FALL_DELAY × Tdpcp	ns
IP25	PS rise time	Tpsr	PS_RISE_DELAY × Tdpcp	ns
IP26	REV toggle time	Trev	REV_TOGGLE_DELAY × Tdpcp	ns

Additionally, the IPU allows a programmable pause between two bursts. The pause is defined in the HSP_CLK cycles. It allows the prevention of timing violation between two sequential bursts or two accesses to different displays. The range of this pause is from 4 to 19 HSP_CLK cycles.

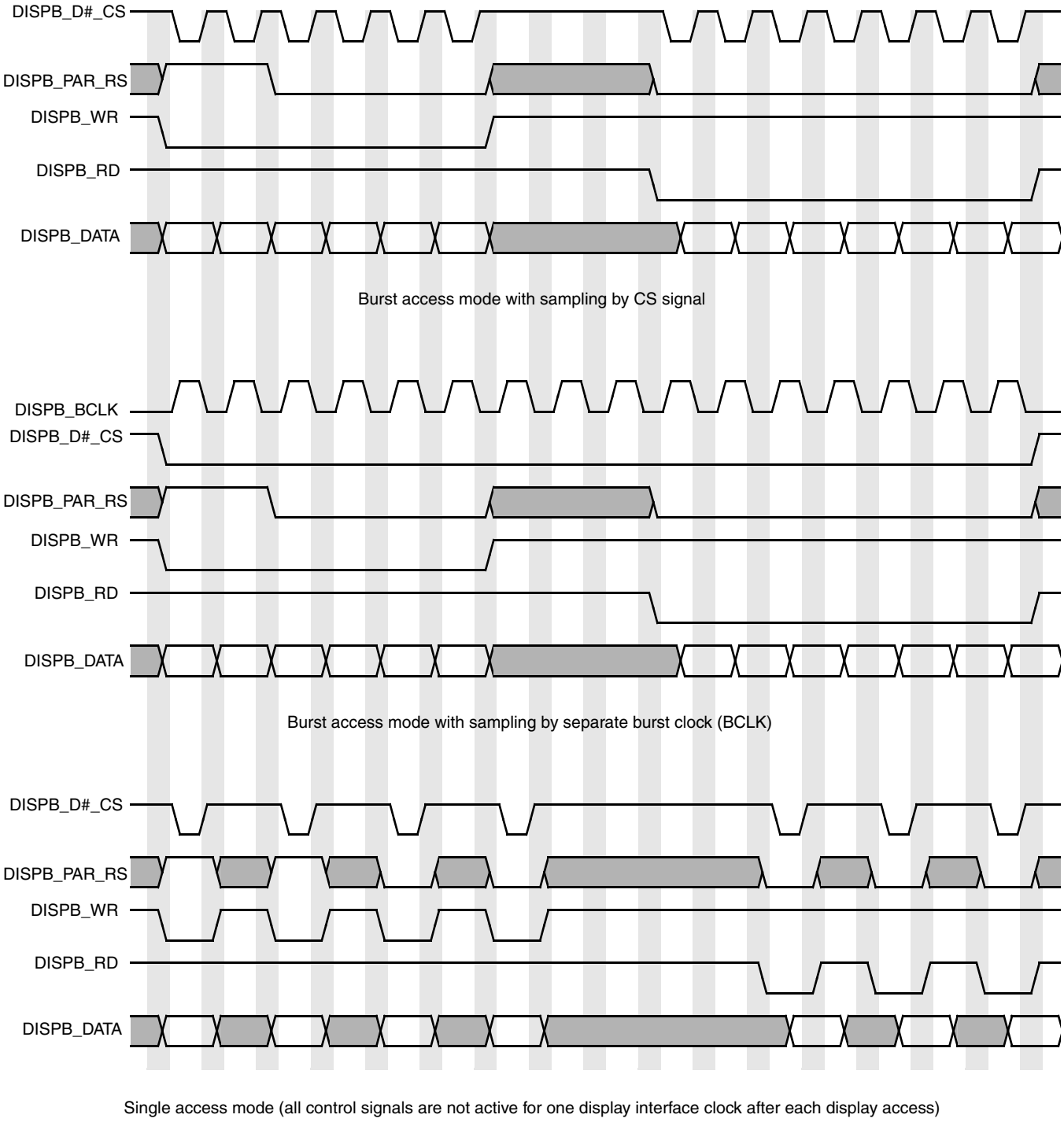


Figure 53. Asynchronous Parallel System 80 Interface (Type 1) Burst Mode Timing Diagram

timing images are based on active low control signals (signal polarity is controlled via the DI_DISP_SIG_POL register).

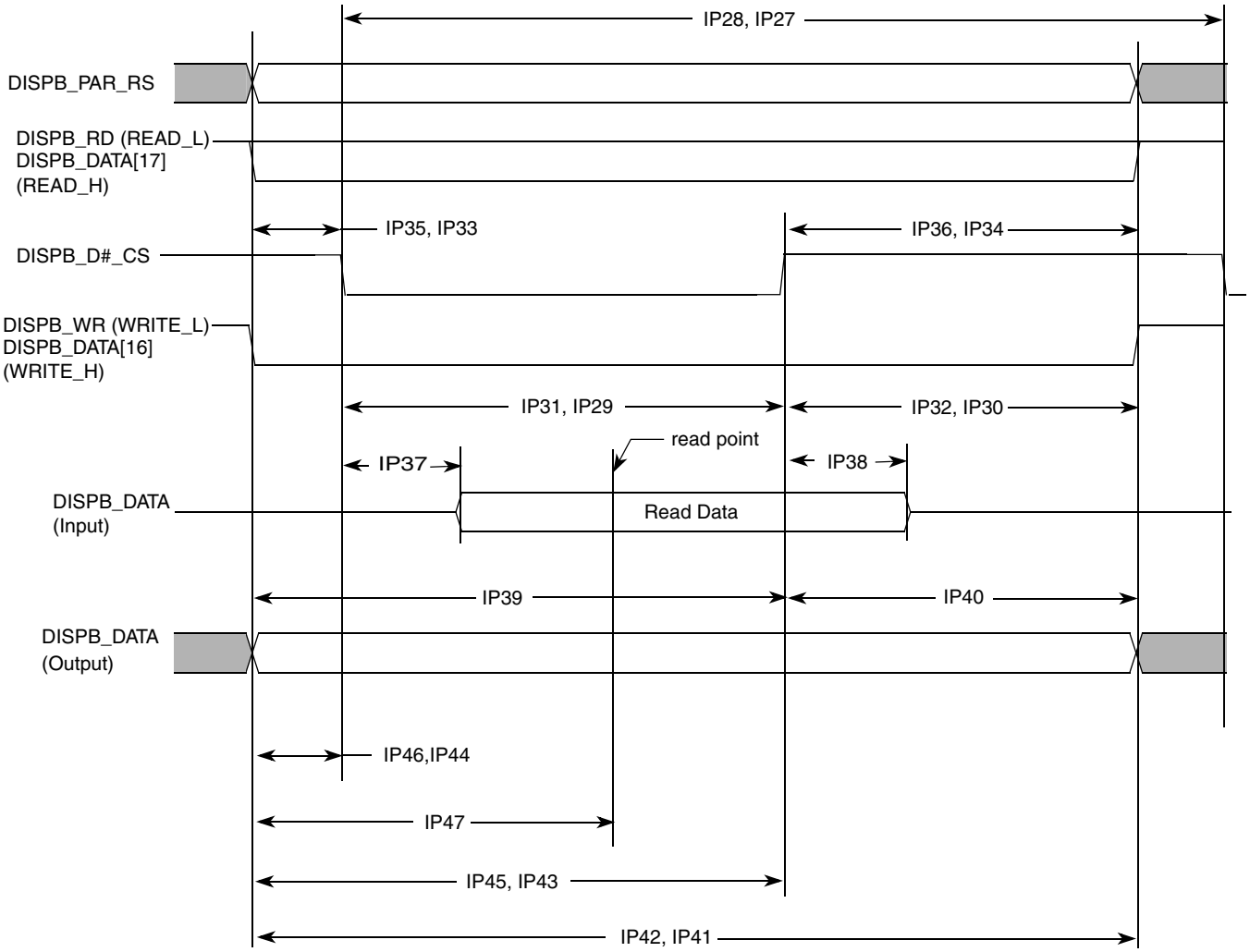


Figure 58. Asynchronous Parallel System 80 Interface (Type 1) Timing Diagram

Figure 65 depicts timing of the 5-wire serial interface (Type 2). For this interface, a separate RS line is added. When a burst is transmitted within a single active chip select interval, the RS can be changed at boundaries of words.

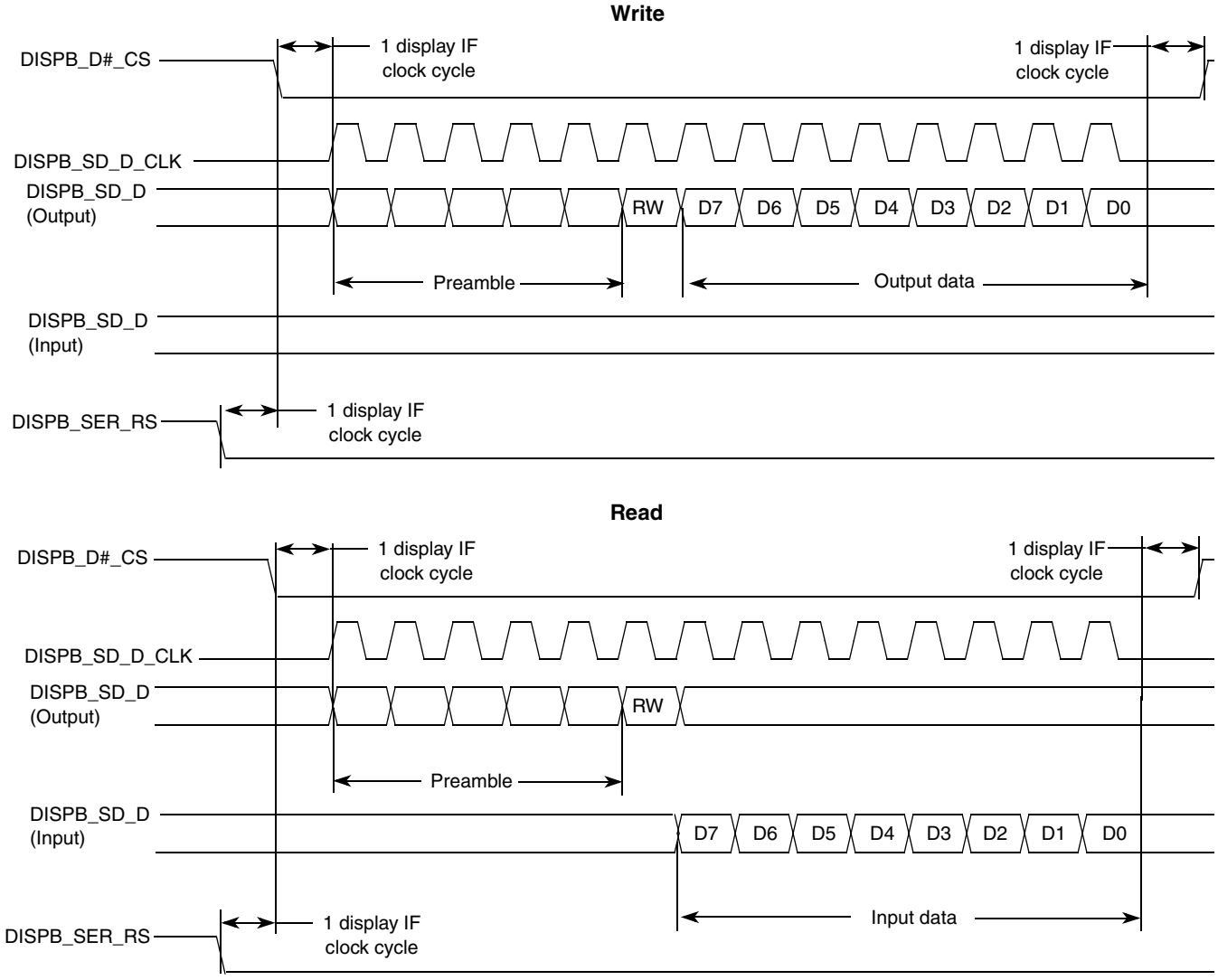


Figure 65. 5-Wire Serial Interface (Type 2) Timing Diagram

4.9.13.5.10 Serial Interfaces, Electrical Characteristics

Figure 66 depicts timing of the serial interface. Table 59 lists the timing parameters at display access level.

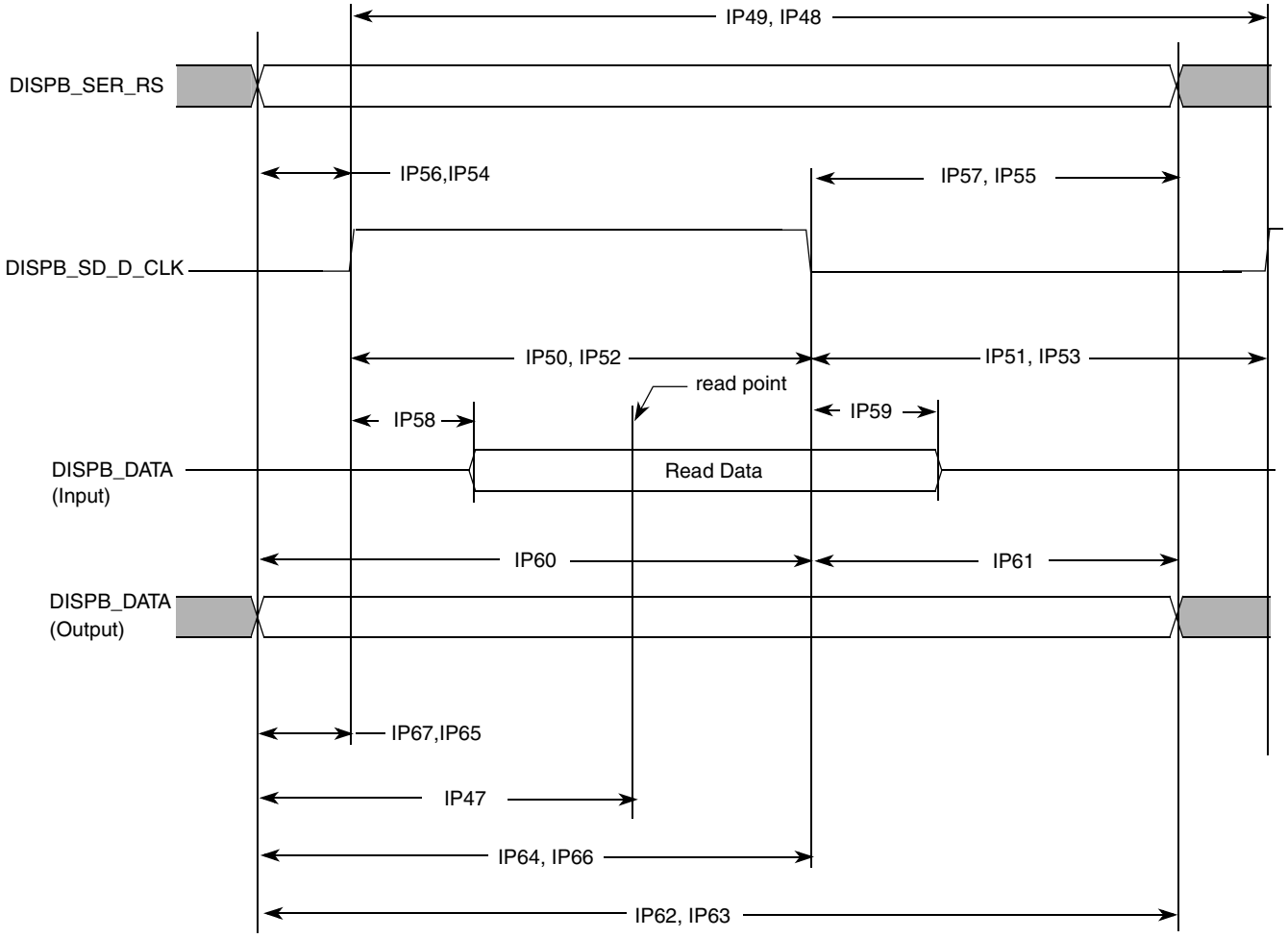


Figure 66. Asynchronous Serial Interface Timing Diagram

Table 59. Asynchronous Serial Interface Timing Parameters—Access Level

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP48	Read system cycle time	Tcycr	Tdicpr – 1.5	Tdicpr[2]	Tdicpr + 1.5	ns
IP49	Write system cycle time	Tcycw	Tdicpw – 1.5	Tdicpw[3]	Tdicpw + 1.5	ns
IP50	Read clock low pulse width	Trl	Tdicdr – Tdicur – 1.5	Tdicdr[4] – Tdicur[5]	Tdicdr – Tdicur + 1.5	ns
IP51	Read clock high pulse width	Trh	Tdicpr – Tdicdr + Tdicur – 1.5	Tdicpr – Tdicdr + Tdicur	Tdicpr – Tdicdr + Tdicur + 1.5	ns
IP52	Write clock low pulse width	Twl	Tdicdw – Tdicuw – 1.5	Tdicdw[6] – Tdicuw[7]	Tdicdw – Tdicuw + 1.5	ns
IP53	Write clock high pulse width	Twh	Tdicpw – Tdicdw + Tdicuw – 1.5	Tdicpw – Tdicdw + Tdicuw	Tdicpw – Tdicdw + Tdicuw + 1.5	ns
IP54	Controls setup time for read	Tdcsr	Tdicur – 1.5	Tdicur	—	ns

Table 59. Asynchronous Serial Interface Timing Parameters—Access Level (continued)

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP55	Controls hold time for read	Tdchr	Tdicpr – Tdicdr – 1.5	Tdicpr – Tdicdr	—	ns
IP56	Controls setup time for write	Tdcsw	Tdicuw – 1.5	Tdicuw	—	ns
IP57	Controls hold time for write	Tdchw	Tdicpw – Tdicdw – 1.5	Tdicpw – Tdicdw	—	ns
IP58	Slave device data delay[8]	Tracc	0	—	Tdrp[9] – Tlbd[10] – Tdicur – 1.5	ns
IP59	Slave device data hold time[8]	Troh	Tdrp – Tlbd – Tdicdr + 1.5	—	Tdicpr – Tdicdr – 1.5	ns
IP60	Write data setup time	Tds	Tdicdw – 1.5	Tdicdw	—	ns
IP61	Write data hold time	Tdh	Tdicpw – Tdicdw – 1.5	Tdicpw – Tdicdw	—	ns
IP62	Read period[2]	Tdicpr	Tdicpr – 1.5	Tdicpr	Tdicpr + 1.5	ns
IP63	Write period[3]	Tdicpw	Tdicpw – 1.5	Tdicpw	Tdicpw + 1.5	ns
IP64	Read down time[4]	Tdicdr	Tdicdr – 1.5	Tdicdr	Tdicdr + 1.5	ns
IP65	Read up time[5]	Tdicur	Tdicur – 1.5	Tdicur	Tdicur + 1.5	ns
IP66	Write down time[6]	Tdicdw	Tdicdw – 1.5	Tdicdw	Tdicdw + 1.5	ns
IP67	Write up time[7]	Tdicuw	Tdicuw – 1.5	Tdicuw	Tdicuw + 1.5	ns
IP68	Read time point[9]	Tdrp	Tdrp – 1.5	Tdrp	Tdrp + 1.5	ns

1 The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device specific.

2 Display interface clock period value for read:

$$Tdicpr = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_RD}{HSP\_CLK\_PERIOD}\right]$$

3 Display interface clock period value for write:

$$Tdicpw = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_WR}{HSP\_CLK\_PERIOD}\right]$$

4 Display interface clock down time for read:

$$Tdicdr = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_DOWN\_RD}{HSP\_CLK\_PERIOD}\right]$$

5 Display interface clock up time for read:

$$Tdicur = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_UP\_RD}{HSP\_CLK\_PERIOD}\right]$$

6 Display interface clock down time for write:

$$Tdicdw = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_DOWN\_WR}{HSP\_CLK\_PERIOD}\right]$$

7 Display interface clock up time for write:

$$Tdicuw = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_UP\_WR}{HSP\_CLK\_PERIOD}\right]$$

8 This parameter is a requirement to the display connected to the IPU.

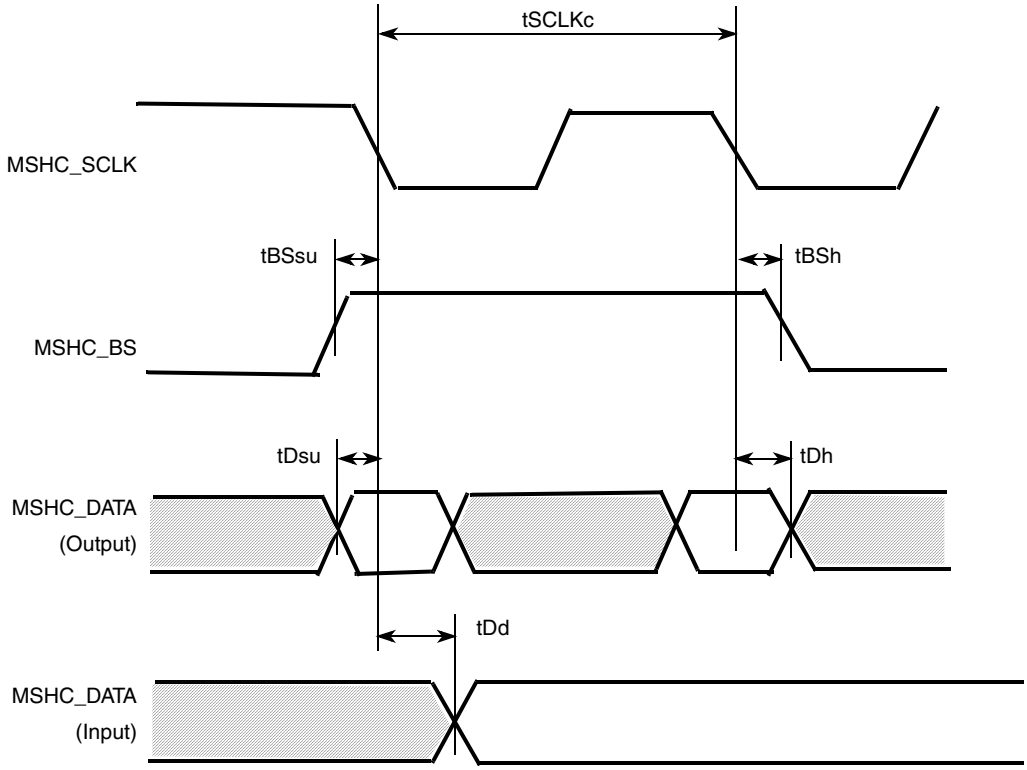


Figure 69. Transfer Operation Timing Diagram (Parallel)

NOTE

The memory stick host controller is designed to meet the timing requirements per Sony's *Memory Stick Pro Format Specifications*. Tables in this section detail the specifications' requirements for parallel and serial modes, and not the i.MX35 timing.

Table 60. Serial Interface Timing Parameters[1]

Signal	Parameter	Symbol	Standards		Unit
			Min.	Max.	
MSHC_SCLK	Cycle	tSCLKc	50	—	ns
	H pulse length	tSCLKwh	15	—	ns
	L pulse length	tSCLKwl	15	—	ns
	Rise time	tSCLKr	—	10	ns
	Fall time	tSCLKf	—	10	ns
MSHC_BS	Setup time	tBSsu	5	—	ns
	Hold time	tBSh	5	—	ns

Table 60. Serial Interface Timing Parameters[1] (continued)

Signal	Parameter	Symbol	Standards		Unit
			Min.	Max.	
MSHC_DATA	Setup time	tDsu	5	—	ns
	Hold time	tDh	5	—	ns
	Output delay time	tDd	—	15	ns

1 Timing is guaranteed for NVCC from 2.7 V through 3.1 V and up to a maximum overdrive NVCC of 3.3 V. See NVCC restrictions described in Table 61.

Table 61. Parallel Interface Timing Parameters[1]

Signal	Parameter	Symbol	Standards		Unit
			Min.	Max.	
MSHC_SCLK	Cycle	tSCLKc	25	—	ns
	H pulse length	tSCLKwh	5	—	ns
	L pulse length	tSCLKwl	5	—	ns
	Rise time	tSCLKr	—	10	ns
	Fall time	tSCLKf	—	10	ns
MSHC_BS	Setup time	tBSsu	8	—	ns
	Hold time	tBSh	1	—	ns
MSHC_DATA	Setup time	tDsu	8	—	ns
	Hold time	tDh	1	—	ns
	Output delay time	tDd	—	15	ns

1 Timing is guaranteed for NVCC from 2.7 V through 3.1 V and up to a maximum overdrive NVCC of 3.3 V. See the NVCC restrictions described in Table 8.

4.9.15 MediaLB Controller Electrical Specifications

This section describes the electrical information of the MediaLB Controller module.

Table 62. MLB 256/512 Fs Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units	Comment
MLBCLK operating frequency[1]	f_{mck}	11.264	12.288 24.576	24.6272 25.600	MHz	Min: 256 × Fs at 44.0 kHz Typ: 256 × Fs at 48.0 kHz Typ: 512 × Fs at 48.0 kHz Max: 512 × Fs at 48.1 kHz Max: 512 × Fs PLL unlocked
MLBCLK rise time	t_{mckr}	—	—	3	ns	V_{IL} TO V_{IH}

Table 71. MDMA Read and Write Timing Parameters (continued)

ATA Parameter	Parameter from Figure 77, Figure 78	Value	Controlling Variable
tn, tj	tkjn	tn = tj = tkjn = (max.(time_k,. time_jn) × T – (tskew1 + tskew2 + tskew6)	time_jn
—	ton toff	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

4.9.17.5 UDMA-In Timing

Figure 79 shows timing when the UDMA-in transfer starts, Figure 80 shows timing when the UDMA-in host terminates transfer, Figure 81 shows timing when the UDMA-in device terminates transfer, and Table 72 lists the timing parameters for the UDMA-in burst.

Figure 79. UDMA-In Transfer Starts Timing Diagram

Figure 80. UDMA-In Host Terminates Transfer Timing Diagram

Figure 81. UDMA-In Device Terminates Transfer Timing Diagram

Table 72. UDMA-In Burst Timing Parameters

ATA Parameter	Parameters from Figure 79, Figure 80, Figure 81	Description	Controlling Variable
tack	tack	tack (min.) = (time_ack × T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv (min.) = (time_env × T) – (tskew1 + tskew2) tenv (max.) = (time_env × T) + (tskew1 + tskew2)	time_env
tds	tds1	tds – (tskew3) – ti_ds > 0	tskew3, ti_ds, ti_dh should be low enough
tdh	tdh1	tdh – (tskew3) – ti_dh > 0	
tcyc	tc1	(tcyc – tskew > T	T big enough
trp	trp	trp (min.) = time_rp × T – (tskew1 + tskew2 + tskew6)	time_rp
—	tx1[1]	(time_rp × T) – (tco + tsu + 3T + 2 × tbuf + 2 × tcable2) > trfs (drive)	time_rp
tmli	tmli1	tmli1 (min.) = (time_mlix + 0.4) × T	time_mlix
tzah	tzah	tzah (min.) = (time_zah + 0.4) × T	time_zah
tdzfs	tdzfs	tdzfs = (time_dzfs × T) – (tskew1 + tskew2)	time_dzfs
tcvh	tcvh	tcvh = (time_cvh × T) – (tskew1 + tskew2)	time_cvh
—	ton toff	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

1 There is a special timing requirement in the ATA host that requires the internal DIOW to go high three clocks after the last active edge on the DSTROBE signal. The equation given on this line tries to capture this constraint.

2. Make ton and toff large enough to avoid bus contention.

4.9.17.6 UDMA-Out Timing

Figure 82 shows timing when the UDMA-out transfer starts, Figure 83 shows timing when the UDMA-out host terminates transfer, Figure 84 shows timing when the UDMA-out device terminates transfer, and Table 73 lists the timing parameters for the UDMA-out burst.

Figure 82. UDMA-Out Transfer Starts Timing Diagram

Figure 83. UDMA-Out Host Terminates Transfer Timing Diagram

Table 97. Silicon Revision 2.1 Ball Map—17 x 17, 0.8 mm Pitch (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
P	FEC_MDIO	FEC_RDATA0	FEC_COL	FEC_TX_CLK	FEC_TDATA0	NVCC_ATA	NVCC_ATA	NVCC_ATA	GND	GND	MVDD	PHY2_VSS	FUSE_VDD	NVCC_SDIO	TDI	NVCC_JTAG	USBPHY1_UPLLVDD	USBPHY1_VBUS	USBPHY1_DP	PHY1_VSSA	P
R	FEC_MDC	FEC_RX_CLK	CTS1	ATA_DA0	ATA_DA2	TXD1	VDD3	VDD3	NVCC_CRM	NVCC_MLB	NVCC_CSI	VDD4	PHY2_VDD	SD1_DATA0	TDO	TMS	TCK	USBPHY1_VSSA_BIAS	USBPHY1_REF	USBPHY1_VDDA_BIAS	R
T	FEC_TX_EN	FEC_RX_DV	ATA_DMARQ	ATA_DATA15	ATA_BUFF_EN	ATA_RESET_B	ATA_CS1	CSPI1_SPI_RDY	VSTBY	CLK_MODE1	GPIO1_0	COMPARE	SD2_DATA1	CSI_VSYNC	CSI_D11	TRSTB	GND	OSC24M_VSS	OSC24M_VDD	EXTAL24M	T
U	RTS1	RXD1	ATA_DATA12	ATA_DATA8	ATA_DATA3	ATA_IORDY	USBOTG_OC	CSPI1_SS1	BOOT_MODE1	RESET_IN_B	GPIO2_0	SD2_DATA3	SD2_CMD	CSI_D14	CSI_D8	SD1_DATA1	SJC_MOD	RTCK	OSC_AUDIO_VSS	XTAL24M	U
V	ATA_DA1	ATA_INTRQ	ATA_DATA10	ATA_DATA6	ATA_DATA2	ATA_DMACK	ATA_CS0	EXT_ARMCLK	CSPI1_MISO	CLKO	GPIO3_0	CAPTURE	SD2_DATA0	CSI_HSYNC	CSI_D13	CSI_D10	SD1_DATA3	SD1_CLK	XTAL_AUDIO	OSC_AUDIO_VDD	V
W	ATA_DATA14	ATA_DATA13	ATA_DATA9	ATA_DATA5	ATA_DATA1	ATA_DIOW	USBOTG_PWR	CSPI1_SCLK	CSPI1_MOSI	BOOT_MODE0	POR_B	MLB_SIG	MLB_CLK	SD2_CLK	CSI_MCLK	CSI_D12	CSI_D9	SD1_DATA2	DE_B	EXTAL_AUDIO	W
Y	GND	ATA_DATA11	ATA_DATA7	ATA_DATA4	ATA_DATA0	ATA_DIOR	TEST_MODE	CSPI1_SS0	POWER_FAIL	CLK_MODE0	GPIO1_1	WDOG_RST	MLB_DAT	SD2_DATA2	CSI_PIXCLK	CSI_D15	USBPHY2_DM	USBPHY2_DP	SD1_CMD	GND	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

6 Product Documentation

All related product documentation for the i.MX35 processor is located at http://www.freescale.com/imx.