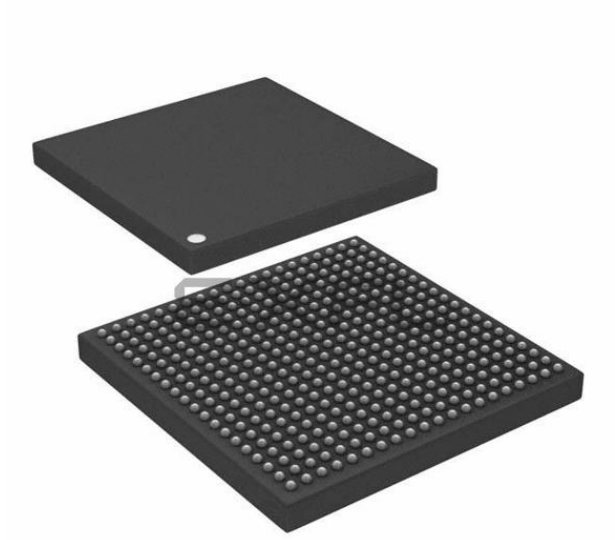


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	532MHz
Co-Processors/DSP	Multimedia; GPU, IPU, VFP
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, KPP, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Secure Fusebox, Secure JTAG
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx356ajm5b

- Branch prediction with return stack
- Low-interrupt latency
- Instruction and data memory management units (MMUs), managed using micro TLB structures backed by a unified main TLB
- Instruction and data L1 caches, including a non-blocking data cache with hit-under-miss
- Virtually indexed/physically addressed L1 caches
- 64-bit interface to both L1 caches
- Write buffer (bypassable)
- High-speed Advanced Micro Bus Architecture (AMBA)™ L2 interface
- Vector floating point co-processor (VFP) for 3D graphics and hardware acceleration of other floating-point applications
- ETM™ and JTAG-based debug support

Table 3 summarizes information about the i.MX35 core.

Table 3. i.MX35 Core

Core Acronym	Core Name	Brief Description	Integrated Memory Features
ARM11 or ARM1136	ARM1136 Platform	The ARM1136™ platform consists of the ARM1136JF-S core, the ETM real-time debug modules, a 6 × 5 multi-layer AHB crossbar switch (MAX), and a vector floating processor (VFP). The i.MX35 provides a high-performance ARM11 microprocessor core and highly integrated system functions. The ARM Application Processor (AP) and other subsystems address the needs of the personal, wireless, and portable product market with integrated peripherals, advanced processor core, and power management capabilities.	• 16-Kbyte instruction cache • 16-Kbyte data cache • 128-Kbyte L2 cache • 32-Kbyte ROM • 128-Kbyte RAM

2.5 Module Inventory

Table 4 shows an alphabetical listing of the modules in the MCIMX35. For extended descriptions of the modules, see the MCIMX35 reference manual.

Table 4. Digital and Analog Modules

Block Mnemonic	Block Name	Domain[1]	Subsystem	Brief Description
1-WIRE	1-Wire interface	ARM	ARM1136 platform peripherals	1-Wire provides the communication line to a 1-Kbit add-only memory. the interface can send or receive 1 bit at a time.
ASRC	Asynchronous sample rate converter	SDMA	Connectivity peripherals	The ASRC is designed to convert the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. It supports a concurrent sample rate conversion of about –120 dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates.

Table 4. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Domain[1]	Subsystem	Brief Description
USBOH	High-speed USB on-the-go	SDMA	Connectivity peripherals	The USB module provides high performance USB on-the-go (OTG) functionality (up to 480 Mbps), compliant with the USB 2.0 specification, the OTG supplement, and the ULPI 1.0 low pin count specification. The module has DMA capabilities handling data transfer between internal buffers and system memory.
WDOG	Watchdog modules	ARM	Timer peripherals	Each module protects against system failures by providing a method of escaping from unexpected events or programming errors. Once activated, the timer must be serviced by software on a periodic basis. If servicing does not take place, the watchdog times out and then either asserts a system reset signal or an interrupt request signal, depending on the software configuration.

1 ARM = ARM1136 platform, SDMA = SDMA platform

3 Signal Descriptions: Special Function Related Pins

Some special functional requirements are supported in the device. The details about these special functions and the corresponding pin names are listed in Table 5.

Table 5. Special Function Related Pins

Function Name	Pin Name	Mux Mode	Detailed Description
External ARM Clock	EXT_ARMCLK	ALT0	External clock input for ARM clock.
External Peripheral Clock	I2C1_CLK	ALT6	External peripheral clock source.
External 32-kHz Clock	CAPTURE	ALT4	External clock input of 32 kHz, used when the internal 24M Oscillator is powered off, which could be configured either from CAPTURE or CSPI1_SS1.
	CSPI1_SS1	ALT2	
Clock Out	CLKO	ALT0	Clock-out pin from CCM, clock source is controllable and can also be used for debug.
Power Ready	GPIO1_0	ALT1	PMIC power-ready signal, which can be configured either from GPIO1_0 or TX1.
	TX1	ALT1	
Tamper Detect	GPIO1_1	ALT6	Tamper-detect logic is used to issue a security violation. This logic is activated if the tamper-detect input is asserted. Tamper-detect logic is enabled by the bit of IOMUXC_GPRA[2]. After enabling the logic, it is impossible to disable it until the next reset.

4 Electrical Characteristics

The following sections provide the device-level and module-level electrical characteristics for the i.MX35 processor.

4.1 i.MX35 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

Table 6. i.MX35 Chip-Level Conditions

Characteristics	Table/Location
Absolute Maximum Ratings	Table 7 on page 13
i.MX35 Operating Ranges	Table 8 on page 14
Interface Frequency	Table 9 on page 15

Stresses beyond those listed in Table 7 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in Table 8 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 7. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply voltage (core)	VDD_{max}[1]	–0.5	1.47	V
Supply voltage (I/O)	$NVCC_{max}$	–0.5	3.6	V
Input voltage range	V_{Imax}	–0.5	3.6	V
Storage temperature	$T_{storage}$	–40	125	°C
ESD damage immunity:	V_{esd}			V
Human Body Model (HBM)		—	2000[2]	
Charge Device Model (CDM)		—	500[3]	

1 VDD is also known as QVCC.

2 HBM ESD classification level according to the AEC-Q100-002 standard

3 Corner pins max. 750 V

Figure 2 shows the power-up sequence and timing.

Figure 2. i.MX35 Power-Up Sequence and Timing

4.3.2 Powering Down

The power-up sequence in reverse order is recommended for powering down. However, all power supplies can be shut down at the same time.

4.4 Reset Timing

There are two ways of resetting the i.MX35 using external pins:

- Power On Reset (using the POR_B pin)
- System Reset (using the RESET_IN_B pin)

4.4.1 Power On Reset

POR_B is normally connected to a power management integrated circuit (PMIC). The PMIC asserts POR_B while the power supplies are turned on and negates POR_B after the power up sequence is finished. See Figure 2.

Table 11. Power Consumption

Power Supply	Voltage (V)	Max Current (mA)
QVCC	1.47	400
MVDD, PVDD	1.65	20
NVCC_EMI1, NVCC_EMI2, NVCC_EMI3, NVCC_LCDC, NVCC_NFC	1.9	90
FUSE_VDD[1]	3.6	62
NVCC_MISC, NVCC_CSI, NVCC_SDIO, NVCC_CRM, NVCC_ATA, NVCC_MLB, NVCC_JTAG	3.6	60
OSC24M_VDD, OSC_AUDIO_VDD, PHY1_VDDA, PHY2_VDD, USBPHY1_UPLLVDD, USBPHY1_VDDA_BIAS	3.6	25

1 This rail is connected to ground; it only needs a voltage if eFuses are to be programmed. FUSE_VDD should be supplied by following the power up sequence given in Section 4.3.1, “Powering Up.”

The method for obtaining max current is as follows:

1. Measure worst case power consumption on individual rails using directed test on i.MX35.
2. Correlate worst case power consumption power measurements with worst case power consumption simulations.
3. Combine common voltage rails based on power supply sequencing requirements
4. Guard band worst case numbers for temperature and process variation. Guard band is based on process data and correlated with actual data measured on i.MX35.
5. The sum of individual rails is greater than real world power consumption, as a real system does not typically maximize power consumption on all peripherals simultaneously.

4.6 Thermal Characteristics

The thermal resistance characteristics for the device are given in Table 12. These values were measured under the following conditions:

- Two-layer substrate
- Substrate solder mask thickness: 0.025 mm
- Substrate metal thicknesses: 0.016 mm
- Substrate core thickness: 0.200 mm
- Core via I.D: 0.168 mm, Core via plating 0.016 mm.
- Full array map design, but nearly all balls under die are power or ground.
- Die Attach: 0.033 mm non-conductive die attach, k = 0.3 W/m K
- Mold compound: k = 0.9 W/m K

Table 12. Thermal Resistance Data

Rating	Condition	Symbol	Value	Unit
Junction to ambient[1] natural convection	Single layer board (1s)	$R_{\theta JA}$	53	ºC/W
Junction to ambient[1] natural convection	Four layer board (2s2p)	$R_{\theta JA}$	30	ºC/W

Table 19. AC Electrical Characteristics, GPIO Pins in Fast Slew Rate Mode [NVCC = 1.65 V–1.95 V]

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	—	60	%
Output pin slew rate (max. drive)	tps	25 pF 50 pF	0.40/0.57 0.25/0.36	0.72/0.97 0.43/0.61	1.2/1.5 0.72/0.95	V/ns
Output pin slew rate (high drive)	tps	25 pF 50 pF	0.38/0.48 0.20/0.30	0.59/0.81 0.34/0.50	0.98/1.27 0.56/0.72	V/ns
Output pin slew rate (standard drive)	tps	25 pF 50 pF	0.23/0.32 0.13/0.20	0.40/0.55 0.23/0.34	0.66/0.87 0.38/0.52	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	7 7	43 46	112 118	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	11 12	31 33	81 85	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	9 10	27 28	71 74	mA/ns

Table 20. AC Electrical Characteristics of GPIO Pins in Slow Slew Rate Mode [NVCC = 2.25 V–2.75 V]

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	—	60	%
Output pin slew rate (max. drive)	tps	25 pF 40 pF 50 pF	0.63/0.85 0.52/0.67 0.41/0.59	1.10/1.40 0.90/1.10 0.73/0.99	1.86/2.20 1.53/1.73 1.20/1.50	V/ns
Output pin slew rate (high drive)	tps	25 pF 40 pF 50 pF	0.40/0.58 0.33/0.43 0.25/0.37	0.71/0.98 0.56/0.70 0.43/0.60	1.16/1.40 0.93/1.07 0.68/0.90	V/ns
Output pin slew rate (standard drive)	tps	25 pF 40 pF 50 pF	0.24/0.36 0.19/0.25 0.13/0.21	0.41/0.59 0.32/0.35 0.23/0.33	0.66/0.87 0.51/0.59 0.36/0.48	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	22 23	62 65	148 151	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	15 16	42 44	102 107	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	7 8	21 22	52 54	mA/ns

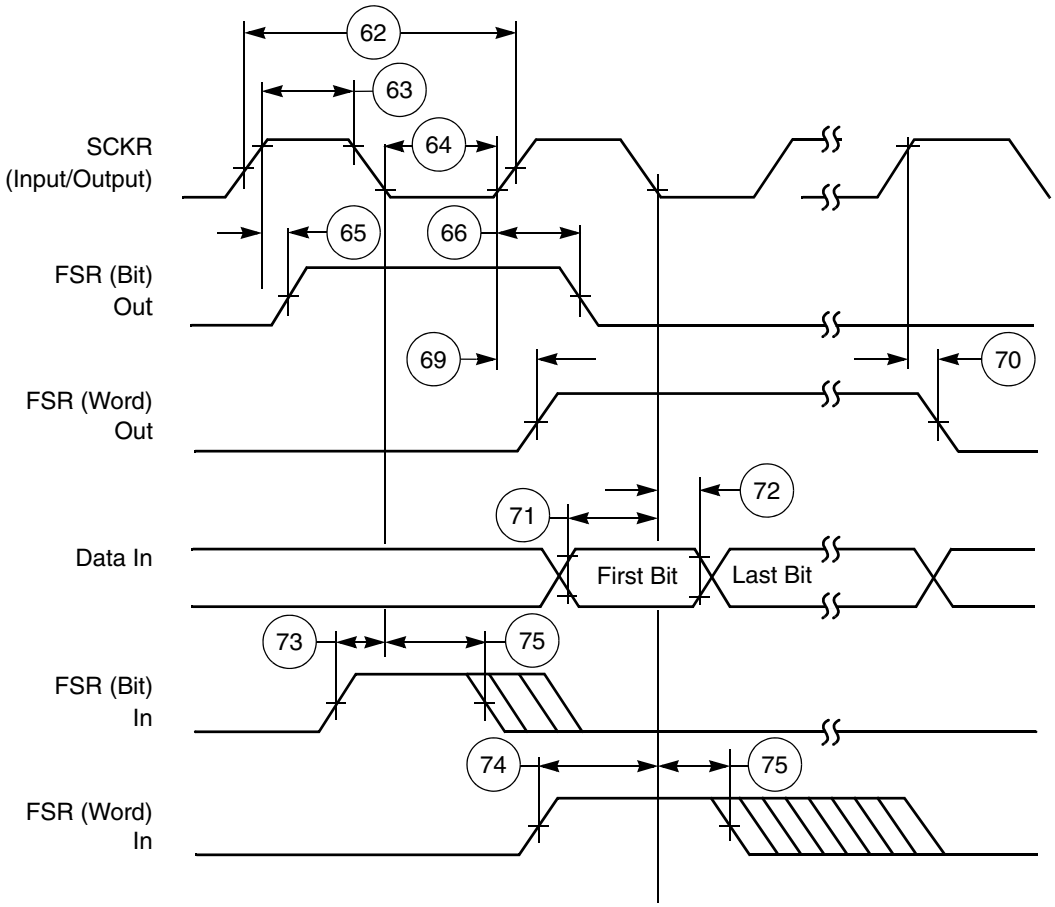


Figure 37. ESAI Receiver Timing

4.9.7 eSDHCv2 AC Electrical Specifications

Figure 38 depicts the timing of eSDHCv2, and Table 47 lists the eSDHCv2 timing characteristics. The following definitions apply to values and signals described in Table 47:

- LS: low-speed mode. Low-speed card can tolerate a clock up to 400 kHz.
- FS: full-speed mode. For a full-speed MMC card, the card clock can reach 20 MHz; a full-speed SD/SDIO card can reach 25 MHz.
- HS: high-speed mode. For a high-speed MMC card, the card clock can reach 52 MHz; SD/SDIO can reach 50 MHz.

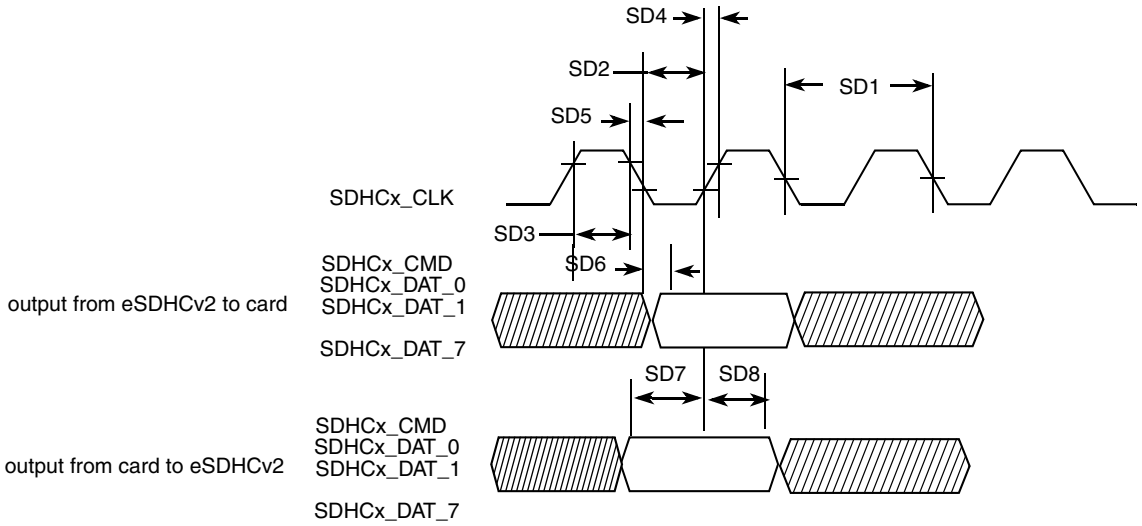


Figure 38. eSDHCv2 Timing

Table 47. eSDHCv2 Interface Timing Specification

ID	Parameter	Symbols	Min.	Max.	Unit
Card Input Clock					
SD1	Clock frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low time	t_{WL}	7	—	ns
SD3	Clock high time	t_{WH}	7	—	ns
SD4	Clock rise time	t_{TLH}	—	3	ns
SD5	Clock fall time	t_{THL}	—	3	ns
eSDHC Output/Card Inputs CMD, DAT (Reference to CLK)					
SD6	eSDHC output delay	t_{OD}	–3	3	ns
eSDHC Input/Card Outputs CMD, DAT (Reference to CLK)					
SD7	eSDHC input setup time	t_{ISU}	5	—	ns
SD8	eSDHC input hold time	t_{IH}[4]	2.5	—	ns

1 In low-speed mode, the card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal-speed mode for the SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.

3 In normal-speed mode for MMC card, clock frequency can be any value between 0 and 20 MHz. In high-speed mode, clock frequency can be any value between 0–52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

Figure 41 shows MII asynchronous input timings listed in Table 50.

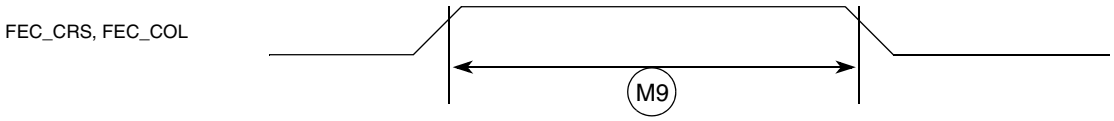


Figure 41. MII Asynch Inputs Timing Diagram

4.9.8.5 MII Serial Management Channel Timing

Serial management channel timing is accomplished using FEC_MDIO and FEC_MDC. The FEC functions correctly with a maximum MDC frequency of 2.5 MHz. Table 51 lists MII serial management channel timings.

The MDC frequency should be equal to or less than 2.5 MHz to be compliant with the IEEE 802.3 MII specification. However the FEC can function correctly with a maximum MDC frequency of 15 MHz.

Table 51. MII Transmit Signal Timing

Num	Characteristic	Min.	Max.	Units
M10	FEC_MDC falling edge to FEC_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	FEC_MDC falling edge to FEC_MDIO output valid (max. propagation delay)	—	5	ns
M12	FEC_MDIO (input) to FEC_MDC rising edge setup	18	—	ns
M13	FEC_MDIO (input) to FEC_MDC rising edge hold	0	—	ns
M14	FEC_MDC pulse width high	40%	60%	FEC_MDC period
M15	FEC_MDC pulse width low	40%	60%	FEC_MDC period

4.9.11 I²C AC Electrical Specifications

This section describes the electrical characteristics of the I²C module.

4.9.11.1 I²C Module Timing

Figure 43 depicts the timing of the I²C module. Table 52 lists the I²C module timing parameters.

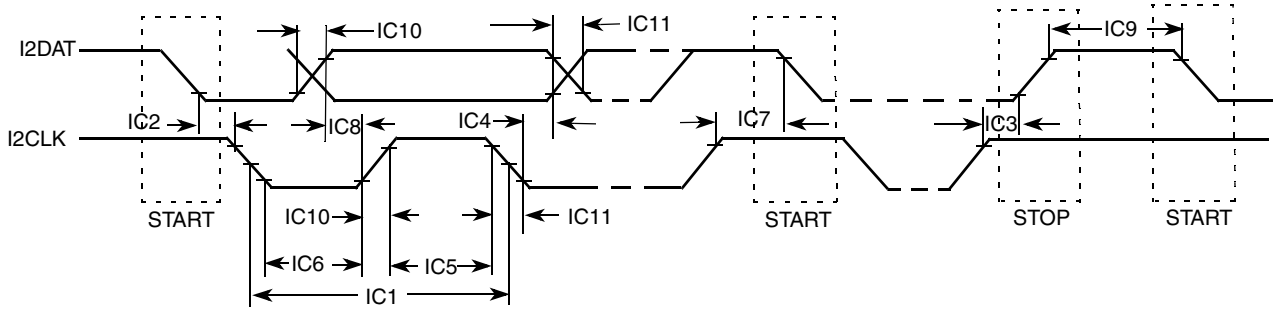


Figure 43. I²C Bus Timing Diagram

Table 52. I²C Module Timing Parameters

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
IC1	I2CLK cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2CLK Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2CLK Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2DAT and I2CLK signals	—	1000	—	300	ns
IC11	Fall time of both I2DAT and I2CLK signals	—	300	—	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for the I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

2 The maximum hold time has to be met only if the device does not stretch the LOW period (ID IC6) of the I2CLK signal.

3 A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement of set-up time (ID IC7) of 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the I2CLK signal. If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line max_rise_time (ID No IC10) + data_setup_time (ID No IC8) = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the I2CLK line is released.

Table 56. Synchronous Display Interface Timing Parameters—Access Level

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP16	Display interface clock low time	Tckl	Tdicd – Tdicu – 1.5	Tdicd[2] – Tdicu[3]	Tdicd – Tdicu + 1.5	ns
IP17	Display interface clock high time	Tckh	Tdicp – Tdicd + Tdicu – 1.5	Tdicp – Tdicd + Tdicu	Tdicp – Tdicd + Tdicu + 1.5	ns
IP18	Data setup time	Tdsu	Tdicd – 3.5	Tdicu	—	ns
IP19	Data holdup time	Tdhd	Tdicp – Tdicd – 3.5	Tdicp – Tdicu	—	ns
IP20	Control signals setup time to display interface clock	Tcsu	Tdicd – 3.5	Tdicu	—	ns

1 The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device specific.

2 Display interface clock down time

$$Tdicd = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP3\_IF\_CLK\_DOWN\_WR}{HSP\_CLK\_PERIOD}\right]$$

3 Display interface clock up time

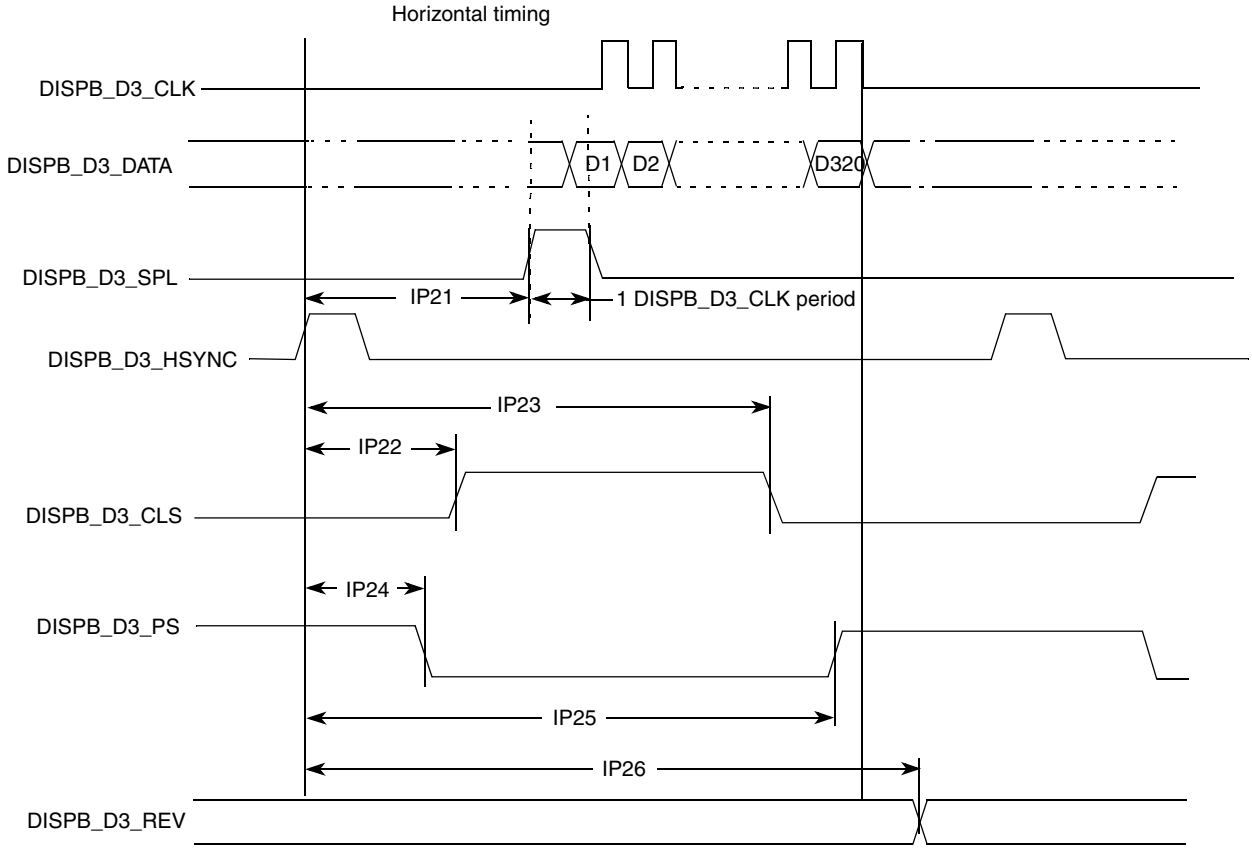
$$Tdicu = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP3\_IF\_CLK\_UP\_WR}{HSP\_CLK\_PERIOD}\right]$$

where CEIL(X) rounds the elements of X to the nearest integers toward infinity.

4.9.13.2 Interface to Sharp HR-TFT Panels

Figure 51 depicts the Sharp HR-TFT panel interface timing, and Table 57 lists the timing parameters. The CLS_RISE_DELAY, CLS_FALL_DELAY, PS_FALL_DELAY, PS_RISE_DELAY, REV_TOGGLE_DELAY parameters are defined in the SDC_SHARP_CONF_1 and SDC_SHARP_CONF_2 registers. For other Sharp interface timing characteristics, refer to

Section 4.9.13.1.5, “Interface to Active Matrix TFT LCD Panels, Electrical Characteristics.” The timing images correspond to straight polarity of the Sharp signals.



Example is drawn with FW + 1 = 320 pixel/line, FH + 1 = 240 lines.
SPL pulse width is fixed and aligned to the first data of the line.
REV toggles every HSYNC period.

Figure 51. Sharp HR-TFT Panel Interface Timing Diagram—Pixel Level

Table 57. Sharp Synchronous Display Interface Timing Parameters—Pixel Level

ID	Parameter	Symbol	Value	Units
IP21	SPL rise time	Tsplr	(BGXP – 1) × Tdpcp	ns
IP22	CLS rise time	Tclsr	CLS_RISE_DELAY × Tdpcp	ns
IP23	CLS fall time	Tclsf	CLS_FALL_DELAY × Tdpcp	ns
IP24	CLS rise and PS fall time	Tpsf	PS_FALL_DELAY × Tdpcp	ns
IP25	PS rise time	Tpsr	PS_RISE_DELAY × Tdpcp	ns
IP26	REV toggle time	Trev	REV_TOGGLE_DELAY × Tdpcp	ns

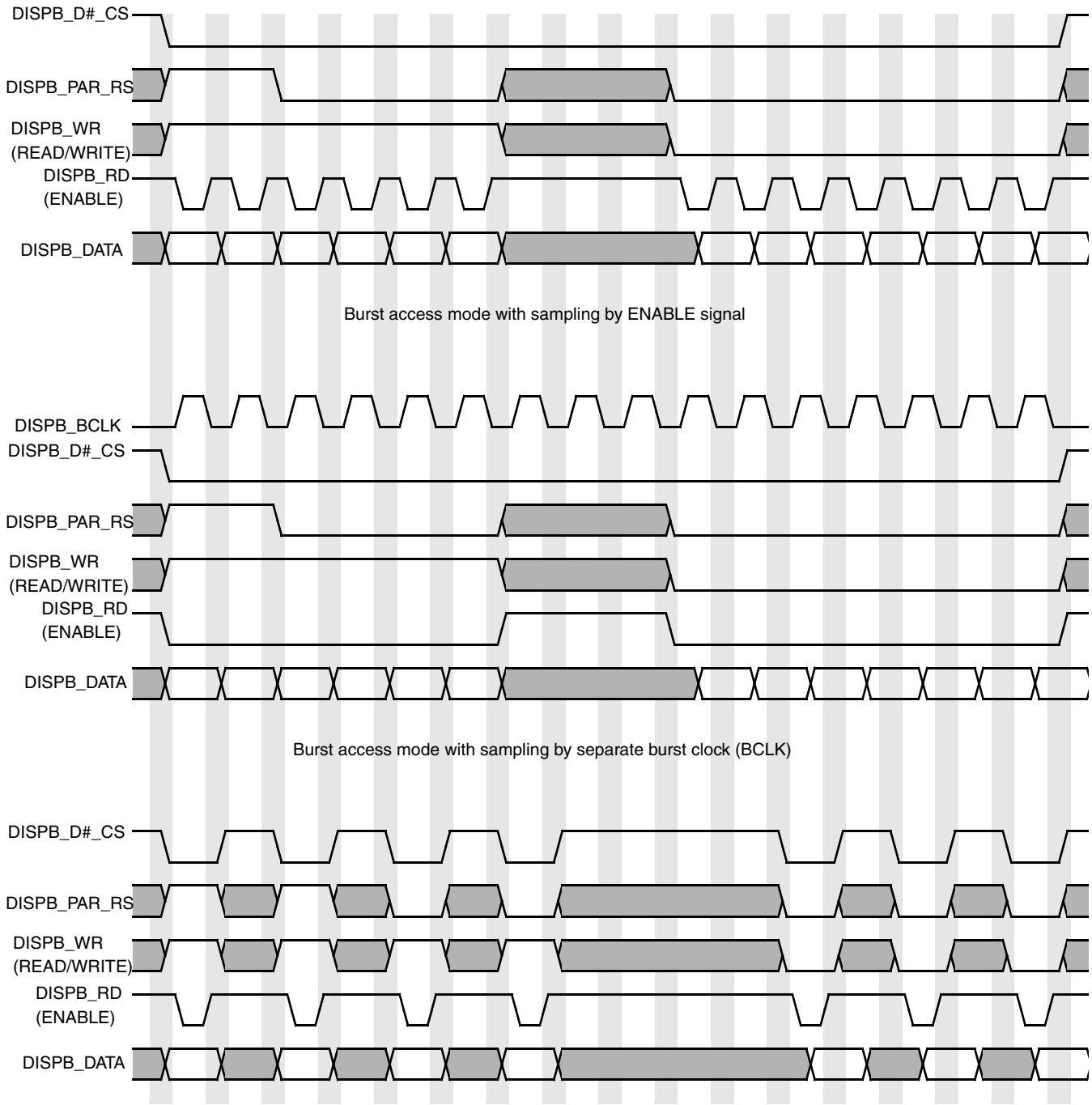


Figure 56. Asynchronous Parallel System 68k Interface (Type 2) Burst Mode TIming Diagram

Display read operation can be performed with wait states when each read access takes up to 4 display interface clock cycles according to the DISP0_RD_WAIT_ST parameter in the

[9] Data read point

$$Tdrp = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_READ\_EN}{HSP\_CLK\_PERIOD}\right]$$

[10] Loopback delay Tlbd is the cumulative propagation delay of read controls and read data. It includes an IPU output delay, a device – level output delay, board delays, a device – level input delay, an IPU input delay. This value is device specific.

The following parameters are programmed via the DI_DISP#_TIME_CONF_1, DI_DISP#_TIME_CONF_2, and DI_HSP_CLK_PER registers:

- DISP#_IF_CLK_PER_WR, DISP#_IF_CLK_PER_RD
- HSP_CLK_PERIOD
- DISP#_IF_CLK_DOWN_WR
- DISP#_IF_CLK_UP_WR
- DISP#_IF_CLK_DOWN_RD
- DISP#_IF_CLK_UP_RD
- DISP#_READ_EN

4.9.13.5 Serial Interfaces, Functional Description

The IPU supports the following types of asynchronous serial interfaces:

- 3-wire (with bidirectional data line)
- 4-wire (with separate data input and output lines)
- 5-wire type 1 (with sampling RS by the serial clock)
- 5-wire type 2 (with sampling RS by the chip select signal)

Figure 62 depicts timing of the 3-wire serial interface. The timing images correspond to active-low DISPB_D#_CS signal and the straight polarity of the DISPB_SD_D_CLK signal.

For this interface, a bidirectional data line is used outside the device. The IPU still uses separate input and output data lines (IPP_IND_DISPB_SD_D and IPP_DO_DISPB_SD_D). The I/O mux connects the internal data lines to the bidirectional external line according to the IPP_OBE_DISPB_SD_D signal provided by the IPU.

Each data transfer can be preceded by an optional preamble with programmable length and contents. The preamble is followed by read/write (RW) and address (RS) bits. The order of the these bits is programmable. The RW bit can be disabled. The following data can consist of one word or of a whole burst. The interface parameters are controlled by the DI_SER_DISP*n*_CONF registers (*n* = 1, 2).

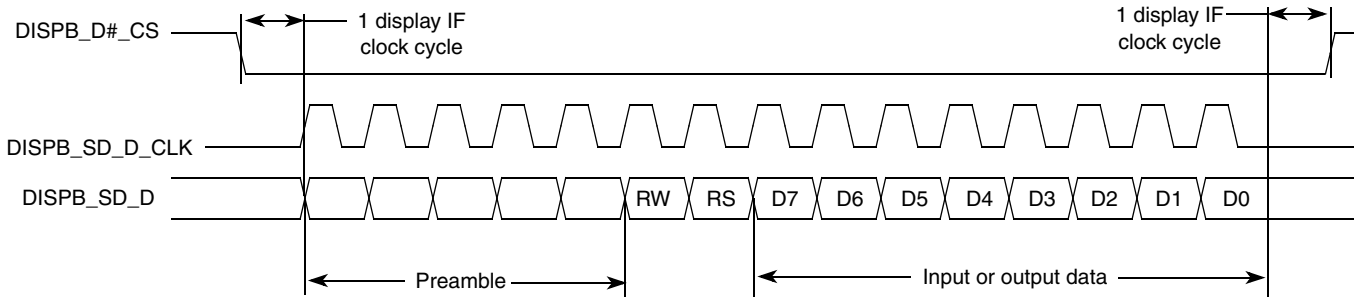


Figure 62. 3-Wire Serial Interface Timing Diagram

Figure 63 depicts timing of the 4-wire serial interface. For this interface, there are separate input and output data lines both inside and outside the device.

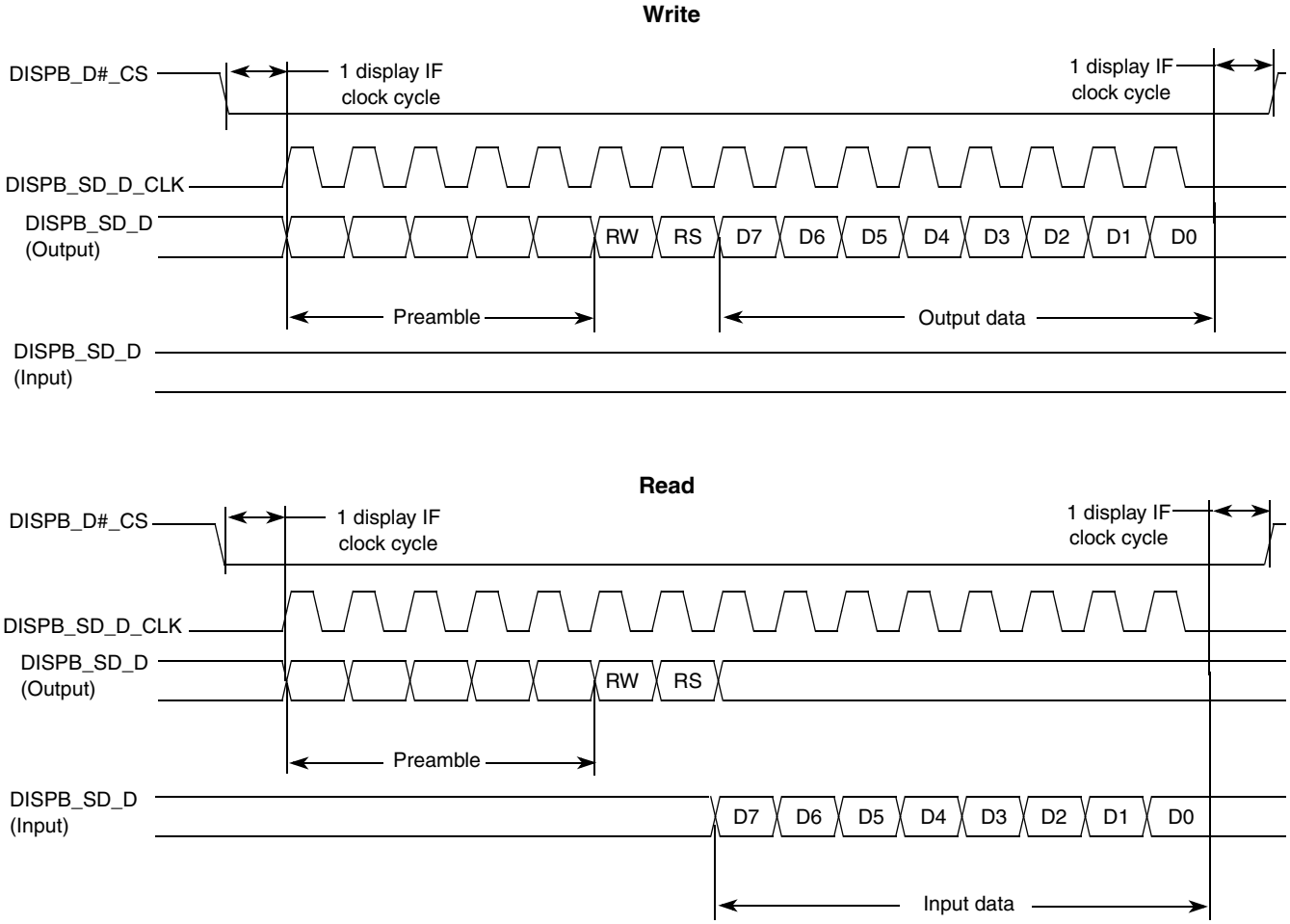


Figure 63. 4-Wire Serial Interface Timing Diagram

4.9.17.4 PIO Mode Timing

Figure 75 shows timing for PIO read, and Table 69 lists the timing parameters for PIO read.

Figure 75. PIO Read Timing Diagram

Table 69. PIO Read Timing Parameters

ATA Parameter	Parameter from Figure 75	Value	Controlling Variable
t1	t1	t1 (min.) = time_1 × T – (tskew1 + tskew2 + tskew5)	time_1
t2	t2r	t2 min.) = time_2r × T – (tskew1 + tskew2 + tskew5)	time_2r
t9	t9	t9 (min.) = time_9 × T – (tskew1 + tskew2 + tskew6)	time_3
t5	t5	t5 (min.) = tco + tsu + tbuf + tbuf + tcable1 + tcable2	If not met, increase time_2
t6	t6	0	—
tA	tA	tA (min.) = (1.5 + time_ax) × T – (tco + tsui + tcable2 + tcable2 + 2 × tbuf)	time_ax
trd	trd1	trd1 (max.) = (–trd) + (tskew3 + tskew4) trd1 (min.) = (time_pio_rdx – 0.5) × T – (tsu + thi) (time_pio_rdx – 0.5) × T > tsu + thi + tskew3 + tskew4	time_pio_rdx
t0	—	t0 (min.) = (time_1 + time_2 + time_9) × T	time_1, time_2r, time_9

Figure 77 shows timing for MDMA read, and Figure 78 shows timing for MDMA write. Table 71 lists the timing parameters for MDMA read and write.

Figure 77. MDMA Read Timing Diagram

Figure 78. MDMA Write Timing Diagram

Table 71. MDMA Read and Write Timing Parameters

ATA Parameter	Parameter from Figure 77, Figure 78	Value	Controlling Variable
tm, ti	tm	tm (min.) = ti (min.) = time_m × T – (tskew1 + tskew2 + tskew5)	time_m
td	td, td1	td1.(min.) = td (min.) = time_d × T – (tskew1 + tskew2 + tskew6)	time_d
tk	tk	tk.(min.) = time_k × T – (tskew1 + tskew2 + tskew6)	time_k
t0	—	t0 (min.) = (time_d + time_k) × T	time_d, time_k
tg(read)	tgr	tgr (min. – read) = tco + tsu + tbuf + tbuf + tcable1 + tcable2 tgr.(min. – drive) = td – te(drive)	time_d
tf(read)	tfr	tfr (min. – drive) = 0	—
tg(write)	—	tg (min. – write) = time_d × T – (tskew1 + tskew2 + tskew5)	time_d
tf(write)	—	tf (min. – write) = time_k × T – (tskew1 + tskew2 + tskew6)	time_k
tL	—	tL (max.) = (time_d + time_k–2) × T – (tsu + tco + 2 × tbuf + 2 × tcable2)	time_d, time_k

4.9.18 Parallel Interface (ULPI) Timing

Electrical and timing specifications of the parallel interface are presented in the subsequent sections.

Table 74. Signal Definitions—Parallel Interface

Name	Direction	Signal Description
USB_Clk	In	Interface clock. All interface signals are synchronous to the clock.
USB_Data[7:0]	I/O	Bidirectional data bus, driven low by the link during idle. Bus ownership is determined by Dir.
USB_Dir	In	Direction. Control the direction of the data bus.
USB_Stp	Out	Stop. The link asserts this signal for 1 clock cycle to stop the data stream currently on the bus.
USB_Nxt	In	Next. The PHY asserts this signal to throttle the data.

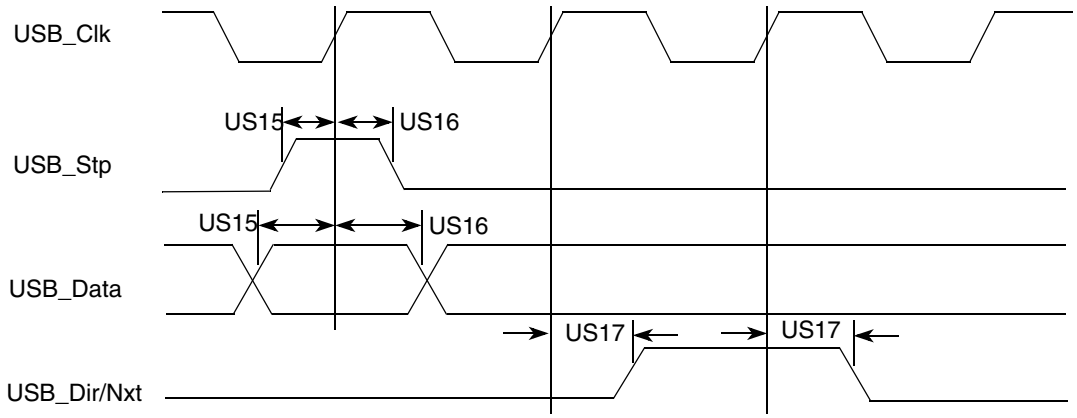


Figure 85. USB Transmit/Receive Waveform in Parallel Mode

Table 75. USB Timing Specification in VP_VM Unidirectional Mode

ID	Parameter	Min.	Max.	Unit	Conditions / Reference Signal
US15	USB_TXOE_B	—	6.0	ns	10 pF
US16	USB_DAT_VP	—	0.0	ns	10 pF
US17	USB_SE0_VM	—	9.0	ns	10 pF

4.9.19 PWM Electrical Specifications

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external

4.9.24.1 DAT_SE0 Bidirectional Mode

Table 86 defines the signals for DAT_SE0 bidirectional mode. Figure 100 and Figure 101 show the transmit and receive waveforms respectively.

Table 86. Signal Definitions—DAT_SE0 Bidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out In	Tx data when USB_TXOE_B is low Differential Rx data when USB_TXOE_B is high
USB_SE0_VM	Out In	SE0 drive when USB_TXOE_B is low SE0 Rx indicator when USB_TXOE_B is high

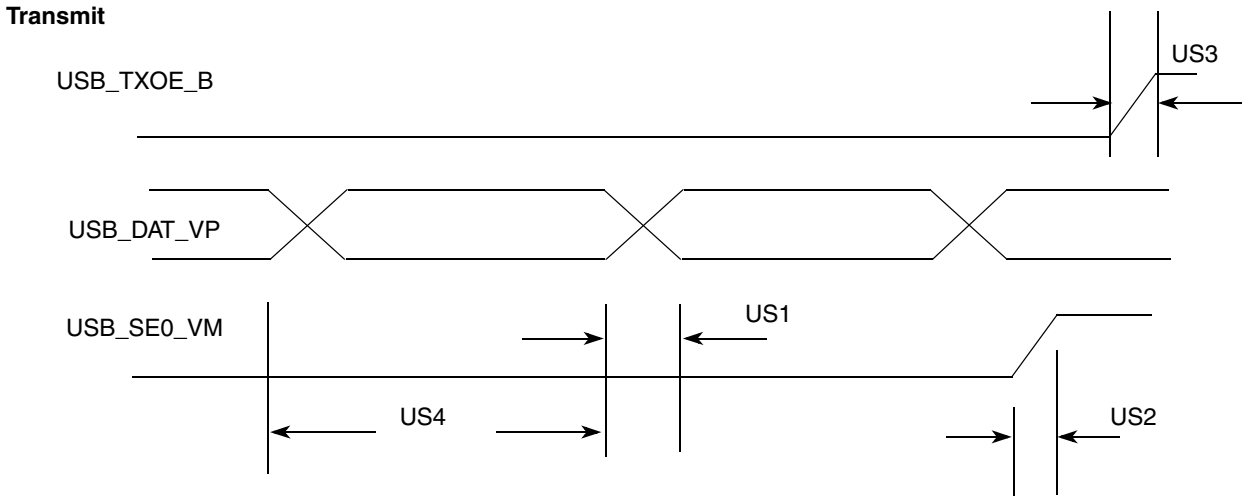


Figure 100. USB Transmit Waveform in DAT_SE0 Bidirectional Mode

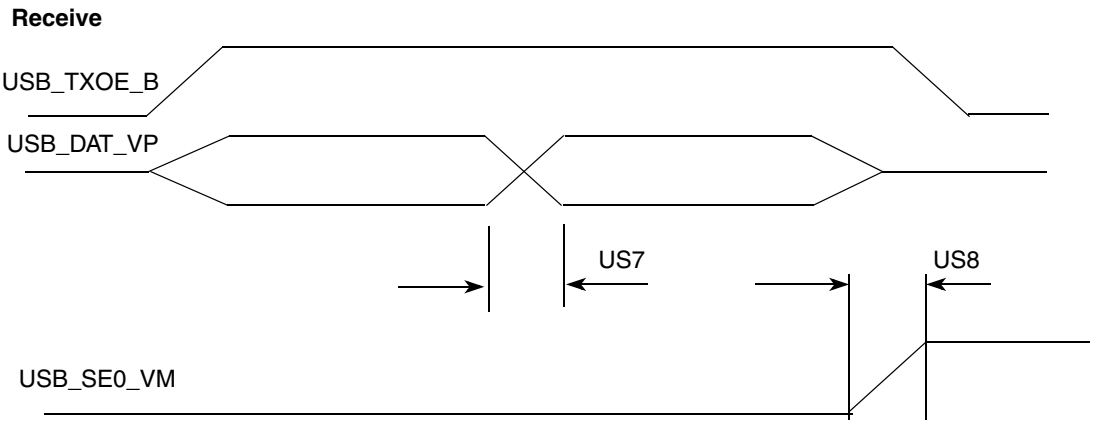


Figure 101. USB Receive Waveform in DAT_SE0 Bidirectional Mode

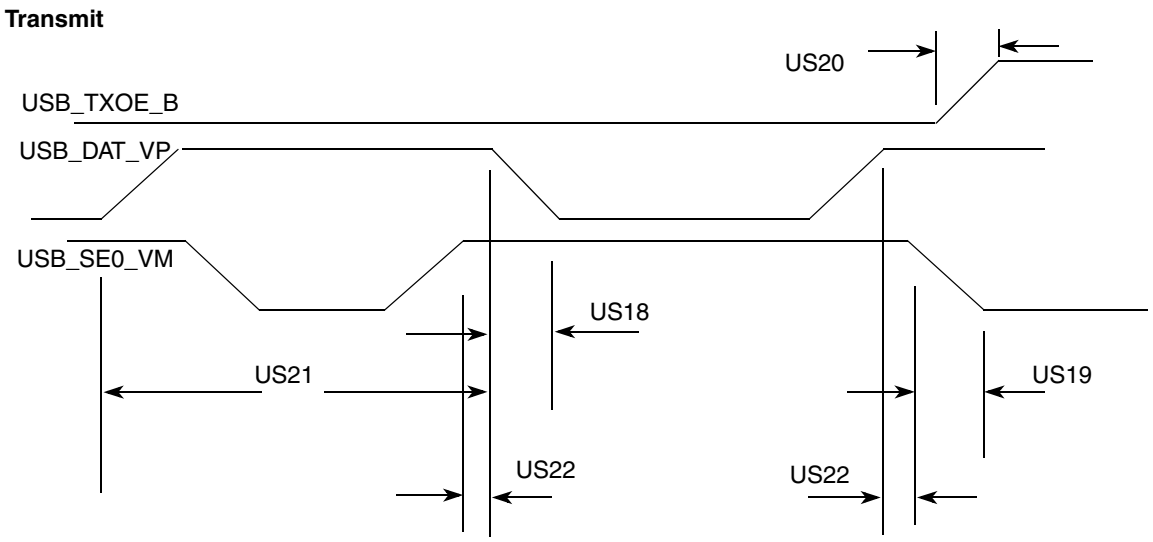


Figure 104. USB Transmit Waveform in VP_VM Bidirectional Mode

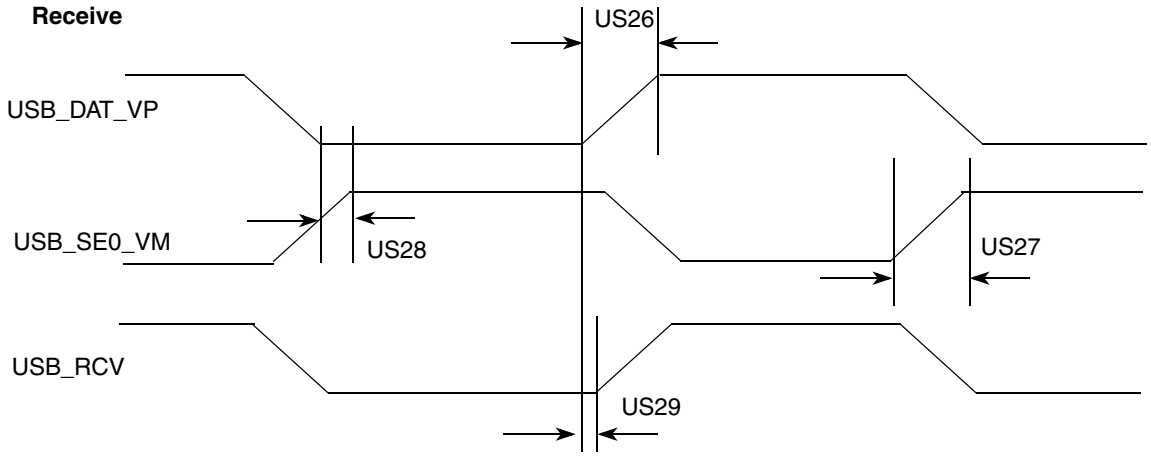


Figure 105. USB Receive Waveform in VP_VM Bidirectional Mode

Table 91 describes the port timing specification in VP_VM bidirectional mode.

Table 91. USB Port Timing Specification in VP_VM Bidirectional Mode

No.	Parameter	Signal Name	Direction	Min.	Max.	Unit	Condition/ Reference Signal
US18	Tx rise/fall time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US19	Tx rise/fall time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US20	Tx rise/fall time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US21	Tx duty cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US22	Tx overlap	USB_SE0_VM	Out	–3.0	+3.0	ns	USB_DAT_VP
US26	Rx rise/fall time	USB_DAT_VP	In	—	3.0	ns	35 pF
US27	Rx rise/fall time	USB_SE0_VM	In	—	3.0	ns	35 pF