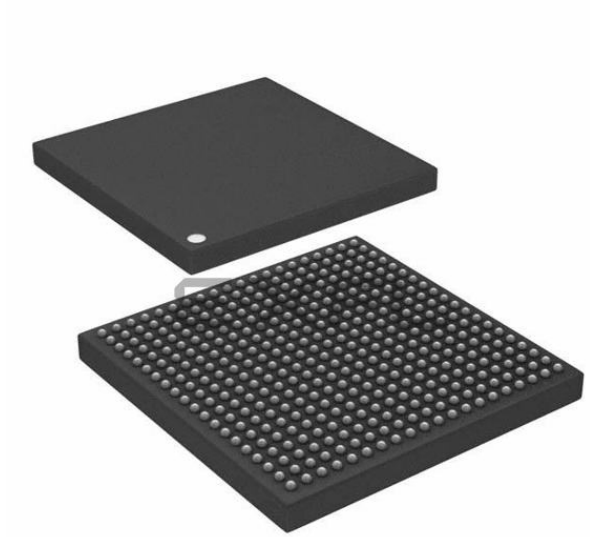

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	532MHz
Co-Processors/DSP	Multimedia; GPU, IPU, VFP
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, KPP, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Secure Fusebox, Secure JTAG
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx356ajm5br2

Table 4. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Domain[1]	Subsystem	Brief Description
ATA	ATA module	SDMA	Connectivity peripherals	The ATA block is an AT attachment host interface. Its main use is to interface with IDE hard disk drives and ATAPI optical disk drives. It interfaces with the ATA device over a number of ATA signals.
AUDMUX	Digital audio mux	ARM	Multimedia peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (SSIs) and peripheral serial interfaces (audio codecs). The AUDMUX has two sets of interfaces: internal ports to on-chip peripherals and external ports to off-chip audio devices. Data is routed by configuring the appropriate internal and external ports.
CAN(2)	CAN module	ARM	Connectivity peripherals	The CAN protocol is primarily designed to be used as a vehicle serial data bus running at 1 Mbps.
CCM	Clock control module	ARM	Clocks	This block generates all clocks for the peripherals in the SDMA platform. The CCM also manages ARM1136 platform low-power modes (WAIT, STOP), disabling peripheral clocks appropriately for power conservation, and provides alternate clock sources for the ARM1136 and SDMA platforms.
CSPI(2)	Configurable serial peripheral interface	SDMA, ARM	Connectivity peripherals	This module is a serial interface equipped with data FIFOs; each master/slave-configurable SPI module is capable of interfacing to both serial port interface master and slave devices. The CSPI ready (SPI_RDY) and slave select (SS) control signals enable fast data communication with fewer software interrupts.
ECT	Embedded cross trigger	SDMA, ARM	Debug	ECT (embedded cross trigger) is an IP for real-time debug purposes. It is a programmable matrix allowing several subsystems to interact with each other. ECT receives signals required for debugging purposes (from cores, peripherals, buses, external inputs, and so on) and propagates them (propagation programmed through software) to the different debug resources available within the SoC.
EMI	External memory interface	SDMA	External memory interface	The EMI module provides access to external memory for the ARM and other masters. It is composed of the following main submodules: M3IF—provides arbitration between multiple masters requesting access to the external memory. SDRAM CTRL—interfaces to mDDR, DDR2 (4-bank architecture type), and SDR interfaces. NANDFC—provides an interface to NAND Flash memories. WEIM—interfaces to NOR Flash and PSRAM.
EPIT(2)	Enhanced periodic interrupt timer	ARM	Timer peripherals	Each EPIT is a 32-bit “set-and-forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler to adjust the input clock frequency to the required time setting for the interrupts, and the counter value can be programmed on the fly.

4 Electrical Characteristics

The following sections provide the device-level and module-level electrical characteristics for the i.MX35 processor.

4.1 i.MX35 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

Table 6. i.MX35 Chip-Level Conditions

Characteristics	Table/Location
Absolute Maximum Ratings	Table 7 on page 13
i.MX35 Operating Ranges	Table 8 on page 14
Interface Frequency	Table 9 on page 15

Stresses beyond those listed in Table 7 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in Table 8 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 7. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply voltage (core)	VDD_{max}[1]	–0.5	1.47	V
Supply voltage (I/O)	$NVCC_{max}$	–0.5	3.6	V
Input voltage range	V_{Imax}	–0.5	3.6	V
Storage temperature	$T_{storage}$	–40	125	°C
ESD damage immunity:	V_{esd}			V
Human Body Model (HBM)		—	2000[2]	
Charge Device Model (CDM)		—	500[3]	

1 VDD is also known as QVCC.

2 HBM ESD classification level according to the AEC-Q100-002 standard

3 Corner pins max. 750 V

Table 17. AC Electrical Characteristics of GPIO Pins in Slow Slew Rate Mode [NVCC = 1.65 V–1.95 V]

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	—	60	%
Output pin slew rate (max. drive)	tps	25 pF 50 pF	0.30/0.42 0.20/0.29	0.54/0.73 0.35/0.50	0.91/1.20 0.60/0.80	V/ns
Output pin slew rate (high drive)	tps	25 pF 50 pF	0.19/0.28 0.12/0.18	0.34/0.49 0.34/0.49	0.58/0/79 0.36/0.49	V/ns
Output pin slew rate (standard drive)	tps	25 pF 50 pF	0.12/0.18 0.07/0.11	0.20/0.30 0.11/0.17	0.34/0.47 0.20/0.27	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	7 7	21 22	56 58	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	5 5	14 15	38 40	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	2 2	7 7	18 19	mA/ns

Table 18. AC Electrical Characteristics of GPIO Pins in Fast Slew Rate Mode for [NVCC = 3.0 V–3.6 V]

Parameter	Symbol	Test Condition	Min. rise/fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	—	60	%
Output pin slew rate (max. drive)	tps	25 pF 50 pF	0.96/1.40 0.54/0.83	1.54/2.10 0.85/1.24	2.30/3.00 1.26/1.70	V/ns
Output pin slew rate (high drive)	tps	25 pF 50 pF	0.76/1.10 0.41/0.64	1.19/1.71 0.63/0.95	1.78/2.39 0.95/1.30	V/ns
Output pin slew rate (standard drive)	tps	25 pF 50 pF	0.52/0.78 0.28/0.44	0.80/1.19 0.43/0.64	1.20/1.60 0.63/0.87	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	46 49	108 113	250 262	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	35 37	82 86	197 207	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	22 23	52 55	116 121	mA/ns

4.9.5.3 ESDCTL Electrical Specifications

Figure 27 through Figure 35 depict the timings pertaining to the ESDCTL module, which interfaces with mobile DDR or SDR SDRAM. Table 35 through Table 45 list the timing parameters.

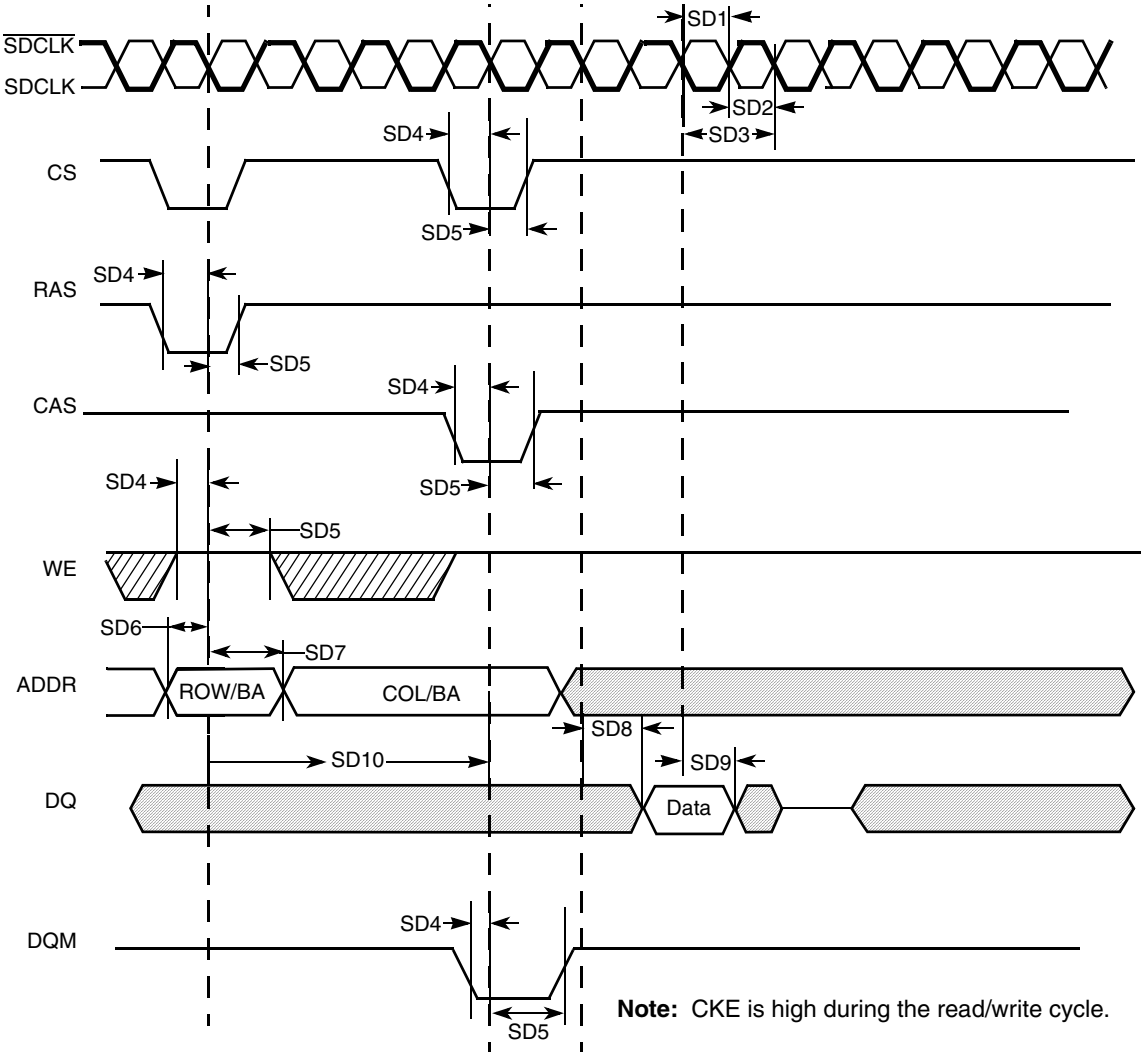


Figure 27. SDRAM Read Cycle Timing Diagram

Table 35. DDR/SDR SDRAM Read Cycle Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD1	SDRAM clock high-level width	tCH	3.4	4.1	ns
SD2	SDRAM clock low-level width	tCL	3.4	4.1	ns
SD3	SDRAM clock cycle time	tCK	7.0	—	ns
SD4	CS, RAS, CAS, WE, DQM, CKE setup time	tCMS	2.0	—	ns
SD5	CS, RAS, CAS, WE, DQM, CKE hold time	tCMH	1.8	—	ns
SD6	Address setup time	tAS	2.0	—	ns

Table 39. DDR2 SDRAM Timing Parameter Table

ID	PARAMETER	Symbol	DDR2-400		Unit
			Min	Max	
DDR5	CS, RAS, CAS, CKE, WE hold time	t_{IH}[1]	1.25	—	ns
DDR6	Address output setup time	t_{IS}[1]	1.5	—	ns
DDR7	Address output hold time	t_{IH}[1]	1.5	—	ns

NOTE

These values are for command/address slew rate of 1 V/ns and SDCLK, SDCLK_B differential slew rate of 2 V/ns. For different values, use the derating table.

Table 40. Derating Values for DDR2–400, DDR2–533

Table 42. DDR Single-ended Slew Rate

NOTE

SDR SDRAM CLK parameters are measured from the 50% point—that is, "high" is defined as 50% of signal value and "low" is defined as 50% of signal value. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and $\overline{\text{SDCLK}}$ (inverted clock).

Test conditions are: Capacitance 15 pF for DDR PADS. Recommended drive strength is Medium for SDCLK and High for Address and controls.

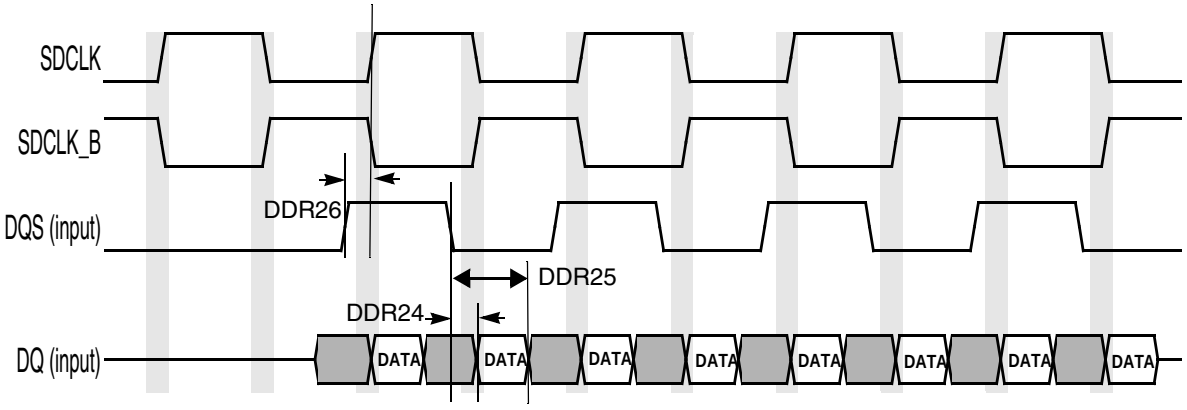


Figure 33. DDR2 SDRAM DQ vs. DQS and SDCLK READ Cycle Timing Diagram

4.9.12 IPU—Sensor Interfaces

This section contains a list of supported camera sensors, a functional description, and the electrical characteristics.

4.9.12.1 Supported Camera Sensors

Table 53 lists the known supported camera sensors at the time of publication.

Table 53. Supported Camera Sensors[1]

Vendor	Model
Conexant	CX11646, CX20490[2], CX20450[2]
Agilant	HDCP–2010, ADCS–1021[2], ADCS–1021[2]
Toshiba	TC90A70
ICMedia	ICM202A, ICM102[2]
iMagic	IM8801
Transchip	TC5600, TC5600J, TC5640, TC5700, TC6000
Fujitsu	MB86S02A
Micron	MI-SOC–0133
Matsushita	MN39980
STMicro	W6411, W6500, W6501[2], W6600[2], W6552[2], STV0974[2]
OmniVision	OV7620, OV6630, OV2640
Sharp	LZ0P3714 (CCD)
Motorola	MC30300 (Python)[2], SCM20014[2], SCM20114[2], SCM22114[2], SCM20027[2]
National Semiconductor	LM9618[2]

1 Freescale Semiconductor does not recommend one supplier over another and in no way suggests that these are the only camera suppliers.

2 These sensors have not been validated at the time of publication.

4.9.12.2 Functional Description

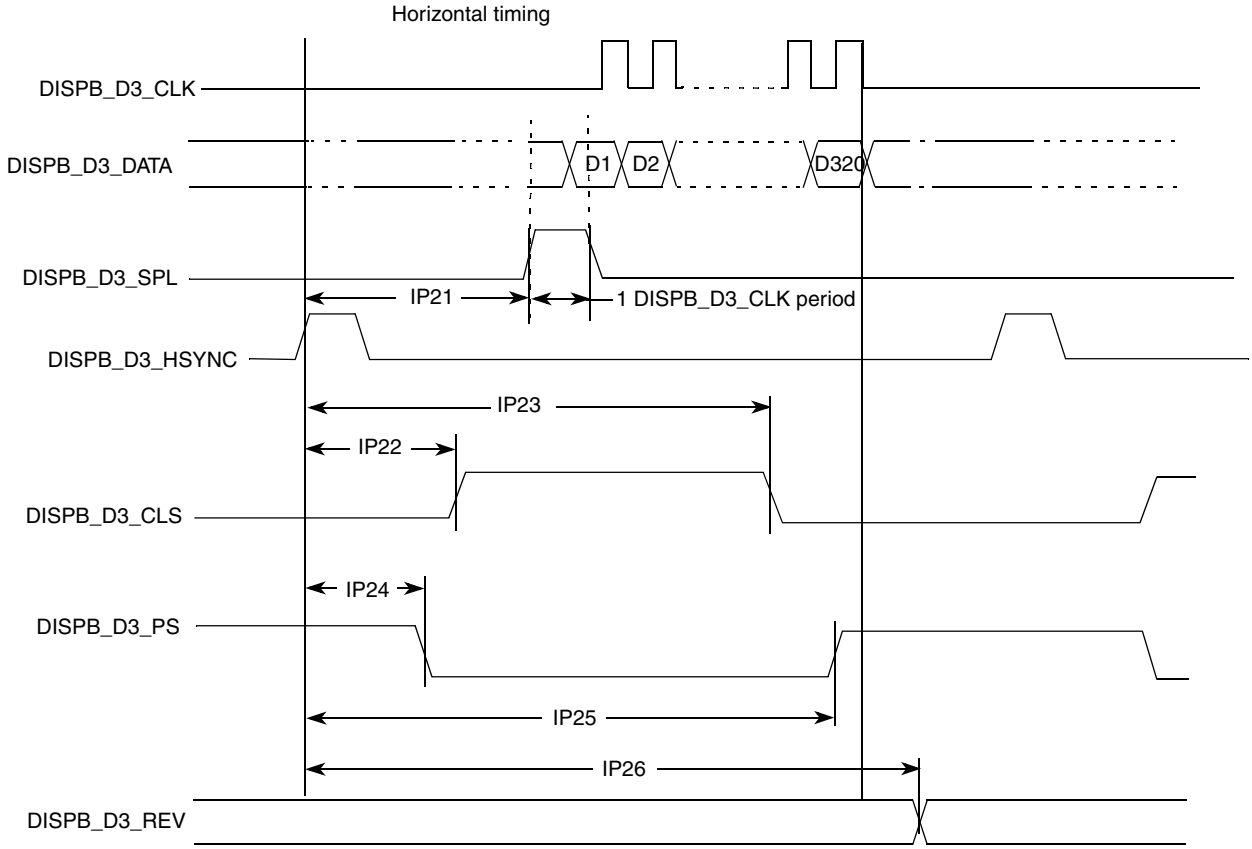
There are three timing modes supported by the IPU.

4.9.12.2.1 Pseudo BT.656 Video Mode

Smart camera sensors, which typically include image processing capability, support video mode transfer operations. They use an embedded timing syntax to replace the SENSB_VSYNC and SENSB_HSYNC signals. The timing syntax is defined by the BT.656 standard.

This operation mode follows the recommendations of the ITU BT.656 specifications. The only control signal used is SENSB_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with an EAV code. In some cases, digital blanking is

Section 4.9.13.1.5, “Interface to Active Matrix TFT LCD Panels, Electrical Characteristics.” The timing images correspond to straight polarity of the Sharp signals.



Example is drawn with FW + 1 = 320 pixel/line, FH + 1 = 240 lines.
SPL pulse width is fixed and aligned to the first data of the line.
REV toggles every HSYNC period.

Figure 51. Sharp HR-TFT Panel Interface Timing Diagram—Pixel Level

Table 57. Sharp Synchronous Display Interface Timing Parameters—Pixel Level

ID	Parameter	Symbol	Value	Units
IP21	SPL rise time	Tsplr	(BGXP – 1) × Tdpcp	ns
IP22	CLS rise time	Tclsr	CLS_RISE_DELAY × Tdpcp	ns
IP23	CLS fall time	Tclsf	CLS_FALL_DELAY × Tdpcp	ns
IP24	CLS rise and PS fall time	Tpsf	PS_FALL_DELAY × Tdpcp	ns
IP25	PS rise time	Tpsr	PS_RISE_DELAY × Tdpcp	ns
IP26	REV toggle time	Trev	REV_TOGGLE_DELAY × Tdpcp	ns

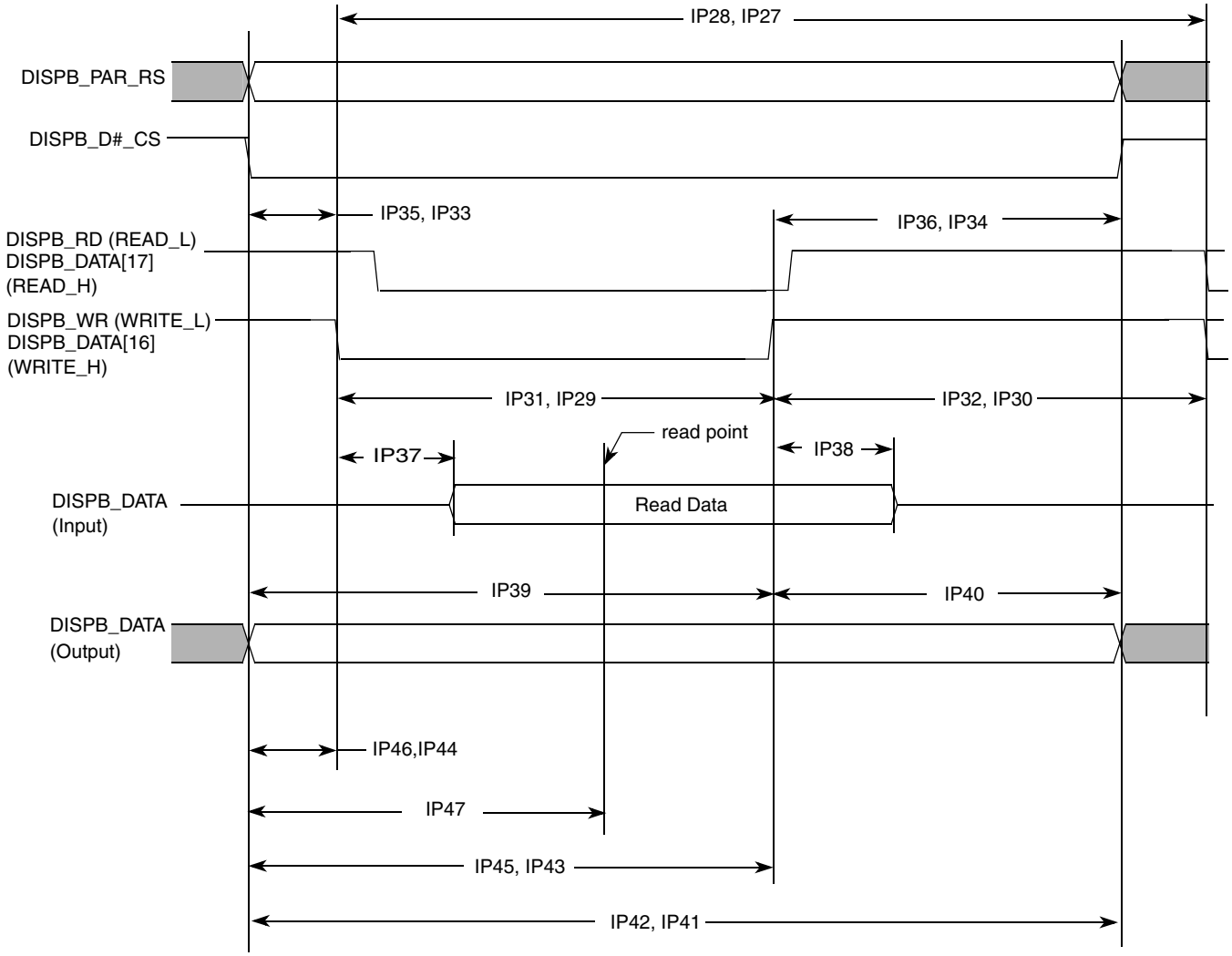


Figure 59. Asynchronous Parallel System 80 Interface (Type 2) Timing Diagram

[9] Data read point

$$Tdrp = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_READ\_EN}{HSP\_CLK\_PERIOD}\right]$$

[10] Loopback delay Tlbd is the cumulative propagation delay of read controls and read data. It includes an IPU output delay, a device – level output delay, board delays, a device – level input delay, an IPU input delay. This value is device specific.

The following parameters are programmed via the DI_DISP#_TIME_CONF_1, DI_DISP#_TIME_CONF_2, and DI_HSP_CLK_PER registers:

- DISP#_IF_CLK_PER_WR, DISP#_IF_CLK_PER_RD
- HSP_CLK_PERIOD
- DISP#_IF_CLK_DOWN_WR
- DISP#_IF_CLK_UP_WR
- DISP#_IF_CLK_DOWN_RD
- DISP#_IF_CLK_UP_RD
- DISP#_READ_EN

4.9.13.5 Serial Interfaces, Functional Description

The IPU supports the following types of asynchronous serial interfaces:

- 3-wire (with bidirectional data line)
- 4-wire (with separate data input and output lines)
- 5-wire type 1 (with sampling RS by the serial clock)
- 5-wire type 2 (with sampling RS by the chip select signal)

Figure 62 depicts timing of the 3-wire serial interface. The timing images correspond to active-low DISPB_D#_CS signal and the straight polarity of the DISPB_SD_D_CLK signal.

For this interface, a bidirectional data line is used outside the device. The IPU still uses separate input and output data lines (IPP_IND_DISPB_SD_D and IPP_DO_DISPB_SD_D). The I/O mux connects the internal data lines to the bidirectional external line according to the IPP_OBE_DISPB_SD_D signal provided by the IPU.

Each data transfer can be preceded by an optional preamble with programmable length and contents. The preamble is followed by read/write (RW) and address (RS) bits. The order of the these bits is programmable. The RW bit can be disabled. The following data can consist of one word or of a whole burst. The interface parameters are controlled by the DI_SER_DISP*n*_CONF registers (*n* = 1, 2).

Figure 64 depicts timing of the 5-wire serial interface (Type 1). For this interface, a separate RS line is added. When a burst is transmitted within a single active chip select interval, the RS can be changed at boundaries of words.

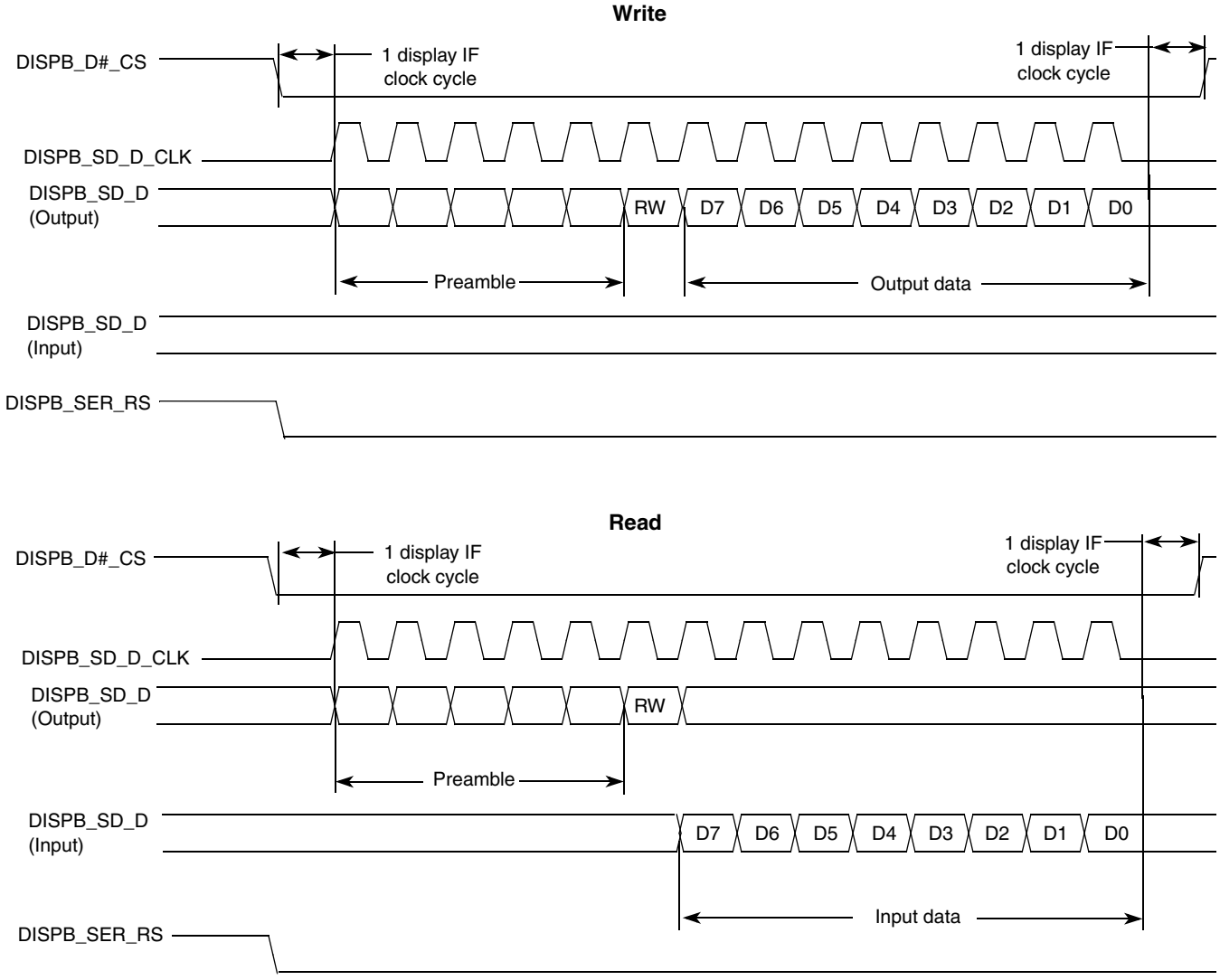


Figure 64. 5-Wire Serial Interface (Type 1) Timing Diagram

Figure 76 shows timing for PIO write, and Table 70 lists the timing parameters for PIO write.

Figure 76. PIO Write Timing Diagram

Table 70. PIO Write Timing Parameters

ATA Parameter	Parameter from Figure 76	Value	Controlling Variable
t1	t1	t1 (min.) = time_1 × T – (tskew1 + tskew2 + tskew5)	time_1
t2	t2w	t2 (min.) = time_2w × T – (tskew1 + tskew2 + tskew5)	time_2w
t9	t9	t9 (min.) = time_9 × T – (tskew1 + tskew2 + tskew6)	time_9
t3	—	t3 (min.) = (time_2w – time_on) × T – (tskew1 + tskew2 +tskew5)	If not met, increase time_2w
t4	t4	t4 (min.) = time_4 × T – tskew1	time_4
tA	tA	tA = (1.5 + time_ax) × T – (tco + tsui + tcable2 + tcable2 + 2*tbuf)	time_ax
t0	—	t0(min.) = (time_1 + time_2 + time_9) × T	time_1, time_2r, time_9
—	—	Avoid bus contention when switching buffer on by making ton long enough.	—
—	—	Avoid bus contention when switching buffer off by making toff long enough.	—

Figure 81. UDMA-In Device Terminates Transfer Timing Diagram

Table 72. UDMA-In Burst Timing Parameters

ATA Parameter	Parameters from Figure 79, Figure 80, Figure 81	Description	Controlling Variable
tack	tack	tack (min.) = (time_ack × T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv (min.) = (time_env × T) – (tskew1 + tskew2) tenv (max.) = (time_env × T) + (tskew1 + tskew2)	time_env
tds	tds1	tds – (tskew3) – ti_ds > 0	tskew3, ti_ds, ti_dh should be low enough
tdh	tdh1	tdh – (tskew3) – ti_dh > 0	
tcyc	tc1	(tcyc – tskew > T	T big enough
trp	trp	trp (min.) = time_rp × T – (tskew1 + tskew2 + tskew6)	time_rp
—	tx1[1]	(time_rp × T) – (tco + tsu + 3T + 2 × tbuf + 2 × tcable2) > trfs (drive)	time_rp
tmli	tmli1	tmli1 (min.) = (time_mlix + 0.4) × T	time_mlix
tzah	tzah	tzah (min.) = (time_zah + 0.4) × T	time_zah
tdzfs	tdzfs	tdzfs = (time_dzfs × T) – (tskew1 + tskew2)	time_dzfs
tcvh	tcvh	tcvh = (time_cvh × T) – (tskew1 + tskew2)	time_cvh
—	ton toff	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

1 There is a special timing requirement in the ATA host that requires the internal DIOW to go high three clocks after the last active edge on the DSTROBE signal. The equation given on this line tries to capture this constraint.

2. Make ton and toff large enough to avoid bus contention.

4.9.18 Parallel Interface (ULPI) Timing

Electrical and timing specifications of the parallel interface are presented in the subsequent sections.

Table 74. Signal Definitions—Parallel Interface

Name	Direction	Signal Description
USB_Clk	In	Interface clock. All interface signals are synchronous to the clock.
USB_Data[7:0]	I/O	Bidirectional data bus, driven low by the link during idle. Bus ownership is determined by Dir.
USB_Dir	In	Direction. Control the direction of the data bus.
USB_Stp	Out	Stop. The link asserts this signal for 1 clock cycle to stop the data stream currently on the bus.
USB_Nxt	In	Next. The PHY asserts this signal to throttle the data.

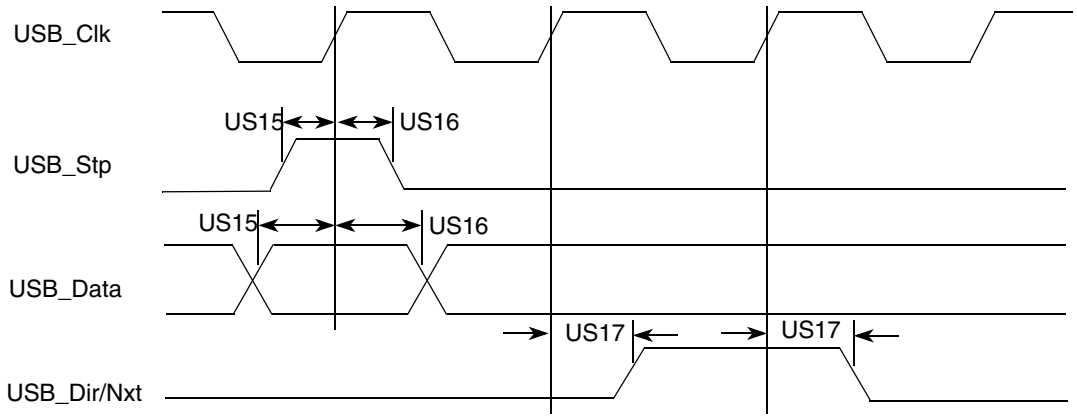


Figure 85. USB Transmit/Receive Waveform in Parallel Mode

Table 75. USB Timing Specification in VP_VM Unidirectional Mode

ID	Parameter	Min.	Max.	Unit	Conditions / Reference Signal
US15	USB_TXOE_B	—	6.0	ns	10 pF
US16	USB_DAT_VP	—	0.0	ns	10 pF
US17	USB_SE0_VM	—	9.0	ns	10 pF

4.9.19 PWM Electrical Specifications

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external

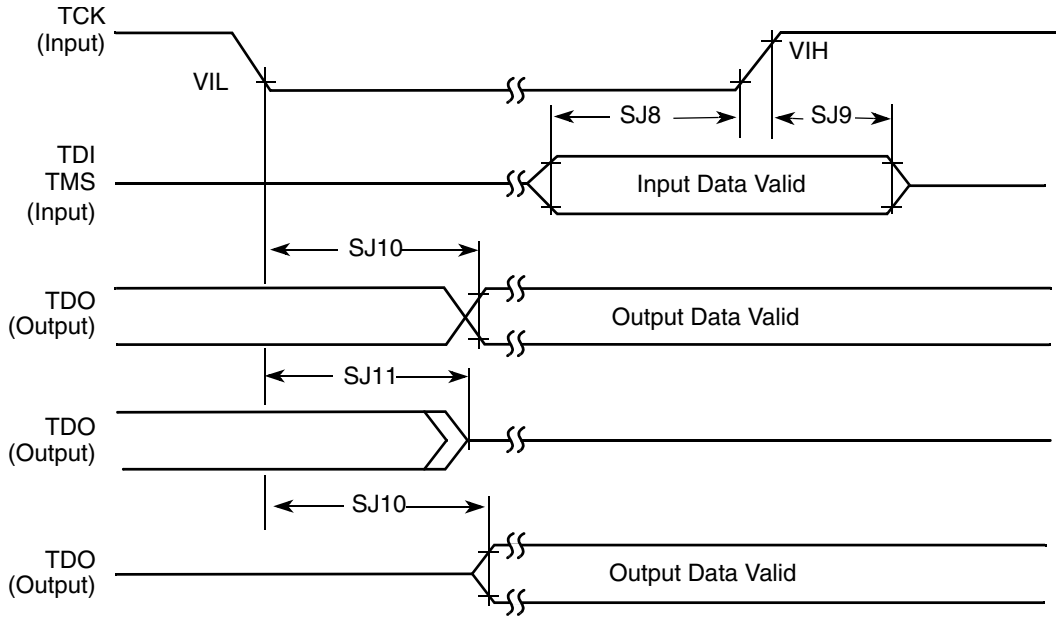


Figure 88. Test Access Port Timing Diagram

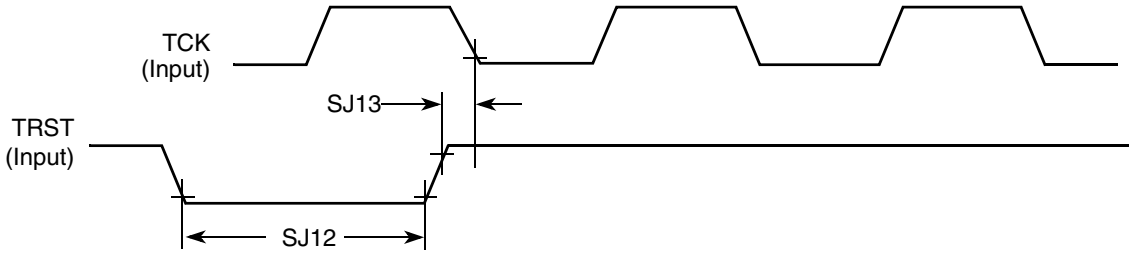


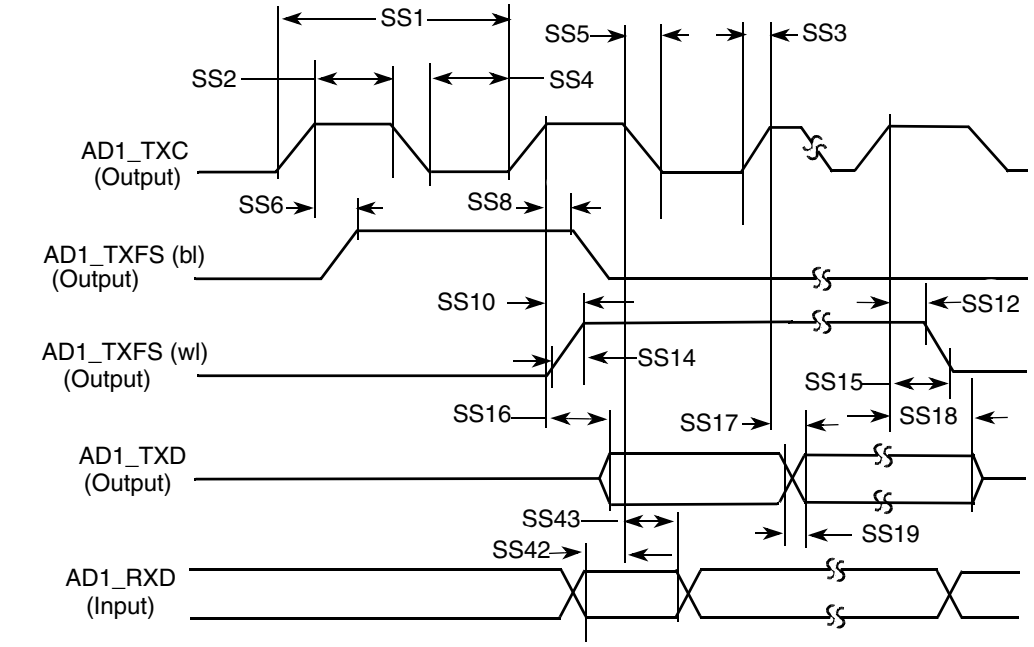
Figure 89. $\overline{\text{TRST}}$ Timing Diagram

Table 76. SJC Timing Parameters

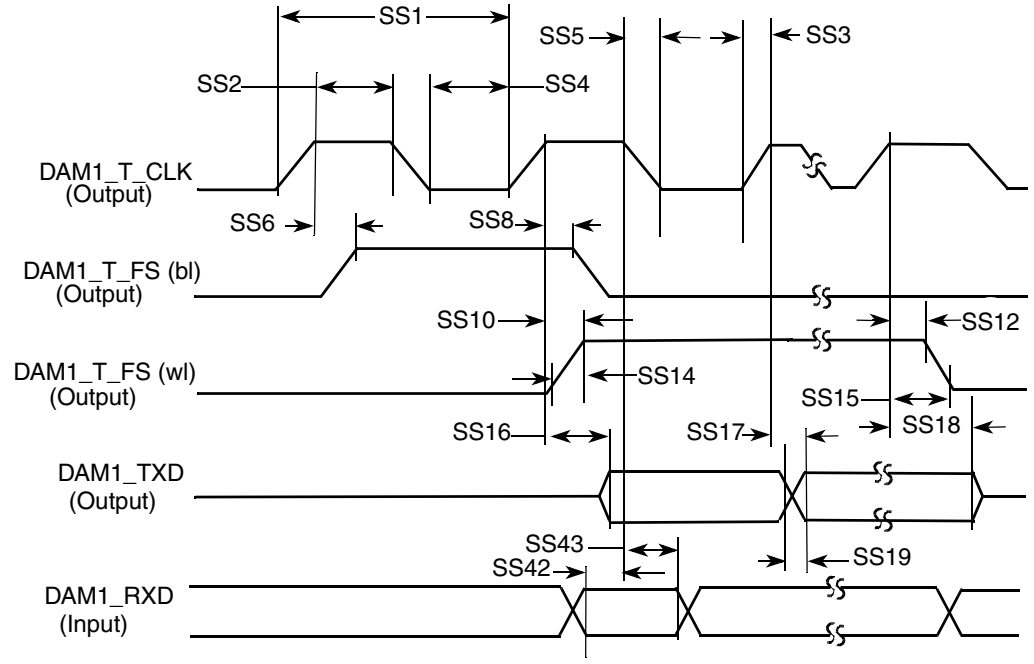
ID	Parameter	All Frequencies		Unit
		Min.	Max.	
SJ1	TCK cycle time	100[1]	—	ns
SJ2	TCK clock pulse width measured at V_M[2]	40	—	ns
SJ3	TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	10	—	ns
SJ5	Boundary scan input data hold time	50	—	ns
SJ6	TCK low to output data valid	—	50	ns
SJ7	TCK low to output high impedance	—	50	ns
SJ8	TMS, TDI data set-up time	10	—	ns
SJ9	TMS, TDI data hold time	50	—	ns
SJ10	TCK low to TDO data valid	—	44	ns

4.9.22.1 SSI Transmitter Timing with Internal Clock

Figure 92 depicts the SSI transmitter timing with internal clock, and Table 78 lists the timing parameters.



Note: SRXD Input in Synchronous mode only



Note: SRXD Input in Synchronous mode only

Figure 92. SSI Transmitter with Internal Clock Timing Diagram

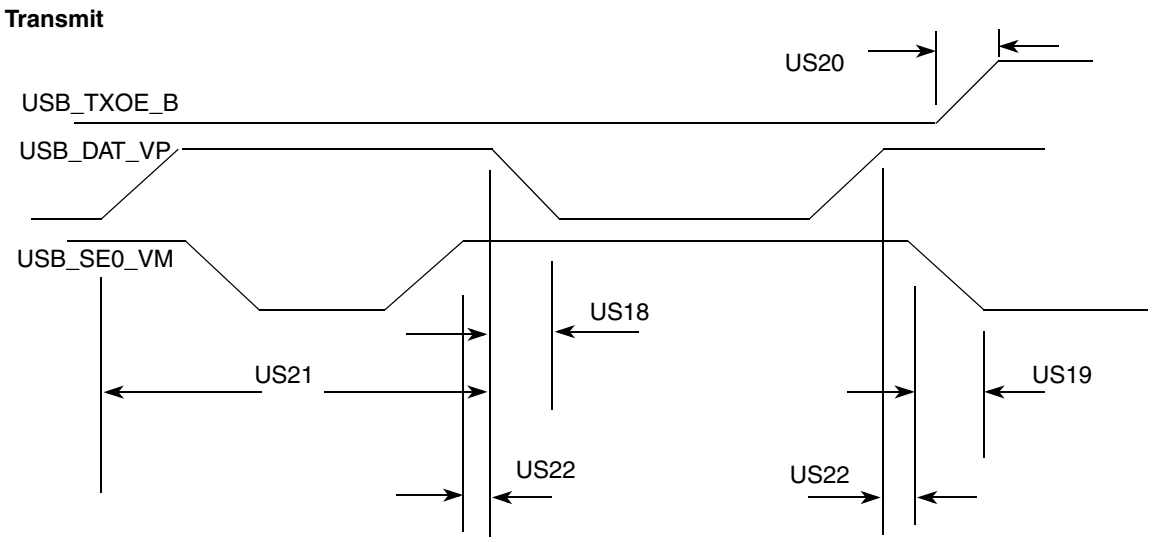


Figure 104. USB Transmit Waveform in VP_VM Bidirectional Mode

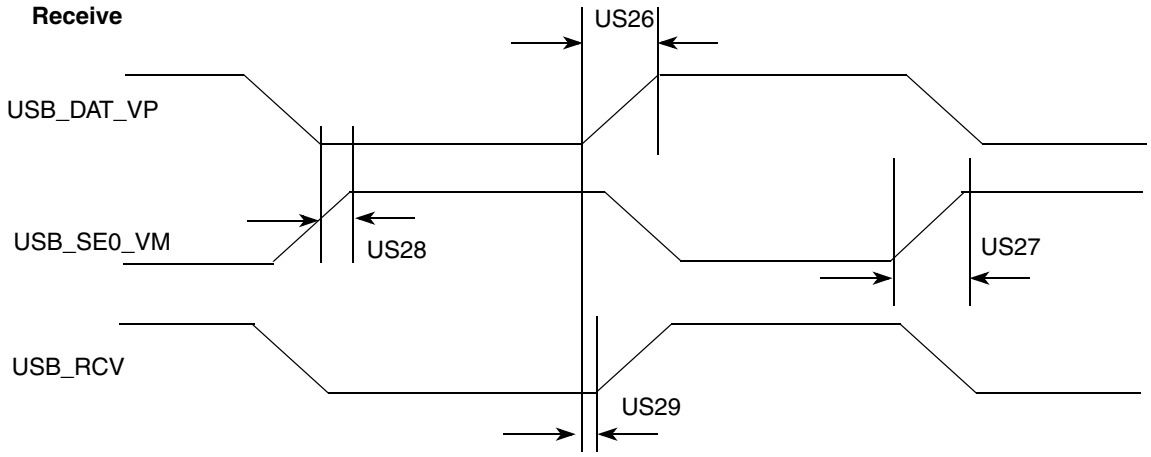


Figure 105. USB Receive Waveform in VP_VM Bidirectional Mode

Table 91 describes the port timing specification in VP_VM bidirectional mode.

Table 91. USB Port Timing Specification in VP_VM Bidirectional Mode

No.	Parameter	Signal Name	Direction	Min.	Max.	Unit	Condition/ Reference Signal
US18	Tx rise/fall time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US19	Tx rise/fall time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US20	Tx rise/fall time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US21	Tx duty cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US22	Tx overlap	USB_SE0_VM	Out	–3.0	+3.0	ns	USB_DAT_VP
US26	Rx rise/fall time	USB_DAT_VP	In	—	3.0	ns	35 pF
US27	Rx rise/fall time	USB_SE0_VM	In	—	3.0	ns	35 pF

Table 94. Silicon Revision 2.0 Signal Ball Map Locations (continued)

Signal ID	Ball Location
ATA_DATA13[1]	W2
ATA_DATA14[1]	W1
ATA_DATA15[1]	T4
ATA_DATA2[1]	V5
ATA_DATA3	U5
ATA_DATA4	Y4
ATA_DATA5	W4
ATA_DATA6	V4
CTS2	G5
D0	A2
D1	D4
D10	D2
D11	E6
D12	E3
D13	F5
D14	D1
D15	E2
D2	B2
D3	E5
D3_CLS[1]	L17
D3_DRDY[1]	L20
D3_FPSHIFT[1]	L15
D3_HSYNC[1]	L18
D3_REV[1]	M17
D3_SPL[1]	M18
D3_VSYNC[1]	M19
D4	C3
D5	B1
D6	D3
D7	C2
D8	C1
D9	E4
DE_B	W19
DQM0	B19
DQM1	D17
DQM2	D16
DQM3	C18
EB0	F18
EB1	F16
ECB	D19
EXT_ARMCLK	V8
EXTAL_AUDIO	W20
EXTAL24M	T20
FEC_COL	P3
FEC_CRS	N5
FEC_MDC	R1

Signal ID	Ball Location
CSI_VSYNC[1]	T14
CSPI1_MISO	V9
CSPI1_MOSI	W9
CSPI1_SCLK	W8
CSPI1_SPI_RDY	T8
CSPI1_SS0	Y8
CSPI1_SS1	U8
CTS1	R3
FEC_TDATA0	P5
FEC_TDATA1	M4
FEC_TDATA2	M5
FEC_TDATA3	L6
FEC_TX_CLK	P4
FEC_TX_EN	T1
FEC_TX_ERR	N4
FSR	K5
FST	J1
FUSE_VDD	P13
FUSE_VSS	M11
GPIO1_0	T11
GPIO1_1	Y11
GPIO2_0	U11
GPIO3_0	V11
HCKR	K2
HCKT	J5
I2C1_CLK	M20
I2C1_DAT	N17
I2C2_CLK	L3
I2C2_DAT	M1
LBA	D20
LD0[1]	F20
LD1[1]	G18
LD10[1]	H20
LD11[1]	J18
LD12[1]	J16
LD13[1]	J19
LD14[1]	J17
LD15[1]	J20
LD16[1]	K14
LD17[1]	K19
LD18[1]	K18
LD19[1]	K20
LD2[1]	G17
LD20[1]	K16
LD21[1]	K17
LD22[1]	K15

Table 95. Silicon Revision 2.1 Signal Ball Map Locations (continued)

Signal ID	Ball Location
VDD	L7
VDD	N7
VDD	R7
VDD	F8
VDD	R8
VDD	F9
VDD	F12
VDD	R12
VDD	G13
VDD	H15
VDD	J15
VSS	A1
VSS	Y1
VSS	J8
VSS	M8
VSS	N8
VSS	J9

Signal ID	Ball Location
VSS	L9
VSS	N9
VSS	K10
VSS	P10
VSS	H11
VSS	H12
NVCC_EMI2	H13
VSS	J13
VSS	K13
VSS	L13
VSS	T17
VSS	A20
VSS	Y20
VSTBY	T9
WDOG_RST	Y12
XTAL_AUDIO	V19
XTAL24M	U20

[1] Not available for the MCIMX351.

Table 96. Silicon Revision 2.0 Ball Map—17 x 17, 0.8 mm Pitch[1] (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
V	ATA_DA1	ATA_INTRQ	ATA_DATA10	ATA_DATA6	ATA_DATA2	ATA_DMACK	ATA_CS0	EXT_ARMCLK	CSPI1_MISO	CLKO	GPIO3_0	CAPTURE	SD2_DATA0	CSI_HSYNC	CSI_D13	CSI_D10	SD1_DATA3	SD1_CLK	XTAL_AUDIO	OSC_AUDIO_VDD	V
W	ATA_DATA14	ATA_DATA13	ATA_DATA9	ATA_DATA5	ATA_DATA1	ATA_DIOW	USBOTG_PWR	CSPI1_SCLK	CSPI1_MOSI	BOOT_MODE0	POR_B	MLB_SIG	MLB_CLK	SD2_CLK	CSI_MCLK	CSI_D12	CSI_D9	SD1_DATA2	DE_B	EXTAL_AUDIO	W
Y	VSS	ATA_DATA11	ATA_DATA7	ATA_DATA4	ATA_DATA0	ATA_DIOR	TEST_MODE	CSPI1_SS0	POWER_FAIL	CLK_MODE0	GPIO1_1	WDOG_RST	MLB_DAT	SD2_DATA2	CSI_PIXCLK	CSI_D15	USBPHY2_DM	USBPHY2_DP	SD1_CMD	VSS	Y

[1] See Table 95 for pins unavailable in the MCIMX351 SoC.

Table 97. Silicon Revision 2.1 Ball Map—17 x 17, 0.8 mm Pitch

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	GND	D0	A9	A7	A0	SDBA0	SD30	SD27	SD24	SD23	SD21	SD18	SD15	SD14	SD10	SD9	SD6	SD4	SD1	GND	A
B	D5	D2	A13	A8	A5	SDBA1	SD31	SD28	SD26	SD22	SD20	SD19	SD12	SD13	SD11	SD7	SD0	SD2	DQM0	CS2	B
C	D8	D7	D4	MA10	A6	A3	A23	SD29	SD25	A20	SD17	SD16	A17	SD8	SD5	SD3	DQM1	DQM3	CS3	RW	C
D	D14	D10	D6	D1	A11	A4	A1	A24	A22	A21	A19	A18	A16	A14	A15	DQM2	SDCKE1	SDCKE0	ECB	LBA	D
E	NFCLE	D15	D12	D9	D3	D11	A2	A25	SDQS3	SDQS2	SDQS1	SDCLK	SDCLK_B	SDQS0	BCLK	RAS	CAS	CS4	CS1	OE	E
F	NFRE_B	NFALE	NFRB	NFWP_B	D13	A12	VDD7	VDD7	VDD7	GND	NVCC_EMI1	VDD7	NVCC_EMI2	GND	A10	EB1	CS0	EB0	CS5	LD0	F
G	RTS2	NFWE_B	NF_CE0	TX0	CTS2	NVCC_NFC	NVCC_EMI1	NVCC_EMI1	NVCC_EMI1	NVCC_EMI1	NVCC_EMI1	NVCC_EMI2	VDD6	NVCC_EMI3	SDWE	LD3	LD2	LD1	LD4	LD7	G
H	TX1	TXD2	RXD2	TX4_RX1	TX2_RX3	NVCC_NFC	NVCC_NFC	GND	NVCC_EMI1	NVCC_EMI1	GND	GND	NVCC_EMI2	NVCC_LCDC	VDD5	LD5	LD8	LD6	LD9	LD10	H
J	FST	TX3_RX2	TX5_RX0	SCKT	HCKT	STXFS5	VDD1	GND	GND	GND	GND	GND	GND	NVCC_LCDC	VDD5	LD12	LD14	LD11	LD13	LD15	J
K	STXD5	HCKR	SCKR	SRXD5	FSR	NVCC_MISC	NVCC_MISC	GND	GND	GND	GND	GND	GND	LD16	LD22	LD20	LD21	LD18	LD17	LD19	K
L	SRXD4	STXFS4	I2C2_CLK	SCK4	SCK5	FEC_TDATA3	VDD2	NVCC_MISC	GND	GND	GND	GND	GND	NVCC_LCDC	D3_FPSHIFT	CONTRAST	D3_CLS	D3_HSYNC	LD23	D3_DRDY	L
M	I2C2_DAT	STXD4	FEC_RDATA2	FEC_TDATA1	FEC_TDATA2	VDD2	GND	GND	GND	GND	FUSE_VSS	PGND	GND	NVCC_LCDC	PHY1_VDDA	TTM_PAD	D3_REV	D3_SPL	D3_VSYNC	I2C1_CLK	M
N	FEC_RDATA3	FEC_RDATA1	FEC_RX_ERR	FEC_TX_ERR	FEC_CRS	NVCC_ATA	VDD3	GND	GND	GND	MGND	GND	PVDD	USBPHY1_UPLLGND	USBPHY1_UPLLVDD	PHY1_VSSA	I2C1_DAT	USBPHY1_UID	USBPHY1_DM	PHY1_VDDA	N