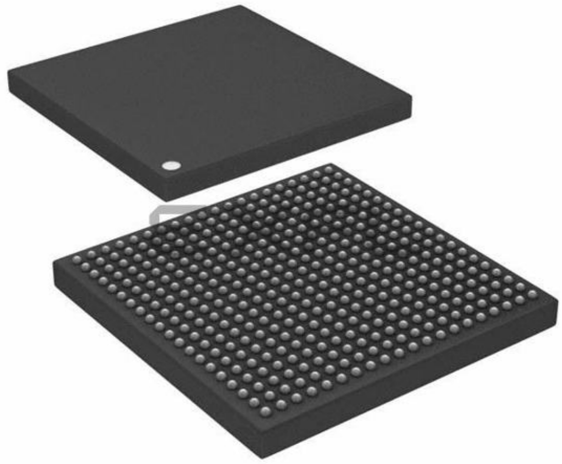

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	532MHz
Co-Processors/DSP	Multimedia; GPU, IPU, VFP
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, KPP, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Secure Fusebox, Secure JTAG
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx356ajq5cr2

- Flash controller—MLC/SLC NAND and NOR
- GPIO with interrupt capabilities
- 3 I^2C modules (up to 400 Kbytes each)
- JTAG
- Key pin port
- Media local bus (MLB) interface
- Asynchronous sample rate converter (ASRC)
- 1-Wire
- Parallel camera sensor (4/8/10/16-bit data port for video color models: YCC, YUV, 30 Mpixels/s)
- Parallel display (primary up to 24-bit, 1024 x 1024)
- Parallel ATA (up to 66 Mbytes) (not available for the MCIMX351)
- PWM
- SPDIF transceiver
- 3 UART (up to 4.0 Mbps each)

1.2 Ordering Information

Table 1 provides the ordering information for the i.MX35 processors for automotive applications.

Table 1. Ordering Information

Description	Part Number	Silicon Revision	Package[1]	Speed	Operating Temperature Range (°C)	Signal Ball Map Locations	Ball Map
i.MX351	MCIMX351AVM4B	2.0	5284	400 MHz	–40 to 85	Table 94	Table 96
i.MX351	MCIMX351AVM5B	2.0	5284	532 MHz[2]	–40 to 85	Table 94	Table 96
i.MX355	MCIMX355AVM4B	2.0	5284	400 MHz	–40 to 85	Table 94	Table 96
i.MX355	MCIMX355AVM5B	2.0	5284	532 MHz[2]	–40 to 85	Table 94	Table 96
i.MX356	MCIMX356AVM4B	2.0	5284	400 MHz	–40 to 85	Table 94	Table 96
i.MX356	MCIMX356AVM5B	2.0	5284	532 MHz[2]	–40 to 85	Table 94	Table 96
i.MX351	MCIMX351AJQ4C	2.1	5284	400MHz	-40 to 85	Table 95	Table 97
i.MX351	MCIMX351AJQ5C	2.1	5284	532MHz[2]	-40 to 85	Table 95	Table 97
i.MX355	MCIMX355AJQ4C	2.1	5284	400MHz	-40 to 85	Table 95	Table 97
i.MX355	MCIMX355AJQ5C	2.1	5284	532MHz[2]	-40 to 85	Table 95	Table 97
i.MX356	MCIMX356AJQ4C	2.1	5284	400MHz	-40 to 85	Table 95	Table 97
i.MX356	MCIMX356AJQ5C	2.1	5284	532MHz[2]	-40 to 85	Table 95	Table 97
i.MX356	SCIMX356BVMB	2	5284	532MHz	-40 to 85	Table 94	Table 96

[1] Case 5284 is RoHS-compliant, lead-free, MSL = 3, 1.

[2] 532 MHz rated devices meet all specifications of 400 MHz rated devices. A 532 MHz device can be substituted in place of a 400 MHz device.

Table 4. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Domain[1]	Subsystem	Brief Description
ESAI	Enhanced serial audio interface	SDMA	Connectivity peripherals	The enhanced serial audio interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other DSPs. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator.
eSDHCv2 (3)	Enhanced secure digital host controller	ARM	Connectivity peripherals	The eSDHCv2 consists of four main modules: CE-ATA, MMC, SD and SDIO. CE-ATA is a hard drive interface that is optimized for embedded applications of storage. The MultiMediaCard (MMC) is a universal, low-cost, data storage and communication media to applications such as electronic toys, organizers, PDAs, and smart phones. The secure digital (SD) card is an evolution of MMC and is specifically designed to meet the security, capacity, performance, and environment requirements inherent in emerging audio and video consumer electronic devices. SD cards are categorized into Memory and I/O. A memory card enables a copyright protection mechanism that complies with the SDMI security standard. SDIO cards provide high-speed data I/O (such as wireless LAN via SDIO interface) with low power consumption. **Note:** CE-ATA is not available for the MCIMX351.
FEC	Ethernet	SDMA	Connectivity peripherals	The Ethernet media access controller (MAC) is designed to support both 10 and 100 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media
GPIO(3)	General purpose I/O modules	ARM	Pins	Used for general purpose input/output to external ICs. Each GPIO module supports 32 bits of I/O.
GPT	General purpose timers	ARM	Timer peripherals	Each GPT is a 32-bit free-running or set-and-forget mode timer with a programmable prescaler and compare and capture registers. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in set-and-forget mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU2D	Graphics processing unit 2Dv1	ARM	Multimedia peripherals	This module accelerates OpenVG and GDI graphics. **Note:** Not available for the MCIMX351.

4.1.1 i.MX35 Operating Ranges

Table 8 provides the recommended operating ranges. The term NVCC in this section refers to the associated supply rail of an input or output.

Table 8. i.MX35 Operating Ranges

Parameter	Symbol	Min.	Typical	Max.	Units
Core Operating Voltage $0 < f_{ARM} < 400$ MHz	V_{DD}	1.22	—	1.47	V
Core Operating Voltage $0 < f_{ARM} < 532$ MHz		1.33	—	1.47	V
State Retention Voltage		1	—	—	V
EMI[1]	NVCC_EMI1,2,3	1.7	—	3.6	V
WTDG, Timer, CCM, CSPI1	NVCC_CRM	1.75	—	3.6	V
NANDF	NVCC_NANDF	1.75	—	3.6	V
ATA, USB generic	NVCC_ATA	1.75	—	3.6	V
eSDHC1	NVCC_SDIO	1.75	—	3.6	V
CSI, SDIO2	NVCC_CSI	1.75	—	3.6	V
JTAG	NVCC_JTAG	1.75	—	3.6	V
LCDC, TTM, I2C1	NVCC_LCDC	1.75	—	3.6	V
I2Sx2,ESAI, I2C2, UART2, UART1, FEC	NVCC_MISC	1.75	—	3.6	V
MLB	NVCC_MLB[2]	1.75	—	3.6	V
USB OTG PHY	PHY1_VDDA	3.17	3.3	3.43	V
USB OTG PHY	USBPHY1_VDDA_BIAS	3.17	3.3	3.43	V
USB OTG PHY	USBPHY1_UPLLVDD	3.17	3.3	3.43	V
USB HOST PHY	PHY2_VDD	3.0	3.3	3.6	V
OSC24M	OSC24M_VDD	3.0	3.3	3.6	V
OSC_AUDIO	OSC_AUDIO_VDD	3.0	3.3	3.6	V
MPLL	MVDD	1.4	—	1.65	V
PPLL	PVDD	1.4	—	1.65	V
Fusebox program supply voltage	FUSE_VDD[3]	3.0	3.6	3.6	V
Operating ambient temperature range	T_A	–40	—	85	^{o}C
Junction temperature range	T_J	–40	—	105	^{o}C

[1] EMI I/O interface power supply should be set up according to external memory. For example, if using SDRAM then NVCC_EMI1,2,3 should all be set at 3.3 V (typ.). If using MDDR or DDR2, NVC_EMI1,2,3 must be set at 1.8 V (typ.).

[2] MLB interface I/O pads can be programmed to function as GPIO by setting NVCC_MLB to 1.8 or 3.3 V, but if used as MLB pads, NVCC_MLB must be set to 2.5 V in order to be compliant with external MOST devices. NVCC_MLB may be left floating.

[3] The Fusebox read supply is connected to supply of the full speed USB PHY. FUSE_VDD is only used for programming. It is recommended that FUSE_VDD be connected to ground when not being used for programming. FUSE_VDD should be supplied by following the power up sequence given in Section 4.3.1, “Powering Up.”

Assuming the i.MX35 chip is already fully powered; it is still possible to reset all of the modules to their default reset by asserting POR_B for at least 4 CKIL cycles and later de-asserting POR_B. This method of resetting the i.MX35 can also be supported by tying the POR_B and RESET_IN_B pins together.

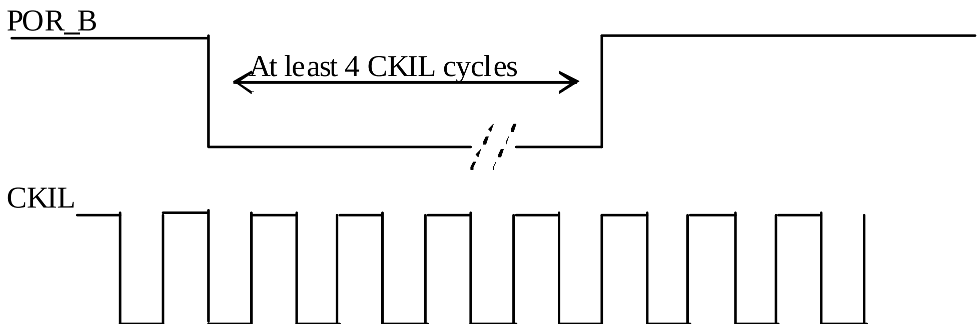


Figure 3. Timing Between POR_B and CKIL for Complete Reset of i.MX35

4.4.2 System Reset

System reset can be achieved by asserting RESET_IN_B for at least 4 CKIL cycles and later negating RESET_IN_B. The following modules are not reset upon system reset: RTC, PLLs, CCM, and IIM. POR_B pin must be deasserted all the time.

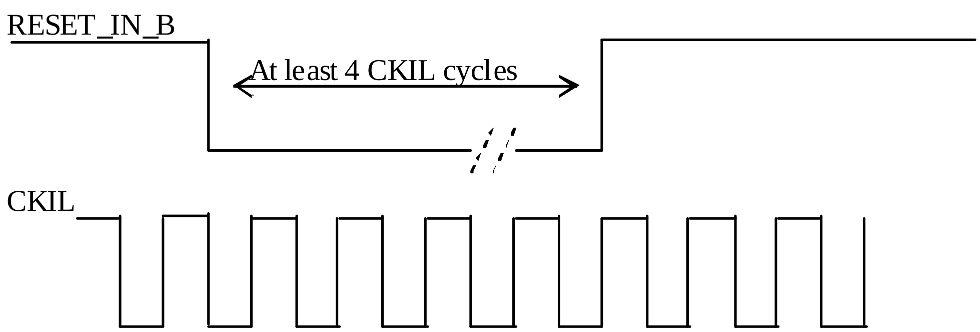


Figure 4. Timing Between RESET_IN_B and CKIL for i.MX35 System Reboot

4.5 Power Characteristics

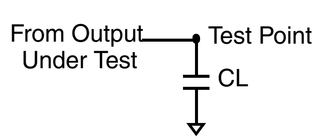
The table shows values representing maximum current numbers for the i.MX35 under worst case voltage and temperature conditions. These values are derived from the i.MX35 with core clock speeds up to 532 MHz. Common supplies have been bundled according to the i.MX35 power-up sequence requirements. Peak numbers are provided for system designers so that the i.MX35 power supply requirements will be satisfied during startup and transient conditions. Freescale recommends that system current measurements be taken with customer-specific use-cases to reflect normal operating conditions in the end system.

Table 14. I/O Pin DC Electrical Characteristics (continued)

Pin	DC Electrical Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
SDR (1.8 V)	High-level output voltage	Voh	Ioh = 5.7 mA	OVDD – 0.28	—	—	V
	Low-level output voltage	Vol	Ioh = 5.7 mA	—	—	0.4	V
	High-level output current	Ioh	Max. drive	5.7	—	—	mA
	Low-level output current	Iol	Max. drive	7.3	—	—	mA
	High-level DC Input Voltage	VIH	—	1.4	—	1.98	V
	Low-level DC Input Voltage	VIL	—	–0.3	—	0.8	V
	Input current (no pull-up/down)	IIN	VI = 0 VI=NVCC	—	—	150 80	μA
	Tri-state I/O supply current	Icc (NVCC)	VI = OVDD or 0	—	—	1180	μA
	Tri-state core supply current	Icc (NVCC)	VI = VDD or 0	—	—	1220	μA
SDR (3.3 V)	High-level output voltage	Voh	Ioh=specified drive (Ioh = –4, –8, –12, –16 mA)	2.4	—	—	V
	Low-level output voltage	Vol	Ioh=specified drive (Ioh = 4, 8, 12, 16 mA)	—	—	0.4	V
	High-level output current	Ioh	Standard drive High drive Max. drive	–4.0 –8.0 –12.0	—	—	mA
	Low-level output current	Iol	Standard drive High drive Max. drive	4.0 8.0 12.0	—	—	mA
	High-level DC Input Voltage	VIH	—	2.0	—	3.6	V
	Low-level DC Input Voltage	VIL	—	–0.3V	—	0.8	V
	Input current (no pull-up/down)	IIN	VI = 0 VI = NVCC	—	—	±1	μA
	Tri-state I/O supply current	Icc (NVCC)	VI = NVCC or 0	—	—	±1	μA

4.8 I/O Pin AC Electrical Characteristics

Figure 5 shows the load circuit for output pins.



CL includes package, probe and jig capacitance

Figure 5. Load Circuit for Output Pin

Table 33. WEIM Bus Timing Parameters[1]

ID	Parameter	Min.	Max.	Unit
WE1	BCLK cycle time[2]	14.5	—	ns
WE2	BCLK low-level width[2]	7	—	ns
WE3	BCLK high-level width[2]	7	—	ns
WE4	Address valid to Clock rise/fall	15	21	ns
WE5	Clock rise/fall to address invalid	22	25	ns
WE6	Clock rise/fall to CSx_B valid	15	19	ns
WE7	Clock rise/fall to CSx_B invalid	3.6	5	ns
WE8	Clock rise/fall to RW_B valid	8	12	ns
WE9	Clock rise/fall to RW_B invalid	3	8	ns
WE10	Clock rise/fall to OE_B valid	7	12	ns
WE11	Clock rise/fall to OE_B invalid	3.8	5.5	ns
WE12	Clock rise/fall to EBy_B valid	6	11.5	ns
WE13	Clock rise/fall to EBy_B invalid	6	10	ns
WE14	Clock rise/fall to LBA_B valid	17.5	20	ns
WE15	Clock rise/fall to LBA_B invalid	0	1	ns
WE16	Clock rise/fall to Output Data valid	5	10	ns
WE17	Clock rise to Output Data invalid	0	2.5	ns
WE18	Input Data Valid to Clock rise[3]	1	—	ns
WE19	Input Data Valid to Clock rise, FCE=0 (in the case there is ECB_B asserted during access)	(BCLK/2) + 3.01	—	ns
WE19	Input Data Valid to Clock rise, FCE=0 (in the case there is NO ECB_B asserted during access)	6.9	—	ns
WE20	Clock rise to Input Data invalid[3]	1	—	ns
WE22	ECB_B setup time[3]	5	—	ns
WE24	ECB_B hold time[3]	0	—	ns
WE26	DTACK_B setup time	5.4	—	ns
WE27	DTACK_B hold time	–3.2	—	ns

[1] “High” is defined as 80% of signal value, and “low” is defined as 20% of signal value.

[2] BCLK parameters are measured from the 50% point. For example, “high” is defined as 50% of signal value and “low” is defined as 50% of signal value.

[3] Parameters W18, W20, W22, and W24 are tested when FCE=1. i.MX35 does not support FCE=0.

NOTE

Test conditions: load capacitance, 25 pF. Recommended drive strength for all controls, address, and BCLK is set to maximum drive.

Table 43. DDR2 SDRAM Read Cycle Parameter Table

ID	PARAMETER	Symbol	DDR2-400		Unit
			Min	Max	
DDR24	DQS – DQ Skew (defines the Data valid window in read cycles related to DQS).	tDQSQ	—	0.35	ns
DDR25	DQS DQ in HOLD time from DQS[1]	tQH	2.925	—	ns
DDR26	DQS output access time from SDCLK posedge	tDQSCK	–0.5	0.5	ns

[1]The value was calculated for an SDCLK frequency of 133 MHz by the formula tQH = tHP – tQHS = min (tCL,tCH) – tQHS = 0.45 × tCK – tQHS = 0.45 × 7.5 – 0.45 = 2.925 ns.

NOTE

SDRAM CLK and DQS-related parameters are measured from the 50% point—that is, "high" is defined as 50% of signal value and "low" is defined as 50% of signal value. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and $\overline{\text{SDCLK}}$ (inverted clock).

Test conditions are: Capacitance 15 pF for DDR PADS. Recommended drive strength is Medium for SDCLK and High for Address and controls.

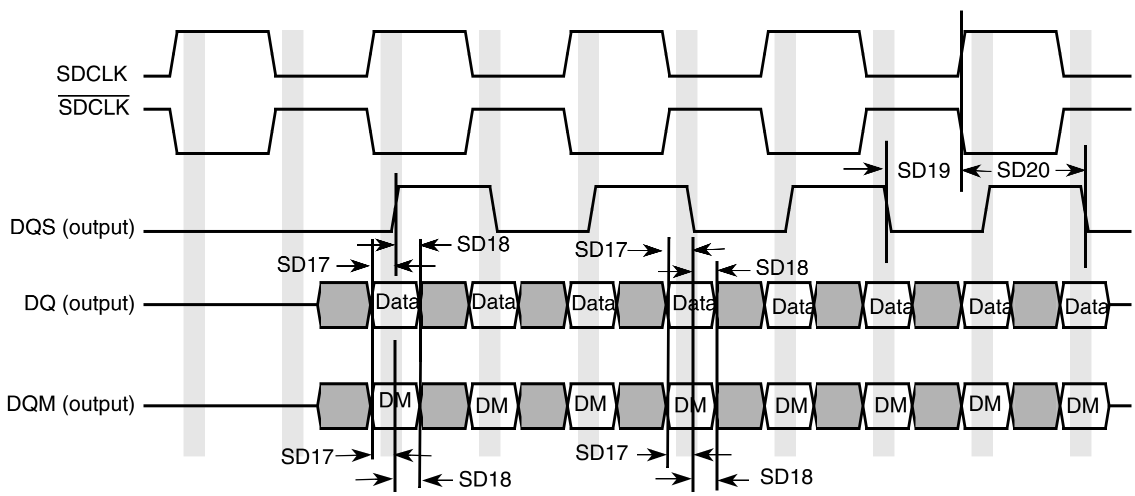


Figure 34. Mobile DDR SDRAM Write Cycle Timing Diagram

Table 44. Mobile DDR SDRAM Write Cycle Timing Parameters[1]

ID	Parameter	Symbol	Min.	Max.	Unit
SD17	DQ and DQM setup time to DQS	tDS	0.95	—	ns
SD18	DQ and DQM hold time to DQS	tDH	0.95	—	ns
SD19	Write cycle DQS falling edge to SDCLK output delay time.	tDSS	1.8	—	ns
SD20	Write cycle DQS falling edge to SDCLK output hold time.	tDSH	1.8	—	ns

[1] Test condition: Measured using delay line 5 programmed as follows: ESDCDLY5[15:0] = 0x0703.

NOTE

SDRAM CLK and DQS-related parameters are measured from the 50% point—that is, "high" is defined as 50% of signal value and "low" is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets. Table 44 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK, and the parameters are measured at maximum memory frequency.

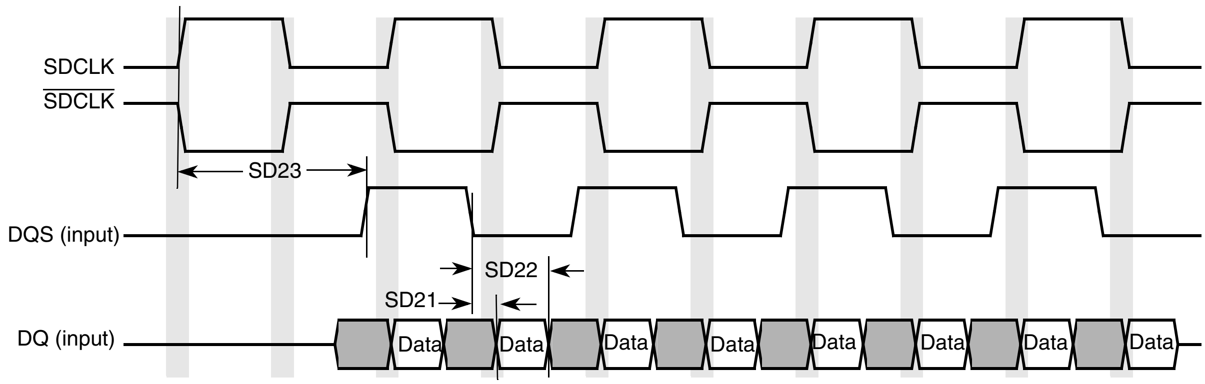


Figure 35. Mobile DDR SDRAM DQ versus DQS and SDCLK Read Cycle Timing Diagram

Table 45. Mobile DDR SDRAM Read Cycle Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD21	DQS – DQ Skew (defines the Data valid window in read cycles related to DQS).	tDQSQ	—	0.85	ns
SD22	DQS DQ HOLD time from DQS	tQH	2.3	—	ns
SD23	DQS output access time from SDCLK posedge	tDQSCK	—	6.7	ns

NOTE

SDRAM CLK and DQS-related parameters are measured from the 50% point—that is, "high" is defined as 50% of signal value, and "low" is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets. Table 45 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK, and the parameters are measured at maximum memory frequency.

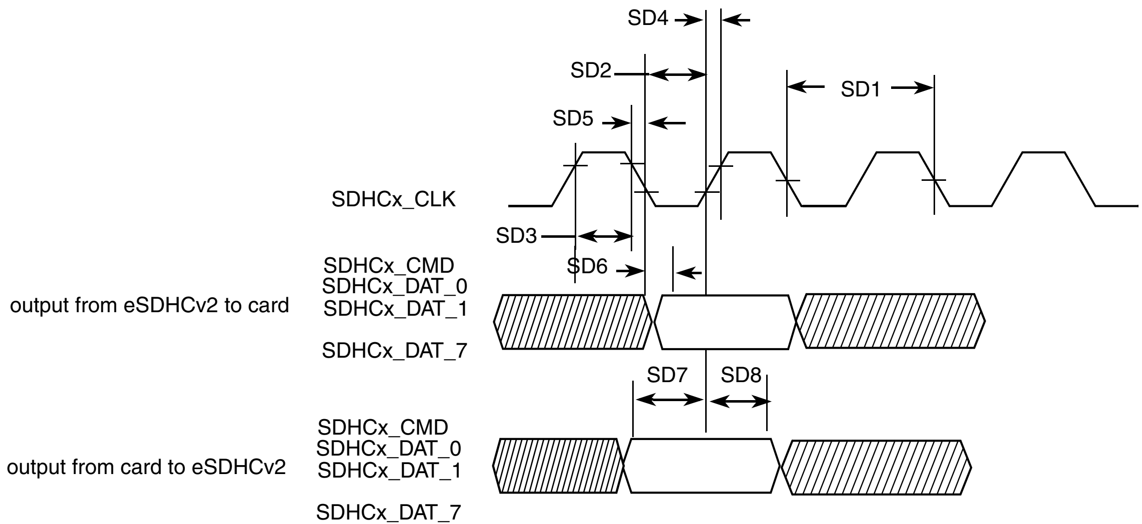


Figure 38. eSDHCv2 Timing

Table 47. eSDHCv2 Interface Timing Specification

ID	Parameter	Symbols	Min.	Max.	Unit
Card Input Clock					
SD1	Clock frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low time	t_{WL}	7	—	ns
SD3	Clock high time	t_{WH}	7	—	ns
SD4	Clock rise time	t_{TLH}	—	3	ns
SD5	Clock fall time	t_{THL}	—	3	ns
eSDHC Output/Card Inputs CMD, DAT (Reference to CLK)					
SD6	eSDHC output delay	t_{OD}	–3	3	ns
eSDHC Input/Card Outputs CMD, DAT (Reference to CLK)					
SD7	eSDHC input setup time	t_{ISU}	5	—	ns
SD8	eSDHC input hold time	t_{IH}[4]	2.5	—	ns

[1] In low-speed mode, the card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

[2] In normal-speed mode for the SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.

[3] In normal-speed mode for MMC card, clock frequency can be any value between 0 and 20 MHz. In high-speed mode, clock frequency can be any value between 0–52 MHz.

[4] To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.9.11 I^2C AC Electrical Specifications

This section describes the electrical characteristics of the I^2C module.

4.9.11.1 I^2C Module Timing

Figure 43 depicts the timing of the I^2C module. Table 52 lists the I^2C module timing parameters.

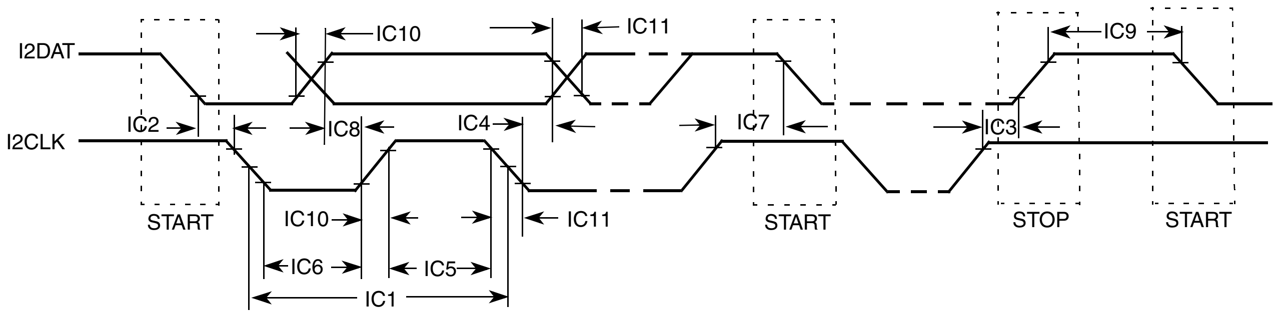


Figure 43. I^2C Bus Timing Diagram

Table 52. I^2C Module Timing Parameters

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
IC1	I2CLK cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2CLK Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2CLK Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2DAT and I2CLK signals	—	1000	—	300	ns
IC11	Fall time of both I2DAT and I2CLK signals	—	300	—	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

[1] A device must internally provide a hold time of at least 300 ns for the I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

[2] The maximum hold time has to be met only if the device does not stretch the LOW period (ID IC6) of the I2CLK signal.

[3] A fast-mode I^2C-bus device can be used in a standard-mode I^2C-bus system, but the requirement of set-up time (ID IC7) of 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the I2CLK signal. If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line max_rise_time (ID No IC10) + data_setup_time (ID No IC8) = 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-bus specification) before the I2CLK line is released.

Figure 64 depicts timing of the 5-wire serial interface (Type 1). For this interface, a separate RS line is added. When a burst is transmitted within a single active chip select interval, the RS can be changed at boundaries of words.

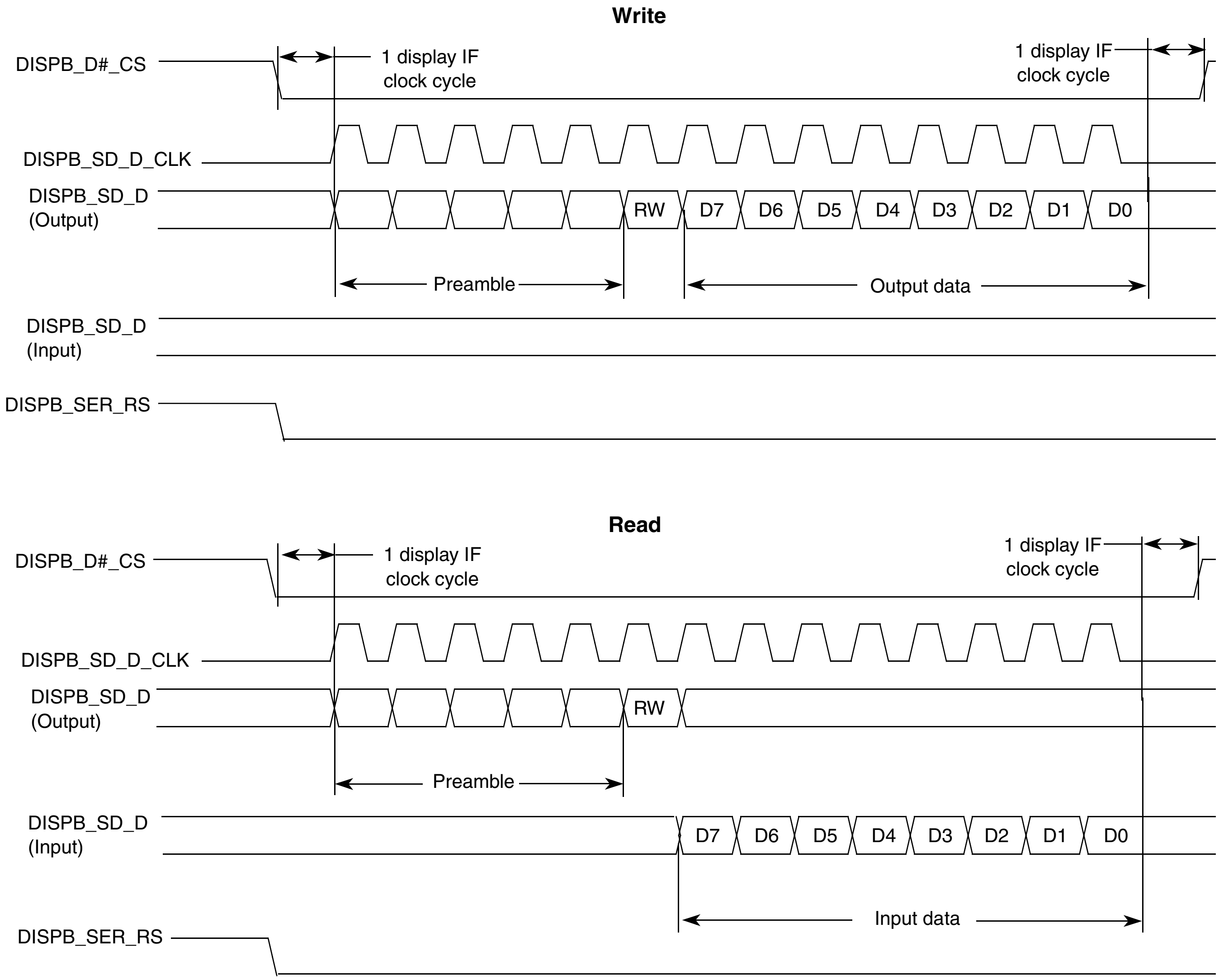


Figure 64. 5-Wire Serial Interface (Type 1) Timing Diagram

Figure 71 depicts write 0 sequence timing, and Table 65 lists the timing parameters.

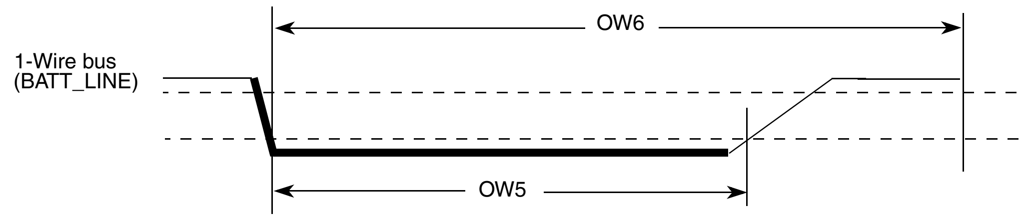


Figure 71. Write 0 Sequence Timing Diagram

Table 65. WR0 Sequence Timing Parameters

ID	Parameter	Symbol	Min.	Typ.	Max.	Units
OW5	Write 0 low time	t_{WR0_low}	60	100	120	µs
OW6	Transmission time slot	t_{SLOT}	OW5	117	120	µs

Figure 72 shows write 1 sequence timing, and Figure 73 depicts the read sequence timing. Table 66 lists the timing parameters.

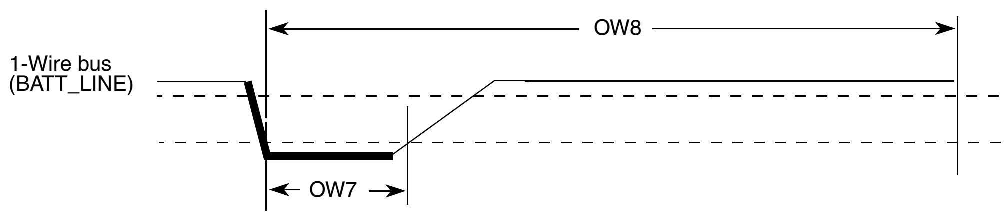


Figure 72. Write 1 Sequence Timing Diagram

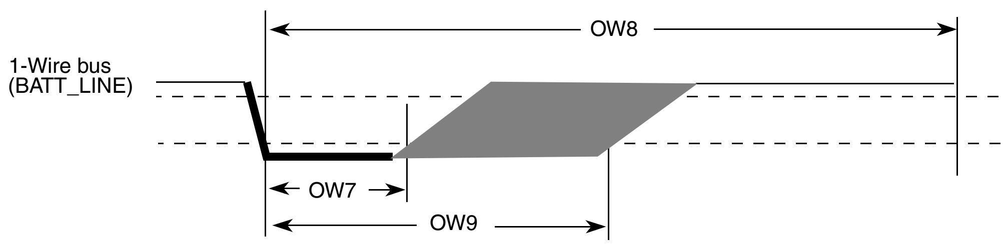


Figure 73. Read Sequence Timing Diagram

Table 66. WR1/RD Timing Parameters

ID	Parameter	Symbol	Min.	Typ.	Max.	Units
OW7	Write 1/read low time	t_{LOW1}	1	5	15	µs
OW8	Transmission time slot	t_{SLOT}	60	117	120	µs
OW9	Release time	$t_{RELEASE}$	15	—	45	µs

Table 71. MDMA Read and Write Timing Parameters (continued)

ATA Parameter	Parameter from Figure 77, Figure 78	Value	Controlling Variable
tn, tj	tkjn	tn = tj = tkjn = (max.(time_k,. time_jn) × T – (tskew1 + tskew2 + tskew6)	time_jn
—	ton toff	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

4.9.17.5 UDMA-In Timing

Figure 79 shows timing when the UDMA-in transfer starts, Figure 80 shows timing when the UDMA-in host terminates transfer, Figure 81 shows timing when the UDMA-in device terminates transfer, and Table 72 lists the timing parameters for the UDMA-in burst.

Figure 79. UDMA-In Transfer Starts Timing Diagram

Figure 80. UDMA-In Host Terminates Transfer Timing Diagram

Figure 84. UDMA-Out Device Terminates Transfer Timing Diagram

Table 73. UDMA-Out Burst Timing Parameters

ATA Parameter	Parameter from Figure 82, Figure 83, Figure 84	Value	Controlling Variable
tack	tack	tack (min.) = (time_ack × T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv (min.) = (time_env × T) – (tskew1 + tskew2) tenv (max.) = (time_env × T) + (tskew1 + tskew2)	time_env
tdvs	tdvs	tdvs = (time_dvs ×T) – (tskew1 + tskew2)	time_dvs
tdvh	tdvh	tdvs = (time_dvh × T) – (tskew1 + tskew2)	time_dvh
tcyc	tcyc	tcyc = time_cyc × T – (tskew1 + tskew2)	time_cyc
t2cyc	—	t2cyc = time_cyc × 2 × T	time_cyc
trfs1	trfs	trfs = 1.6 × T + tsui + tco + tbuf + tbuf	—
—	tdzfs	tdzfs = time_dzfs × T – (tskew1)	time_dzfs
tss	tss	tss = time_ss × T – (tskew1 + tskew2)	time_ss
tmli	tdzfs_mli	tdzfs_mli = max. (time_dzfs, time_mli) × T – (tskew1 + tskew2)	—
tli	tli1	tli1 > 0	—
tli	tli2	tli2 > 0	—
tli	tli3	tli3 > 0	—
tcvh	tcvh	tcvh = (time_cvh × T) – (tskew1 + tskew2)	time_cvh
—	ton toff	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

4.9.18 Parallel Interface (ULPI) Timing

Electrical and timing specifications of the parallel interface are presented in the subsequent sections.

Table 74. Signal Definitions—Parallel Interface

Name	Direction	Signal Description
USB_Clk	In	Interface clock. All interface signals are synchronous to the clock.
USB_Data[7:0]	I/O	Bidirectional data bus, driven low by the link during idle. Bus ownership is determined by Dir.
USB_Dir	In	Direction. Control the direction of the data bus.
USB_Stp	Out	Stop. The link asserts this signal for 1 clock cycle to stop the data stream currently on the bus.
USB_Nxt	In	Next. The PHY asserts this signal to throttle the data.

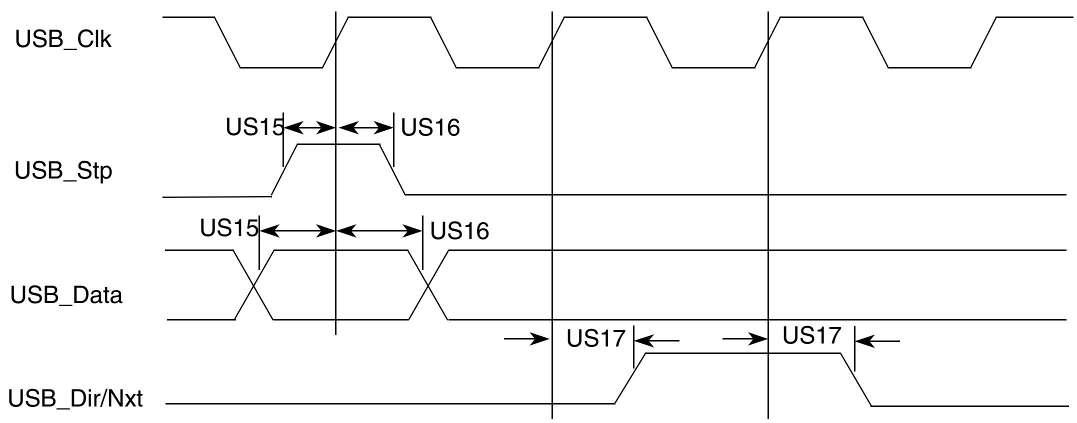


Figure 85. USB Transmit/Receive Waveform in Parallel Mode

Table 75. USB Timing Specification in VP_VM Unidirectional Mode

ID	Parameter	Min.	Max.	Unit	Conditions / Reference Signal
US15	USB_TXOE_B	—	6.0	ns	10 pF
US16	USB_DAT_VP	—	0.0	ns	10 pF
US17	USB_SE0_VM	—	9.0	ns	10 pF

4.9.19 PWM Electrical Specifications

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external

4.9.22.1 SSI Transmitter Timing with Internal Clock

Figure 92 depicts the SSI transmitter timing with internal clock, and Table 78 lists the timing parameters.

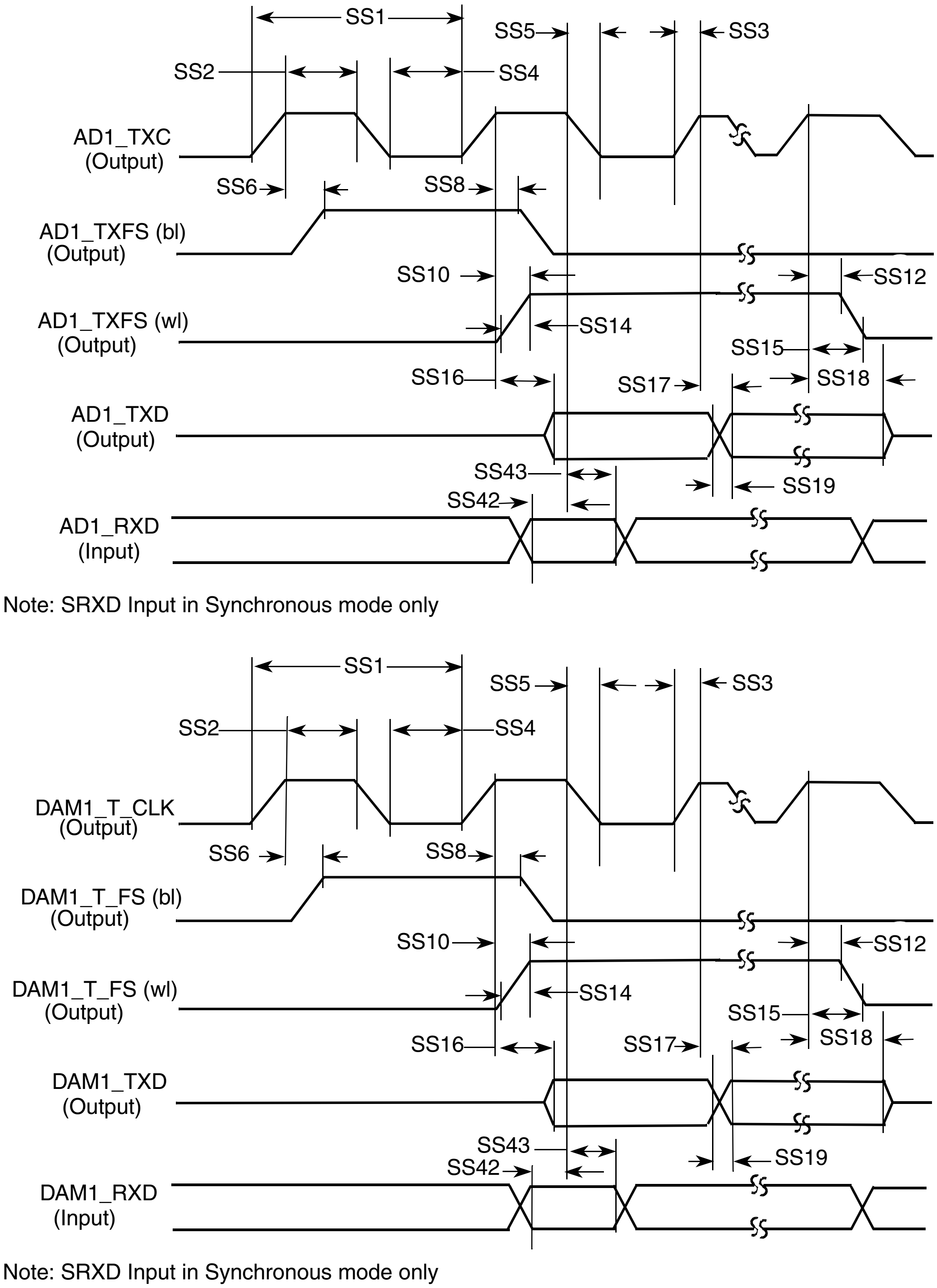


Figure 92. SSI Transmitter with Internal Clock Timing Diagram

4.9.22.2 SSI Receiver Timing with Internal Clock

Figure 93 depicts the SSI receiver timing with internal clock. Table 79 lists the timing parameters shown in Figure 93.

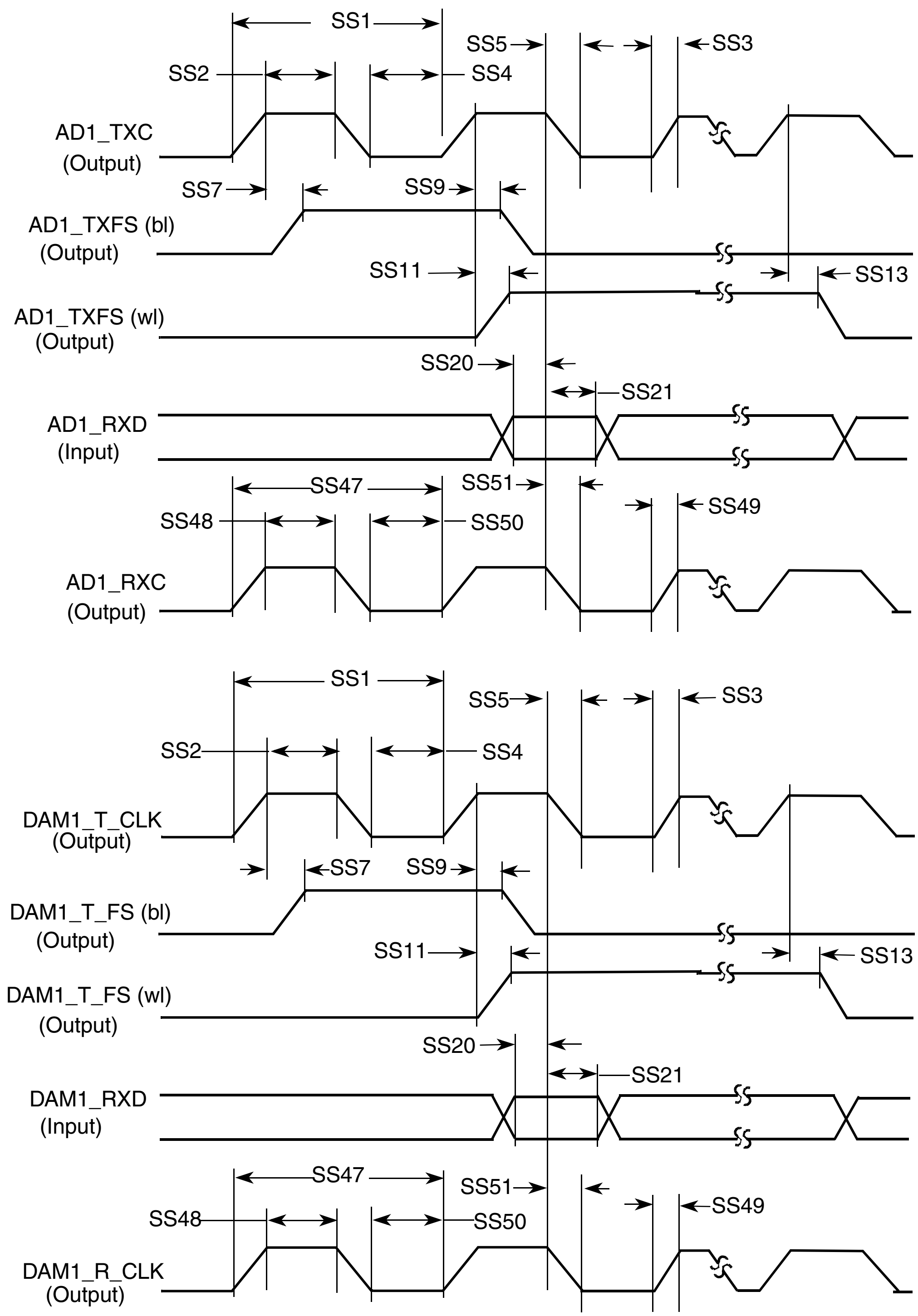


Figure 93. SSI Receiver with Internal Clock Timing Diagram

5.1 MAPBGA Production Package 1568-01, 17 × 17 mm, 0.8 Pitch

See Figure 108 for the package drawing and dimensions of the production package.

Figure 108. Production Package: Mechanical Drawing

Table 94. Silicon Revision 2.0 Signal Ball Map Locations (continued)

Signal ID	Ball Location
FEC_MDIO	P1
FEC_RDATA0	P2
FEC_RDATA1	N2
FEC_RDATA2	M3
FEC_RDATA3	N1
FEC_RX_CLK	R2
FEC_RX_DV	T2
FEC_RX_ERR	N3
MA10	C4
MGND	N11
MLB_CLK	W13
MLB_DAT	Y13
MLB_SIG	W12
MVDD	P11
NF_CE0	G3
NFALE	F2
NFCLE	E1
NFRB	F3
NFRE_B	F1
NFWE_B	G2
NFWP_B	F4
NGND_ATA	M9
NGND_ATA	P9
NGND_ATA	L10
NGND_CRM	L11
NGND_CSI	N10
NGND_EMI1	H8
NGND_EMI1	H10
NGND_EMI1	J10
NGND_EMI2	J11
NGND_EMI3	J12
NGND_EMI3	K12
NGND_JTAG	M13
NGND_LCDC	K11
NGND_LCDC	L12
NGND_MISC	M7
NGND_MISC	K8
NGND_MLB	M10
NGND_NFC	K9
NGND_SDIO	N12
NVCC_ATA	N6
NVCC_ATA	P6
NVCC_ATA	P7
NVCC_ATA	P8
NVCC_CRM	R9
NVCC_CSI	R11
LD23[1]	L19
LD3[1]	G16
LD4[1]	G19
LD5[1]	H16
LD6[1]	H18
LD7[1]	G20
LD8[1]	H17
LD9[1]	H19
NVCC_EMI2	G12
NVCC_EMI2	F13
NVCC_EMI2	F14
NVCC_EMI3	G14
NVCC_JTAG	P16
NVCC_LCDC	H14
NVCC_LCDC	J14
NVCC_LCDC	L14
NVCC_LCDC	M14
NVCC_MISC	K6
NVCC_MISC	K7
NVCC_MISC	L8
NVCC_MLB	R10
NVCC_NFC	G6
NVCC_NFC	H6
NVCC_NFC	H7
NVCC_SDIO	P14
OE	E20
OSC_AUDIO_VDD	V20
OSC_AUDIO_VSS	U19
OSC24M_VDD	T19
OSC24M_VSS	T18
PGND	M12
PHY1_VDDA	M15
PHY1_VDDA	N20
PHY1_VSSA	N16
PHY1_VSSA	P20
PHY2_VDD	R13
PHY2_VSS	P12
POR_B	W11
POWER_FAIL	Y9
PVDD	N13
RAS	E15
RESET_IN_B	U10
RTCK	U18
RTS1	U1
RTS2	G1
RW	C20

Table 95. Silicon Revision 2.1 Signal Ball Map Locations (continued)

Signal ID	Ball Location
MA10	C4
MGND	N11
MLB_CLK	W13
MLB_DAT	Y13
MLB_SIG	W12
MVDD	P11
NF_CE0	G3
NFALE	F2
NFCLE	E1
NFRB	F3
NFRE_B	F1
NFWE_B	G2
NFWP_B	F4
NGND_ATA	M9
NGND_ATA	P9
NGND_ATA	L10
NGND_CRM	L11
NGND_CSI	N10
NGND_EMI1	H8
NVCC_EMI1	H10
NGND_EMI1	J10
NGND_EMI2	J11
NGND_EMI3	J12
NGND_EMI3	K12
NGND_JTAG	M13
NGND_LCDC	K11
NGND_LCDC	L12
NGND_MISC	M7
NGND_MISC	K8
NGND_MLB	M10
NGND_NFC	K9
NGND_SDIO	N12
NVCC_ATA	N6
NVCC_ATA	P6
NVCC_ATA	P7
NVCC_ATA	P8
NVCC_CRM	R9
NVCC_CSI	R11
NVCC_EMI1	G7
NVCC_EMI1	G8
NVCC_EMI1	G9
NVCC_EMI1	H9
NGND_EMI1	F10
NVCC_EMI1	G10
NVCC_EMI1	F11
NVCC_EMI1	G11
NVCC_EMI2	G12
NVCC_EMI2	F13
VSS	F14
NVCC_EMI3	G14
NVCC_JTAG	P16
NVCC_LCDC	H14
NVCC_LCDC	J14
NVCC_LCDC	L14
NVCC_LCDC	M14
NVCC_MISC	K6
NVCC_MISC	K7
NVCC_MISC	L8
NVCC_MLB	R10
NVCC_NFC	G6
NVCC_NFC	H6
NVCC_NFC	H7
NVCC_SDIO	P14
OE	E20
OSC_AUDIO_VDD	V20
OSC_AUDIO_VSS	U19
OSC24M_VDD	T19
OSC24M_VSS	T18
PGND	M12
PHY1_VDDA	M15
PHY1_VDDA	N20
PHY1_VSSA	N16
PHY1_VSSA	P20
PHY2_VDD	R13
PHY2_VSS	P12
POR_B	W11
POWER_FAIL	Y9
PVDD	N13
BCLK	E15
RESET_IN_B	U10
RTCK	U18
RTS1	U1
RTS2	G1
RW	C20
RXD1	U2
RXD2	H3
SCK4	L4
SCK5	L5
SCKR	K3
SCKT	J4
DQM1	C17
SD1	A19