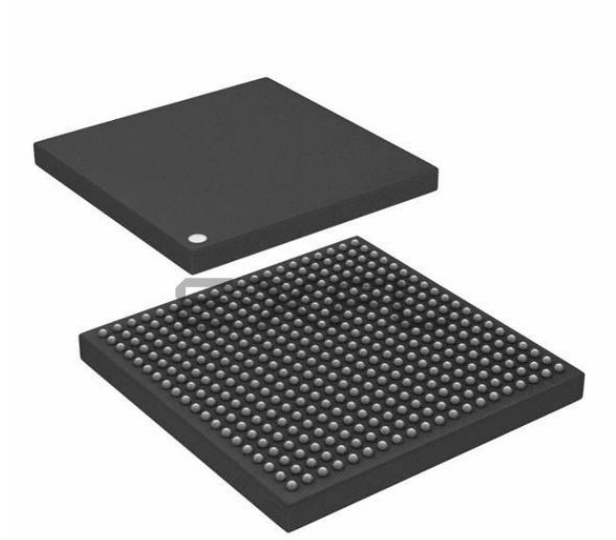

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	532MHz
Co-Processors/DSP	Multimedia; GPU, IPU, VFP
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, KPP, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Secure Fusebox, Secure JTAG
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx356avm5br2

- Flash controller—MLC/SLC NAND and NOR
- GPIO with interrupt capabilities
- 3 I^2C modules (up to 400 Kbytes each)
- JTAG
- Key pin port
- Media local bus (MLB) interface
- Asynchronous sample rate converter (ASRC)
- 1-Wire
- Parallel camera sensor (4/8/10/16-bit data port for video color models: YCC, YUV, 30 Mpixels/s)
- Parallel display (primary up to 24-bit, 1024 x 1024)
- Parallel ATA (up to 66 Mbytes) (not available for the MCIMX351)
- PWM
- SPDIF transceiver
- 3 UART (up to 4.0 Mbps each)

1.2 Ordering Information

Table 1 provides the ordering information for the i.MX35 processors for automotive applications.

Table 1. Ordering Information

Description	Part Number	Silicon Revision	Package[1]	Speed	Operating Temperature Range (°C)	Signal Ball Map Locations	Ball Map
i.MX351	MCIMX351AVM4B	2.0	5284	400 MHz	–40 to 85	Table 94	Table 96
i.MX351	MCIMX351AVM5B	2.0	5284	532 MHz[2]	–40 to 85	Table 94	Table 96
i.MX355	MCIMX355AVM4B	2.0	5284	400 MHz	–40 to 85	Table 94	Table 96
i.MX355	MCIMX355AVM5B	2.0	5284	532 MHz[2]	–40 to 85	Table 94	Table 96
i.MX356	MCIMX356AVM4B	2.0	5284	400 MHz	–40 to 85	Table 94	Table 96
i.MX356	MCIMX356AVM5B	2.0	5284	532 MHz[2]	–40 to 85	Table 94	Table 96
i.MX351	MCIMX351AJQ4C	2.1	5284	400MHz	-40 to 85	Table 95	Table 97
i.MX351	MCIMX351AJQ5C	2.1	5284	532MHz[2]	-40 to 85	Table 95	Table 97
i.MX355	MCIMX355AJQ4C	2.1	5284	400MHz	-40 to 85	Table 95	Table 97
i.MX355	MCIMX355AJQ5C	2.1	5284	532MHz[2]	-40 to 85	Table 95	Table 97
i.MX356	MCIMX356AJQ4C	2.1	5284	400MHz	-40 to 85	Table 95	Table 97
i.MX356	MCIMX356AJQ5C	2.1	5284	532MHz[2]	-40 to 85	Table 95	Table 97
i.MX356	SCIMX356BVMB	2	5284	532MHz	-40 to 85	Table 94	Table 96

1 Case 5284 is RoHS-compliant, lead-free, MSL = 3, 1.

2 532 MHz rated devices meet all specifications of 400 MHz rated devices. A 532 MHz device can be substituted in place of a 400 MHz device.

4 Electrical Characteristics

The following sections provide the device-level and module-level electrical characteristics for the i.MX35 processor.

4.1 i.MX35 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

Table 6. i.MX35 Chip-Level Conditions

Characteristics	Table/Location
Absolute Maximum Ratings	Table 7 on page 13
i.MX35 Operating Ranges	Table 8 on page 14
Interface Frequency	Table 9 on page 15

Stresses beyond those listed in Table 7 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in Table 8 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 7. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply voltage (core)	VDD_{max}[1]	–0.5	1.47	V
Supply voltage (I/O)	$NVCC_{max}$	–0.5	3.6	V
Input voltage range	V_{Imax}	–0.5	3.6	V
Storage temperature	$T_{storage}$	–40	125	°C
ESD damage immunity:	V_{esd}			V
Human Body Model (HBM)		—	2000[2]	
Charge Device Model (CDM)		—	500[3]	

1 VDD is also known as QVCC.

2 HBM ESD classification level according to the AEC-Q100-002 standard

3 Corner pins max. 750 V

Figure 6 shows the output pin transition time waveform.

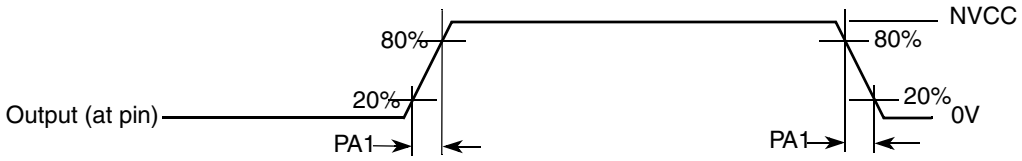


Figure 6. Output Pin Transition Time Waveform

4.8.1 AC Electrical Test Parameter Definitions

AC electrical characteristics in Table 16 through Table 21 are not applicable for the output open drain pull-down driver.

The dI/dt parameters are measured with the following methodology:

- The zero voltage source is connected between pin and load capacitance.
- The current (through this source) derivative is calculated during output transitions.

Table 15. AC Requirements of I/O Pins

Parameter	Symbol	Min.	Max.	Units
AC input logic high	VIH(ac)	NVCC ÷ 2 + 0.25	NVCC + 0.3	V
AC input logic low	VIL(ac)	–0.3	NVCC ÷ 2 – 0.25	V

Table 16. AC Electrical Characteristics of GPIO Pins in Slow Slew Rate Mode [NVCC = 3.0 V–3.6 V]

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ. Rise/Fall	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	—	60	%
Output pin slew rate (max. drive)	tps	25 pF 50 pF	0.79/1.12 0.49/0.73	1.30/1.77 0.84/1.23	2.02/2.58 1.19/1.58	V/ns
Output pin slew rate (high drive)	tps	25 pF 50 pF	0.48/0.72 0.27/0.42	0.76/1.10 0.41/0.62	1.17/1.56 0.63/0.86	V/ns
Output pin slew rate (standard drive)	tps	25 pF 50 pF	0.25/0.40 0.14/0.21	0.40/0.59 0.21/0.32	0.60/0.83 0.32/0.44	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	15 16	36 38	76 80	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	8 9	20 21	45 47	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	4 4	10 10	22 23	mA/ns

Table 21. AC Electrical Characteristics of GPIO Pins in Fast Slew Rate Mode [NVCC = 2.25 V–2.75 V]

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units	Notes
Duty cycle	Fduty	—	40	—	60	%	—
Output pin slew rate (max. drive)	tps	25 pF 40 pF 50 pF	0.84/1.10 0.68/0.83 0.58/0.72	1.45/1.80 1.14/1.34 0.86/1.10	2.40/2.80 1.88/2.06 1.40/1.70	V/ns	2
Output pin slew rate (high drive)	tps	25 pF 40 pF 50 pF	0.69/0.96 0.55/0.69 0.40/0.59	1.18/1.50 0.92/1.10 0.67/0.95	1.90/2.30 1.49/1.67 1.10/1.30	V/ns	
Output pin slew rate (standard drive)	tps	25 pF 40 pF 50 pF	0.24/0.36 0.37/0.47 0.13/0.21	0.80/1.00 0.62/0.76 0.45/0.65	1.30/1.60 1.00/1.14 0.70/0.95	V/ns	
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	46 49	124 131	310 324	mA/ns	3
Output pin di/dt (high drive)	tdit	25 pF 50 pF	33 35	89 94	290 304	mA/ns	
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	28 29	75 79	188 198	mA/ns	

4.8.2 AC Electrical Characteristics for DDR Pins (DDR2, Mobile DDR, and SDRAM Modes)

Table 22. AC Electrical Characteristics of DDR Type IO Pins in DDR2 Mode

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	45	50	55	%
Clock frequency	f	—	—	133	—	MHz
Output pin slew rate	tps	25 pF 50 pF	0.86/0.98 0.46/054	1.35/1.5 0.72/0.81	2.15/2.19 1.12/1.16	V/ns
Output pin di/dt	tdit	25 pF 50 pF	65 70	157 167	373 396	mA/ns

Table 23. AC Requirements of DDR2 Pins

Parameter[1]	Symbol	Min.	Max.	Units
AC input logic high	VIH(ac)	NVCC ÷ 2 + 0.25	NVCC + 0.3	V
AC input logic low	VIL(ac)	–0.3	NVCC ÷ 2 – 0.25	V
AC differential cross point voltage for output[2]	Vox(ac)	NVCC ÷ 2 – 0.125	NVCC ÷ 2 + 0.125	V

[1] The Jedec SSTL_18 specification (JESD8-15a) for an SSTL interface for class II operation supersedes any specification in this document.

4.9.4 Embedded Trace Macrocell (ETM) Electrical Specifications

ETM is an ARM protocol. The timing specifications in this section are given as a guide for a test point access (TPA) that supports TRACECLK frequencies up to 133 MHz.

Figure 9 depicts the TRACECLK timings of ETM, and Table 30 lists the timing parameters.

Figure 9. ETM TRACECLK Timing Diagram

Table 30. ETM TRACECLK Timing Parameters

ID	Parameter	Min.	Max.	Unit
T_{cyc}	Clock period	Frequency dependent	—	ns
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	—	3	ns
T_f	Clock and data fall time	—	3	ns

Figure 10 depicts the setup and hold requirements of the trace data pins with respect to TRACECLK, and Table 31 lists the timing parameters.

Figure 10. Trace Data Timing Diagram

Table 31. ETM Trace Data Timing Parameters

ID	Parameter	Min.	Max.	Unit
T_s	Data setup	2	—	ns
T_h	Data hold	1	—	ns

4.9.4.1 Half-Rate Clocking Mode

When half-rate clocking is used, the trace data signals are sampled by the TPA on both the rising and falling edges of TRACECLK, where TRACECLK is half the frequency of the clock shown in Figure 10. The same T_s and T_h parameters from Table 31 still apply with respect to the falling edge of the TRACECLK signal.

Table 32. NFC Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = NFC Clock Cycle[2]		Example Timing for NFC Clock ≈ 33 MHz T = 30 ns		Unit
			Min.	Max.	Min.	Max.	
NF5	$\overline{\text{NF\_WP}}$ pulse width	tWP	T – 1.0 ns		29		ns
NF6	NFALE setup time	tALS	T – 4.0 ns	—	26	—	ns
NF7	NFALE hold time	tALH	T – 4.5 ns	—	25.5	—	ns
NF8	Data setup time	tDS	T – 2.0 ns	—	28	—	ns
NF9	Data hold time	tDH	T – 5.0 ns	—	25	—	ns
NF10	Write cycle time	tWC	2T – 3.0 ns		57		ns
NF11	$\overline{\text{NFWE}}$ hold time	tWH	T – 5.0 ns		25		ns
NF12	Ready to $\overline{\text{NFRE}}$ low	tRR	6T	—	180	—	ns
NF13	$\overline{\text{NFRE}}$ pulse width	tRP	1.5T – 1.0 ns	—	44	—	ns
NF14	READ cycle time	tRC	2T – 5.5 ns	—	54.5	—	ns
NF15	$\overline{\text{NFRE}}$ high hold time	tREH	0.5T – 4.0 ns		11	—	ns
NF16	Data setup on READ	tDSR	N/A		9	—	ns
NF17	Data hold on READ	tDHR	N/A		0	—	ns

1 The flash clock maximum frequency is 50 MHz.

2 Subject to DPLL jitter specification listed in Table 28, "DPLL Specifications," on page 32.

NOTE

High is defined as 80% of signal value and low is defined as 20% of signal value.

Timing for HCLK is 133 MHz and internal NFC clock (flash clock) is approximately 33 MHz (30 ns). All timings are listed according to this NFC clock frequency (multiples of NFC clock phases), except NF16 and NF17, which are not NFC clock related.

4.9.5.2 Wireless External Interface Module (WEIM)

All WEIM output control signals may be asserted and deasserted by internal clocks related to the BCLK rising edge or falling edge according to the corresponding assertion or negation control fields. The address always begins related to BCLK falling edge but may be ended both on rising and falling edge in muxed mode according to control register configuration. Output data begins related to BCLK rising edge except in muxed mode where both rising and falling edge may be used according to control register configuration.

inserted in between EAV and SAV code. The CSI decodes and filters out the timing coding from the data stream, thus recovering SENSB_VSYNC and SENSB_HSYNC signals for internal use.

4.9.12.2.2 Gated Clock Mode

The SENSB_VSYNC, SENSB_HSYNC, and SENSB_PIX_CLK signals are used in this mode. See Figure 44.

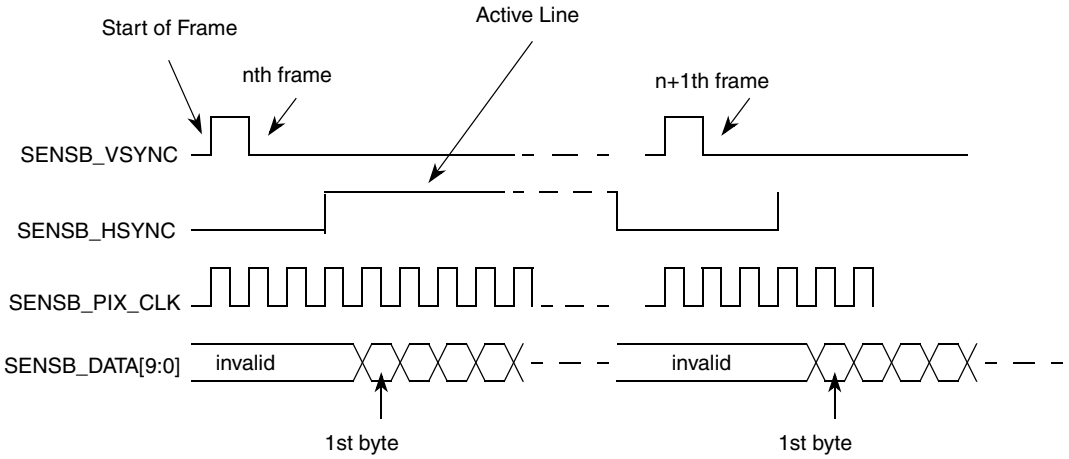


Figure 44. Gated Clock Mode Timing Diagram

A frame starts with a rising edge on SENSB_VSYNC (all the timing corresponds to straight polarity of the corresponding signals). Then SENSB_HSYNC goes to high and hold for the entire line. The pixel clock is valid as long as SENSB_HSYNC is high. Data is latched at the rising edge of the valid pixel clocks. SENSB_HSYNC goes to low at the end of the line. Pixel clocks then become invalid and the CSI stops receiving data from the stream. For the next line, the SENSB_HSYNC timing repeats. For the next frame, the SENSB_VSYNC timing repeats.

4.9.12.2.3 Non-Gated Clock Mode

The timing is the same as the gated-clock mode (described in Section 4.9.12.2.2, “Gated Clock Mode”), except for the SENSB_HSYNC signal, which is not used. See Figure 45. All incoming pixel clocks are valid and will cause data to be latched into the input FIFO. The SENSB_PIX_CLK signal is inactive (states low) until valid data is going to be transmitted over the bus.

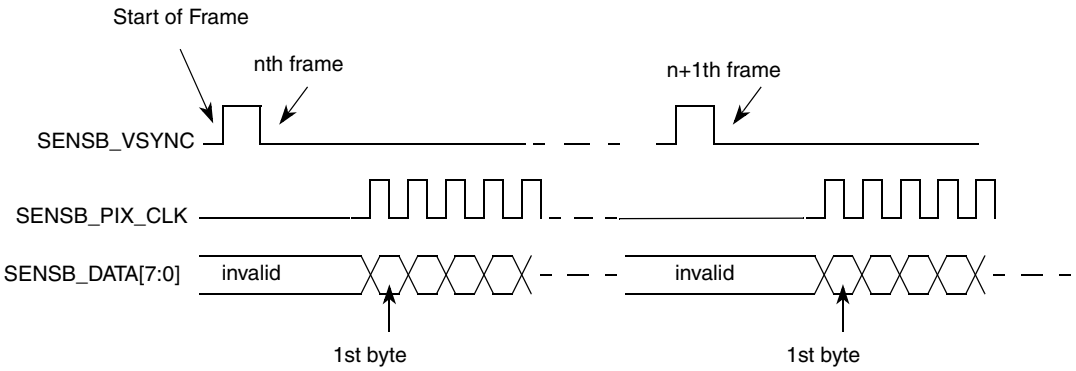


Figure 45. Non-Gated Clock Mode Timing Diagram

Additionally, the IPU allows a programmable pause between two bursts. The pause is defined in the HSP_CLK cycles. It allows the prevention of timing violation between two sequential bursts or two accesses to different displays. The range of this pause is from 4 to 19 HSP_CLK cycles.

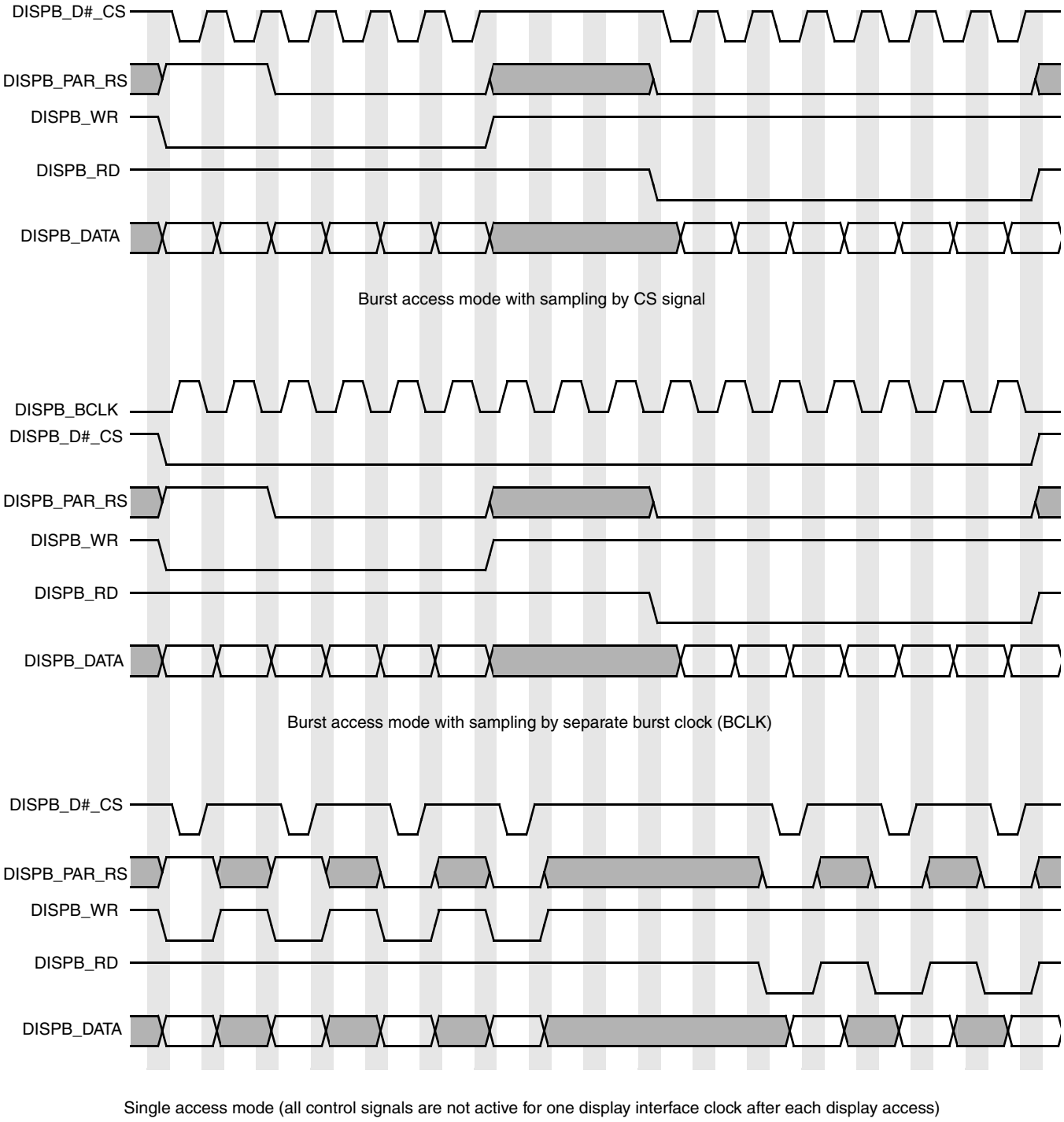


Figure 53. Asynchronous Parallel System 80 Interface (Type 1) Burst Mode Timing Diagram

4.9.13.5.10 Serial Interfaces, Electrical Characteristics

Figure 66 depicts timing of the serial interface. Table 59 lists the timing parameters at display access level.

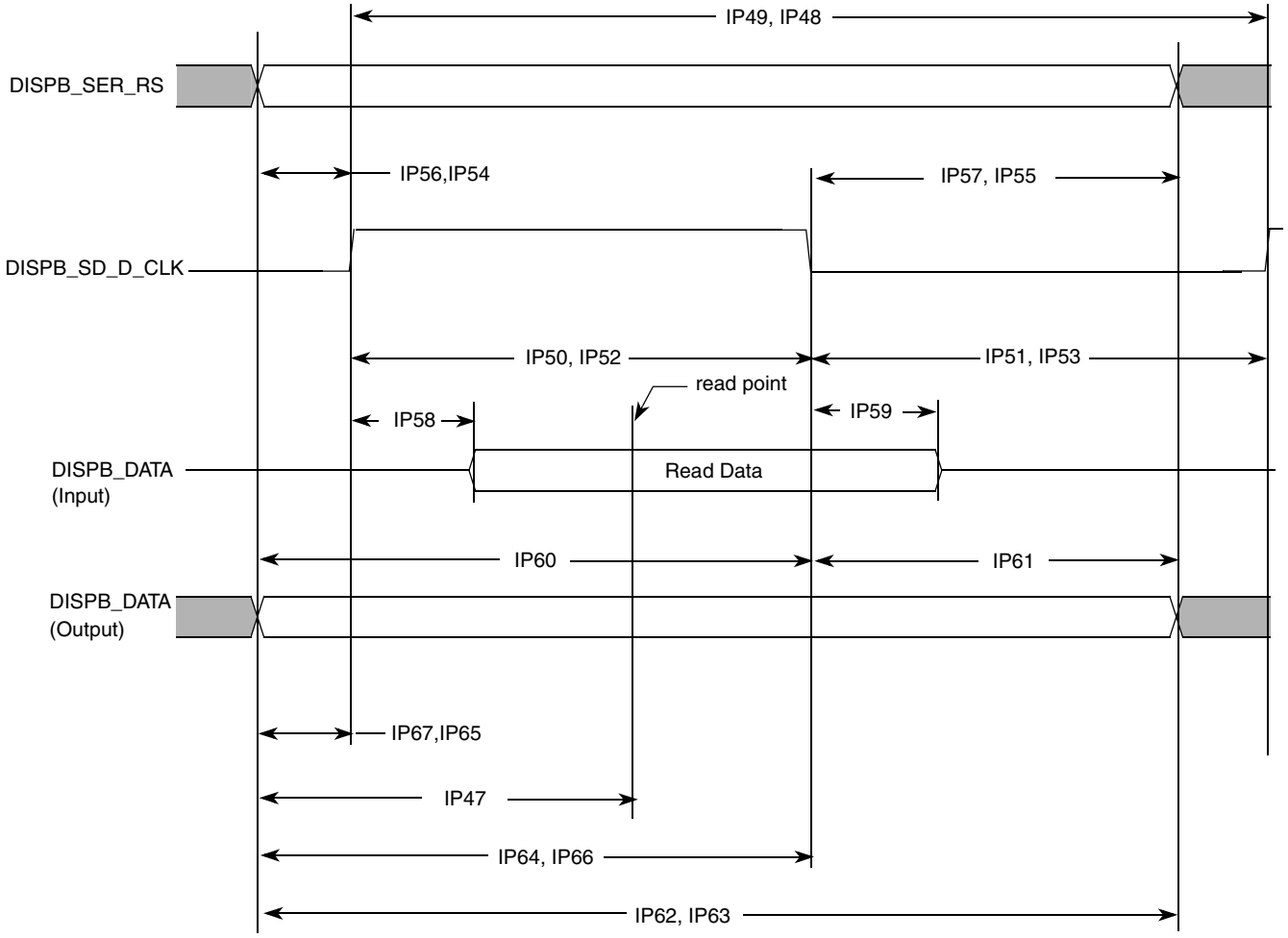


Figure 66. Asynchronous Serial Interface Timing Diagram

Table 59. Asynchronous Serial Interface Timing Parameters—Access Level

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP48	Read system cycle time	Tcycr	Tdicpr – 1.5	Tdicpr[2]	Tdicpr + 1.5	ns
IP49	Write system cycle time	Tcycw	Tdicpw – 1.5	Tdicpw[3]	Tdicpw + 1.5	ns
IP50	Read clock low pulse width	Trl	Tdicdr – Tdicur – 1.5	Tdicdr[4] – Tdicur[5]	Tdicdr – Tdicur + 1.5	ns
IP51	Read clock high pulse width	Trh	Tdicpr – Tdicdr + Tdicur – 1.5	Tdicpr – Tdicdr + Tdicur	Tdicpr – Tdicdr + Tdicur + 1.5	ns
IP52	Write clock low pulse width	Twl	Tdicdw – Tdicuw – 1.5	Tdicdw[6] – Tdicuw[7]	Tdicdw – Tdicuw + 1.5	ns
IP53	Write clock high pulse width	Twh	Tdicpw – Tdicdw + Tdicuw – 1.5	Tdicpw – Tdicdw + Tdicuw	Tdicpw – Tdicdw + Tdicuw + 1.5	ns
IP54	Controls setup time for read	Tdcsr	Tdicur – 1.5	Tdicur	—	ns

Table 59. Asynchronous Serial Interface Timing Parameters—Access Level (continued)

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP55	Controls hold time for read	Tdchr	Tdicpr – Tdicdr – 1.5	Tdicpr – Tdicdr	—	ns
IP56	Controls setup time for write	Tdcsw	Tdicuw – 1.5	Tdicuw	—	ns
IP57	Controls hold time for write	Tdchw	Tdicpw – Tdicdw – 1.5	Tdicpw – Tdicdw	—	ns
IP58	Slave device data delay[8]	Tracc	0	—	Tdrp[9] – Tlbd[10] – Tdicur – 1.5	ns
IP59	Slave device data hold time[8]	Troh	Tdrp – Tlbd – Tdicdr + 1.5	—	Tdicpr – Tdicdr – 1.5	ns
IP60	Write data setup time	Tds	Tdicdw – 1.5	Tdicdw	—	ns
IP61	Write data hold time	Tdh	Tdicpw – Tdicdw – 1.5	Tdicpw – Tdicdw	—	ns
IP62	Read period[2]	Tdicpr	Tdicpr – 1.5	Tdicpr	Tdicpr + 1.5	ns
IP63	Write period[3]	Tdicpw	Tdicpw – 1.5	Tdicpw	Tdicpw + 1.5	ns
IP64	Read down time[4]	Tdicdr	Tdicdr – 1.5	Tdicdr	Tdicdr + 1.5	ns
IP65	Read up time[5]	Tdicur	Tdicur – 1.5	Tdicur	Tdicur + 1.5	ns
IP66	Write down time[6]	Tdicdw	Tdicdw – 1.5	Tdicdw	Tdicdw + 1.5	ns
IP67	Write up time[7]	Tdicuw	Tdicuw – 1.5	Tdicuw	Tdicuw + 1.5	ns
IP68	Read time point[9]	Tdrp	Tdrp – 1.5	Tdrp	Tdrp + 1.5	ns

1 The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device specific.

2 Display interface clock period value for read:

$$Tdicpr = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_RD}{HSP\_CLK\_PERIOD}\right]$$

3 Display interface clock period value for write:

$$Tdicpw = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_WR}{HSP\_CLK\_PERIOD}\right]$$

4 Display interface clock down time for read:

$$Tdicdr = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_DOWN\_RD}{HSP\_CLK\_PERIOD}\right]$$

5 Display interface clock up time for read:

$$Tdicur = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_UP\_RD}{HSP\_CLK\_PERIOD}\right]$$

6 Display interface clock down time for write:

$$Tdicdw = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_DOWN\_WR}{HSP\_CLK\_PERIOD}\right]$$

7 Display interface clock up time for write:

$$Tdicuw = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_UP\_WR}{HSP\_CLK\_PERIOD}\right]$$

8 This parameter is a requirement to the display connected to the IPU.

Table 62. MLB 256/512 Fs Timing Parameters (continued)

Parameter	Symbol	Min	Typ	Max	Units	Comment
MLB fall time	t_{mckf}	—	—	3	ns	V_{IH} TO V_{IL}
MLBCLK cycle time	t_{mckc}	— —	81 40	— —	ns	256 × Fs 512 × Fs
MLBCLK low time	t_{mckl}	31.5 30	37 35.5	— —	ns	256 × Fs 256 × Fs PLL unlocked
		14.5 14	17 16.5	— —	ns	512 × Fs 512 × Fs PLL unlocked
MLBCLK high time	t_{mckh}	31.5 30	38 36.5	— —	ns	256 × Fs 256 × Fs PLL unlocked
		14.5 14	17 16.5	— —	ns	512 × Fs 512 × Fs PLL unlocked
MLBCLK pulse width variation	t_{mpwv}	—	—	2	ns pp	Note[2]
MLBSIG/MLBDAT input valid to MLBCLK falling	t_{dsmcf}	1	—	—	ns	—
MLBSIG/MLBDAT input hold from MLBCLK low	t_{dhmcf}	0	—	—	ns	—
MLBSIG/MLBDAT output high impedance from MLBCLK low	t_{mcfdz}	0	—	t_{mckl}	ns	—
Bus Hold Time	t_{mdzh}	4	—	—	ns	Note[3]

1 The MLB controller can shut off MLBCLK to place MediaLB in a low-power state.

2 Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (pp)

3 The board must be designed to insure that the high-impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

Ground = 0.0 V; load capacitance = 40 pF; MediaLB speed = 1024 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed below unless otherwise noted.

Table 63. MLB Device 1024Fs Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units	Comment
MLBCLK Operating Frequency[1]	f_{mck}	45.056	49.152	49.2544 51.200	MHz	Min: 1024 × Fs at 44.0 kHz Typ: 1024 × Fs at 48.0 kHz Max: 1024 × Fs at 48.1 kHz Max: 1024 × Fs PLL unlocked
MLBCLK rise time	t_{mckr}	—	—	1	ns	V_{IL} TO V_{IH}
MLB fall time	t_{mckf}	—	—	1	ns	V_{IH} TO V_{IL}
MLBCLK cycle time	t_{mckc}	—	20.3	—	ns	—
MLBCLK low time	t_{mckl}	6.5 6.1	7.7 7.3	—	ns	PLL unlocked

Figure 71 depicts write 0 sequence timing, and Table 65 lists the timing parameters.

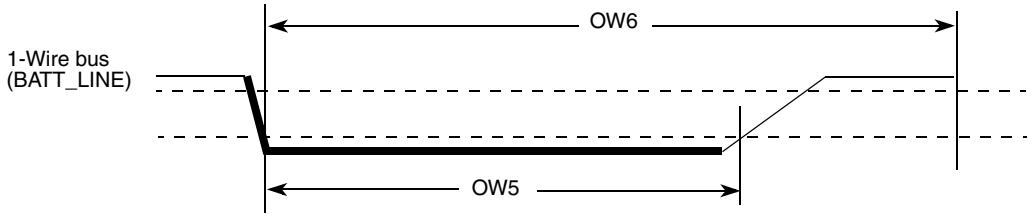


Figure 71. Write 0 Sequence Timing Diagram

Table 65. WR0 Sequence Timing Parameters

ID	Parameter	Symbol	Min.	Typ.	Max.	Units
OW5	Write 0 low time	t_{WR0_low}	60	100	120	µs
OW6	Transmission time slot	t_{SLOT}	OW5	117	120	µs

Figure 72 shows write 1 sequence timing, and Figure 73 depicts the read sequence timing. Table 66 lists the timing parameters.

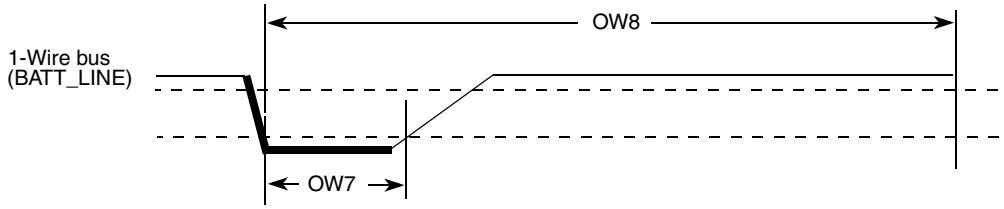


Figure 72. Write 1 Sequence Timing Diagram

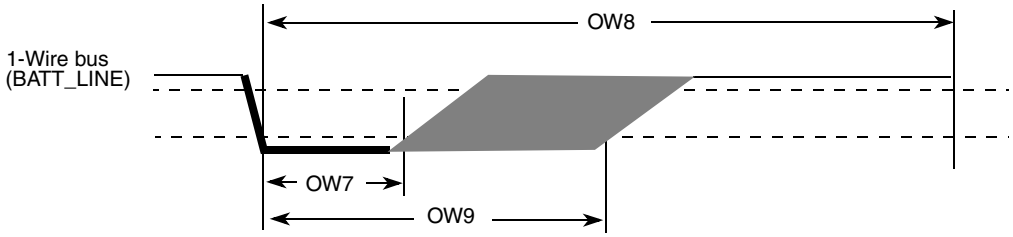


Figure 73. Read Sequence Timing Diagram

Table 66. WR1/RD Timing Parameters

ID	Parameter	Symbol	Min.	Typ.	Max.	Units
OW7	Write 1/read low time	t_{LOW1}	1	5	15	µs
OW8	Transmission time slot	t_{SLOT}	60	117	120	µs
OW9	Release time	$t_{RELEASE}$	15	—	45	µs

4.9.17 Parallel ATA Module AC Electrical Specifications

The parallel ATA module can work on PIO/multiword DMA/ultra-DMA transfer modes (not available for the MCIMX351). Each transfer mode has a different data transfer rate, Ultra DMA mode 4 data transfer rate is up to 100 MBps.

The parallel ATA module interface consists of a total of 29 pins. Some pins have different functions in different transfer modes. There are various requirements for timing relationships among the function pins, in compliance with the ATA/ATAPI-6 specification, and these requirements are configurable by the ATA module registers.

4.9.17.1 General Timing Requirements

Table 67 and Figure 74 define the AC characteristics of the interface signals on all data transfer modes.

Table 67. AC Characteristics of All Interface Signals

ID	Parameter	Symbol	Min.	Max.	Unit
SI1	Rising edge slew rate for any signal on the ATA interface[1]	S_{rise}[1]	—	1.25	V/ns
SI2	Falling edge slew rate for any signal on the ATA interface[1]	S_{fall}[1]	—	1.25	V/ns
SI3	Host interface signal capacitance at the host connector	C_{host}	—	20	pF

[1] SRISE and SFALL meet this requirement when measured at the sender's connector from 10–90% of full signal amplitude with all capacitive loads from 15 pF through 40 pF, where all signals have the same capacitive load value.

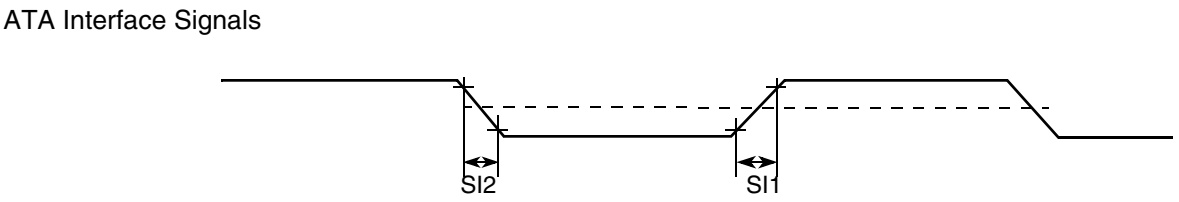


Figure 74. ATA Interface Signals Timing Diagram

4.9.17.2 ATA Electrical Specifications (ATA Bus, Bus Buffers)

This section discusses ATA parameters. For a detailed description, refer to the ATA-6 specification.

Level shifters are required for 3.3-V or 5.0-V compatibility on the ATA interface.

The use of bus buffers introduces delays on the bus and introduces skew between signal lines. These factors make it difficult to operate the bus at the highest speed (UDMA-5) when bus buffers are used. Use of bus buffers is not recommended if fast UDMA mode is required.

The ATA specification imposes a slew rate limit on the ATA bus. According to this limit, any signal driven on the bus should have a slew rate between 0.4 and 1.2 V/ns with a 40 pF load. Few vendors of bus buffers specify the slew rate of the outgoing signals.

When bus buffers are used the ata_data bus buffer is bidirectional, and uses the direction control signal ata_buffer_en. When ata_buffer_en is asserted, the bus should drive from host to device. When

Table 76. SJC Timing Parameters (continued)

ID	Parameter	All Frequencies		Unit
		Min.	Max.	
SJ11	TCK low to TDO high impedance	—	44	ns
SJ12	$\overline{\text{TRST}}$ assert time	100	—	ns
SJ13	$\overline{\text{TRST}}$ set-up time to TCK low	40	—	ns

1 On cases where SDMA TAP is put in the chain, the max. TCK frequency is limited by max. ratio of 1:8 of SDMA core frequency to TCK limitation. This implies max. frequency of 8.25 MHz (or 121.2 ns) for 66 MHz IPG clock.

2 V_M = mid point voltage

4.9.21 SPDIF Timing

SPDIF data is sent using bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Figure 90 shows SPDIF timing parameters, including the timing of the modulating Rx clock (SRCK) for SPDIF in Rx mode and the timing of the modulating Tx clock (STCLK). for SPDIF in Tx mode.

Table 77. SPDIF Timing Parameters

Parameters	Symbol	Timing Parameter Range		Units
		Min.	Max.	
SPDIFIN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIFOUT output (Load = 50 pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 24.2 31.3	ns
SPDIFOUT1 output (Load = 30 pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 13.6 18.0	ns
Modulating Rx clock (SRCK) period	srckp	40.0	—	ns
SRCK high period	srckph	16.0	—	ns
SRCK low period	srckpl	16.0	—	ns
Modulating Tx clock (STCLK) period	stclkp	40.0	—	ns
STCLK high period	stclkph	16.0	—	ns
STCLK low period	stclkpl	16.0	—	ns

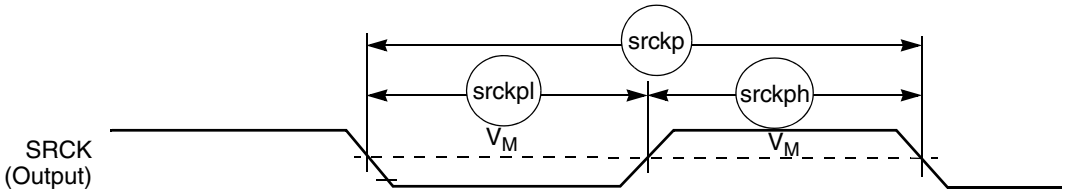


Figure 90. SRCK Timing

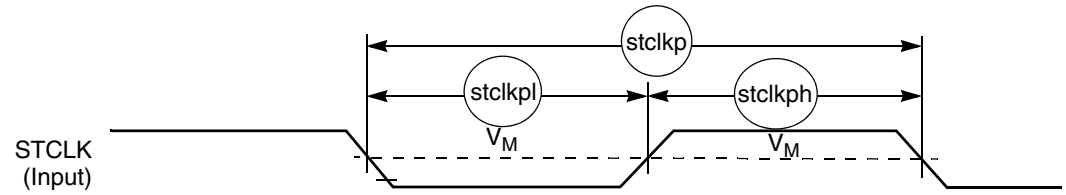


Figure 91. STCLK Timing

4.9.22 SSI Electrical Specifications

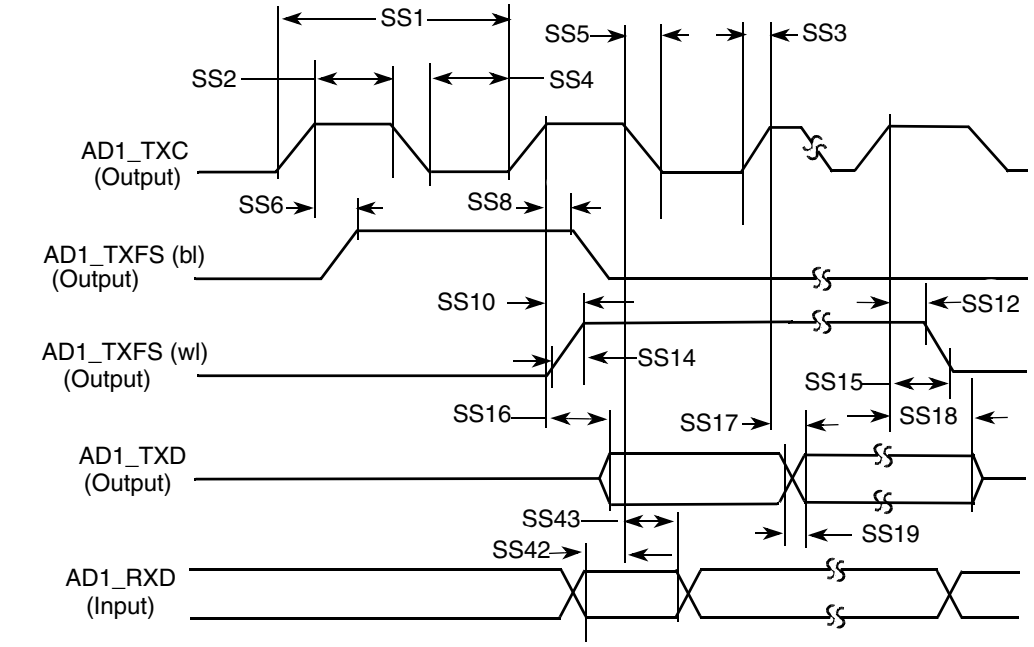
This section describes electrical characteristics of the SSI.

NOTE

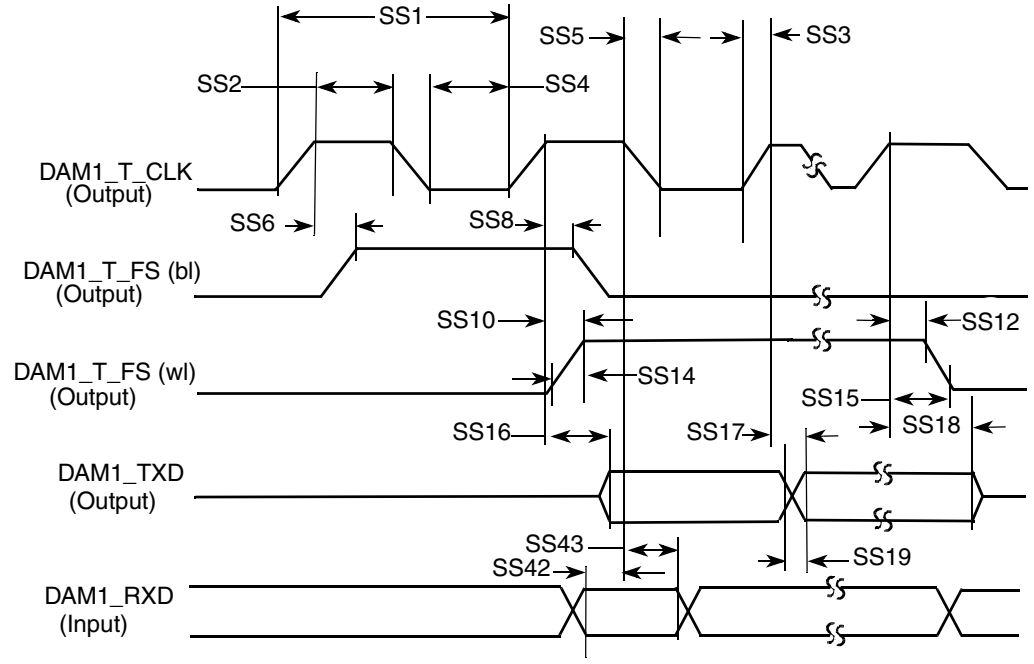
- All of the timing for the SSI is given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timing is on AUDMUX signals when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the transmit and receive sections of the SSI, respectively.
- For internal frame sync operations using the external clock, the FS timing will be the same as that of Tx Data (for example, during AC97 mode of operation).

4.9.22.1 SSI Transmitter Timing with Internal Clock

Figure 92 depicts the SSI transmitter timing with internal clock, and Table 78 lists the timing parameters.



Note: SRXD Input in Synchronous mode only



Note: SRXD Input in Synchronous mode only

Figure 92. SSI Transmitter with Internal Clock Timing Diagram

4.9.22.3 SSI Transmitter Timing with External Clock

Figure 94 depicts the SSI transmitter timing with external clock, and Table 80 lists the timing parameters.

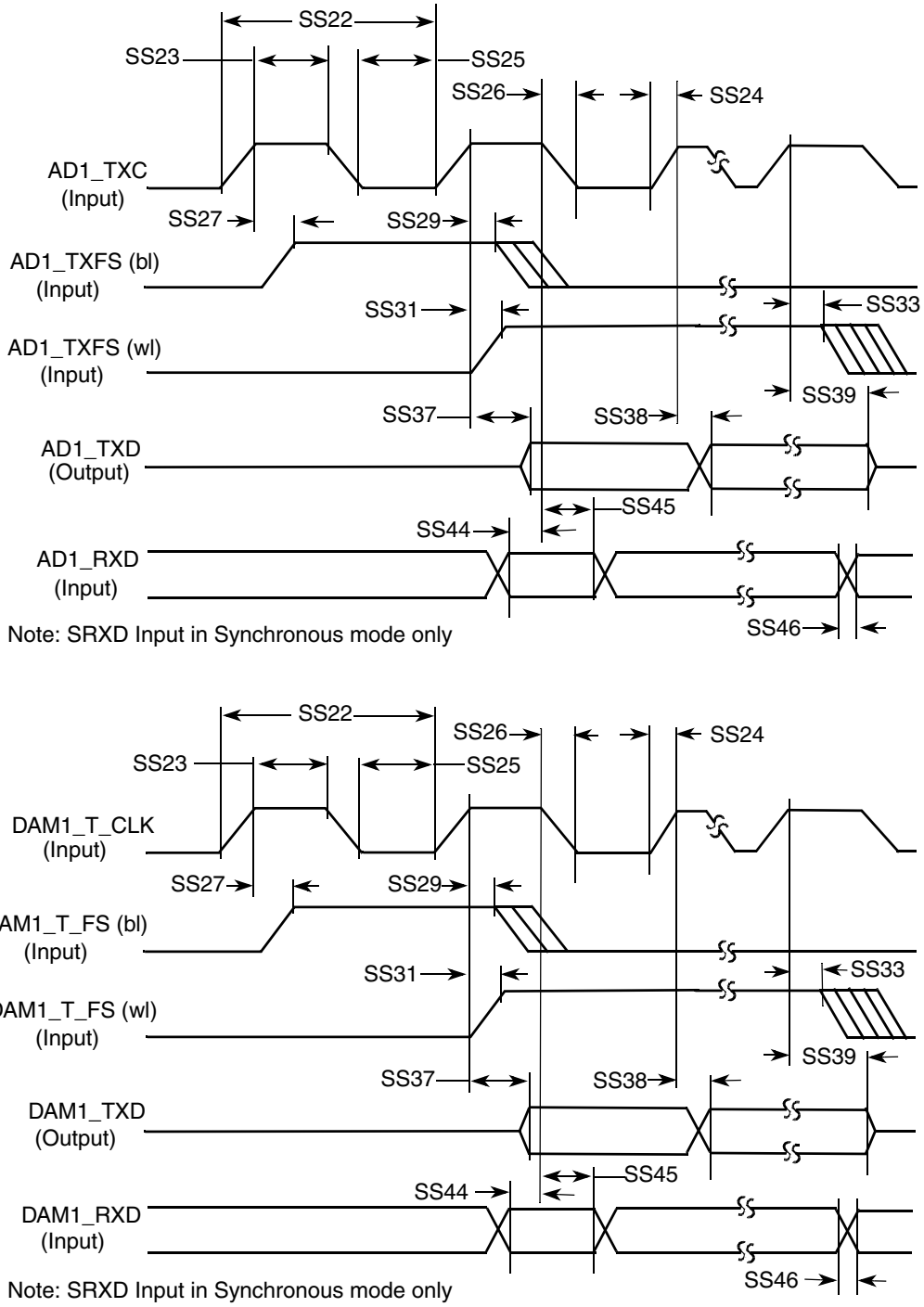


Figure 94. SSI Transmitter with External Clock Timing Diagram

Table 82. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$ [1] – T_{ref_clk} [2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.
[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.9.23.1.12 UART Receiver

Figure 97 depicts the RS-232 serial mode receive timing, with 8 data bit/1 stop bit format. Table 83 lists serial mode receive timing characteristics.

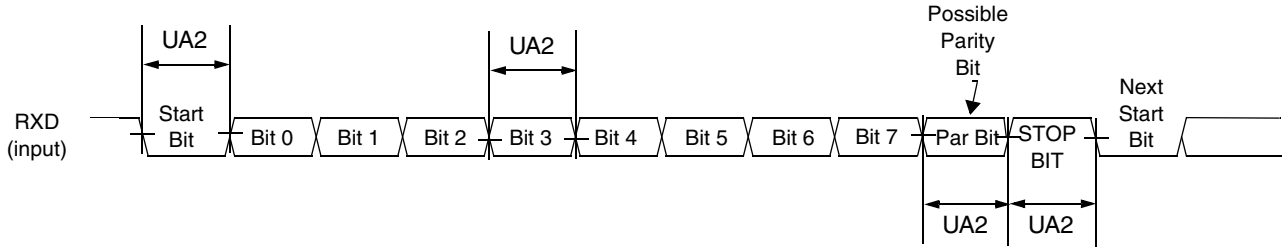


Figure 97. UART RS-232 Serial Mode Receive Timing Diagram

Table 83. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$ [2] – $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—

[1] The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.
[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency) ÷ 16.

4.9.23.2 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

4.9.23.2.13 UART IrDA Mode Transmitter

Figure 98 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 84 lists the transmit timing characteristics.

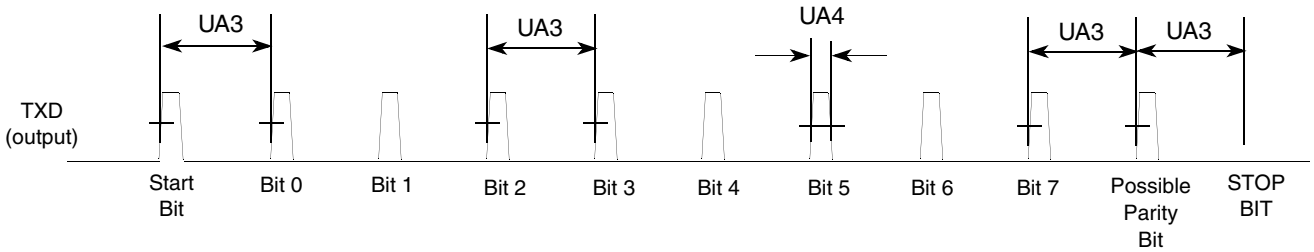


Figure 98. UART IrDA Mode Transmit Timing Diagram

Table 94. Silicon Revision 2.0 Signal Ball Map Locations (continued)

Signal ID	Ball Location
FEC_MDIO	P1
FEC_RDATA0	P2
FEC_RDATA1	N2
FEC_RDATA2	M3
FEC_RDATA3	N1
FEC_RX_CLK	R2
FEC_RX_DV	T2
FEC_RX_ERR	N3
MA10	C4
MGND	N11
MLB_CLK	W13
MLB_DAT	Y13
MLB_SIG	W12
MVDD	P11
NF_CE0	G3
NFALE	F2
NFCLE	E1
NFRB	F3
NFRE_B	F1
NFWE_B	G2
NFWP_B	F4
NGND_ATA	M9
NGND_ATA	P9
NGND_ATA	L10
NGND_CRM	L11
NGND_CSI	N10
NGND_EMI1	H8
NGND_EMI1	H10
NGND_EMI1	J10
NGND_EMI2	J11
NGND_EMI3	J12
NGND_EMI3	K12
NGND_JTAG	M13
NGND_LCDC	K11
NGND_LCDC	L12
NGND_MISC	M7
NGND_MISC	K8
NGND_MLB	M10
NGND_NFC	K9
NGND_SDIO	N12
NVCC_ATA	N6
NVCC_ATA	P6
NVCC_ATA	P7
NVCC_ATA	P8
NVCC_CRM	R9
NVCC_CSI	R11

Signal ID	Ball Location
LD23[1]	L19
LD3[1]	G16
LD4[1]	G19
LD5[1]	H16
LD6[1]	H18
LD7[1]	G20
LD8[1]	H17
LD9[1]	H19
NVCC_EMI2	G12
NVCC_EMI2	F13
NVCC_EMI2	F14
NVCC_EMI3	G14
NVCC_JTAG	P16
NVCC_LCDC	H14
NVCC_LCDC	J14
NVCC_LCDC	L14
NVCC_LCDC	M14
NVCC_MISC	K6
NVCC_MISC	K7
NVCC_MISC	L8
NVCC_MLB	R10
NVCC_NFC	G6
NVCC_NFC	H6
NVCC_NFC	H7
NVCC_SDIO	P14
OE	E20
OSC_AUDIO_VDD	V20
OSC_AUDIO_VSS	U19
OSC24M_VDD	T19
OSC24M_VSS	T18
PGND	M12
PHY1_VDDA	M15
PHY1_VDDA	N20
PHY1_VSSA	N16
PHY1_VSSA	P20
PHY2_VDD	R13
PHY2_VSS	P12
POR_B	W11
POWER_FAIL	Y9
PVDD	N13
RAS	E15
RESET_IN_B	U10
RTCK	U18
RTS1	U1
RTS2	G1
RW	C20

Table 95. Silicon Revision 2.1 Signal Ball Map Locations (continued)

Signal ID	Ball Location
MA10	C4
MGND	N11
MLB_CLK	W13
MLB_DAT	Y13
MLB_SIG	W12
MVDD	P11
NF_CE0	G3
NFALE	F2
NFCLE	E1
NFRB	F3
NFRE_B	F1
NFWE_B	G2
NFWP_B	F4
NGND_ATA	M9
NGND_ATA	P9
NGND_ATA	L10
NGND_CRM	L11
NGND_CSI	N10
NGND_EMI1	H8
NVCC_EMI1	H10
NGND_EMI1	J10
NGND_EMI2	J11
NGND_EMI3	J12
NGND_EMI3	K12
NGND_JTAG	M13
NGND_LCDC	K11
NGND_LCDC	L12
NGND_MISC	M7
NGND_MISC	K8
NGND_MLB	M10
NGND_NFC	K9
NGND_SDIO	N12
NVCC_ATA	N6
NVCC_ATA	P6
NVCC_ATA	P7
NVCC_ATA	P8
NVCC_CRM	R9
NVCC_CSI	R11
NVCC_EMI1	G7
NVCC_EMI1	G8
NVCC_EMI1	G9
NVCC_EMI1	H9
NGND_EMI1	F10
NVCC_EMI1	G10
NVCC_EMI1	F11
NVCC_EMI1	G11

Signal ID	Ball Location
NVCC_EMI2	G12
NVCC_EMI2	F13
VSS	F14
NVCC_EMI3	G14
NVCC_JTAG	P16
NVCC_LCDC	H14
NVCC_LCDC	J14
NVCC_LCDC	L14
NVCC_LCDC	M14
NVCC_MISC	K6
NVCC_MISC	K7
NVCC_MISC	L8
NVCC_MLB	R10
NVCC_NFC	G6
NVCC_NFC	H6
NVCC_NFC	H7
NVCC_SDIO	P14
OE	E20
OSC_AUDIO_VDD	V20
OSC_AUDIO_VSS	U19
OSC24M_VDD	T19
OSC24M_VSS	T18
PGND	M12
PHY1_VDDA	M15
PHY1_VDDA	N20
PHY1_VSSA	N16
PHY1_VSSA	P20
PHY2_VDD	R13
PHY2_VSS	P12
POR_B	W11
POWER_FAIL	Y9
PVDD	N13
BCLK	E15
RESET_IN_B	U10
RTCK	U18
RTS1	U1
RTS2	G1
RW	C20
RXD1	U2
RXD2	H3
SCK4	L4
SCK5	L5
SCKR	K3
SCKT	J4
DQM1	C17
SD1	A19