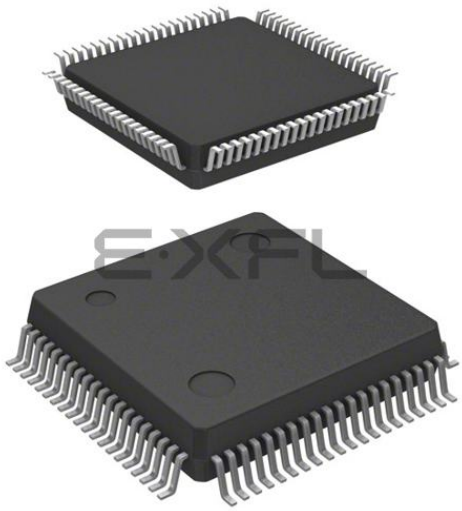

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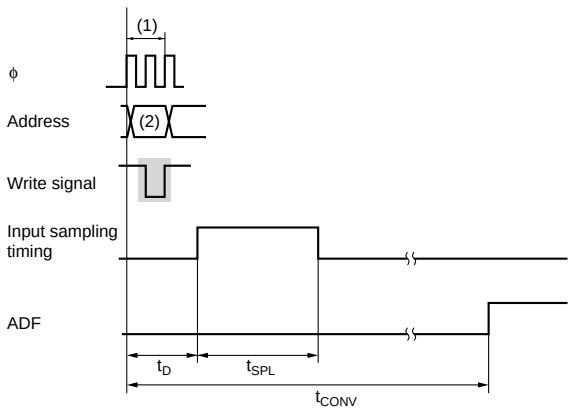
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	IrDA, SCI
Peripherals	POR, PWM, WDT
Number of I/O	57
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2132rfa20v

Item	Page	Revision (See Manual for Details)
16.4 Usage Notes	514 to 521	• Notes on WAIT Function • Notes on ICDR Reads and ICCR Access in Slave Transmit Mode • Notes on TRS Bit Setting in Slave Mode • Notes on Notes on Arbitration Lost in Master Mode • Notes on Interrupt Occurrence after ACKB Reception Description added
17.1.3 Input and Output Pins Table 17.1 Host Interface Input/Output Pins	525	Note * amended Note: * Selection of $\overline{CS2}$ or $\overline{ECS2}$ is by means of the CS2E bit in SYSCR and ...
19.4.3 Input Sampling and A/D Conversion Time Figure 19.5 A/D Conversion Timing	566	Figure 19.5 amended 
19.6 Usage Notes Figure 19.11 Example of Analog Input Circuit	572	Note added Note: Values are reference values.
21.5.2 Flash Memory Control Register 2 (FLMCR2)	590	Description amended Bits 6 to 2—Reserved: Always write 0 when writing to these bits.
21.6.1 Boot Mode	597	Description amended ... H'(FF)E080 to H'(FF)EFFF (3968 bytes) in the 128-kbyte versions including H8S/2132, except for H8S/2132R or H'(FF)E880 to H'(FF)EFFF (1920 bytes) in the 64-kbyte versions including H8S/2132R, except for H8S/2132.

2.6.3 Table of Instructions Classified by Function

Table 2.3 summarizes the instructions in each functional category. The notation used in table 2.3 is defined below.

Operation Notation

Rd	General register (destination)*
Rs	General register (source)*
Rn	General register*
ERn	General register (32-bit register)
(EAd)	Destination operand
(EAs)	Source operand
EXR	Extended control register
CCR	Condition-code register
N	N (negative) flag in CCR
Z	Z (zero) flag in CCR
V	V (overflow) flag in CCR
C	C (carry) flag in CCR
PC	Program counter
SP	Stack pointer
#IMM	Immediate data
disp	Displacement
+	Addition
–	Subtraction
×	Multiplication
÷	Division
∧	Logical AND
∨	Logical OR
⊕	Logical exclusive OR
→	Move
¬	NOT (logical complement)
:8/:16/:24/:32	8-, 16-, 24-, or 32-bit length

Note: * General registers include 8-bit registers (R0H to R7H, R0L to R7L), 16-bit registers (R0 to R7, E0 to E7), and 32-bit registers (ER0 to ER7).

Interrupts KIN7 to KIN0: Interrupts KIN7 to KIN0 are requested by input signals at pins $\overline{\text{KIN7}}$ to $\overline{\text{KIN0}}$. When any of pins $\overline{\text{KIN7}}$ to $\overline{\text{KIN0}}$ are used as key-sense inputs, the corresponding KMIMR bits should be cleared to 0 to enable those key-sense input interrupts. The remaining unused key-sense input KMIMR bits should be set to 1 to disable those interrupts. Interrupts KIN7 to KIN0 correspond to the IRQ6 interrupt. Interrupt request generation pin conditions, interrupt request enabling, interrupt control level setting, and interrupt request status indications, are all in accordance with the IRQ6 interrupt settings.

When pins $\overline{\text{KIN7}}$ to $\overline{\text{KIN0}}$ are used as key-sense interrupt input pins, either low-level sensing or falling-edge sensing must be designated as the interrupt sense condition for the corresponding interrupt source (IRQ6).

5.3.2 Internal Interrupts

There are 38 sources for internal interrupts from on-chip supporting modules, plus one software interrupt source (address break).

- For each on-chip supporting module there are flags that indicate the interrupt request status, and enable bits that select enabling or disabling of these interrupts. If any one of these is set to 1, an interrupt request is issued to the interrupt controller.
- The interrupt control level can be set by means of ICR.
- The DTC can be activated by an FRT, TMR, SCI, or other interrupt request. When the DTC is activated by an interrupt, the interrupt control mode and interrupt mask bits have no effect.

5.3.3 Interrupt Exception Vector Table

Table 5.4 shows interrupt exception handling sources, vector addresses, and interrupt priorities. For default priorities, the lower the vector number, the higher the priority.

Priorities among modules can be set by means of ICR. The situation when two or more modules are set to the same priority, and priorities within a module, are fixed as shown in table 5.4.

6.7 Bus Arbitration

6.7.1 Overview

The H8S/2138 Group and H8S/2134 Group have a bus arbiter that arbitrates bus master operations.

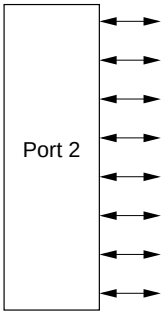
There are two bus masters, the CPU and the DTC, which perform read/write operations when they have possession of the bus. Each bus master requests the bus by means of a bus request signal. The bus arbiter determines priorities at the prescribed timing, and permits use of the bus by means of a bus request acknowledge signal. The selected bus master then takes possession of the bus and begins its operation.

6.7.2 Operation

The bus arbiter detects the bus masters' bus request signals, and if the bus is requested, sends a bus request acknowledge signal to the bus master making the request. If there are bus requests from both bus masters, the bus request acknowledge signal is sent to the one with the higher priority. When a bus master receives the bus request acknowledge signal, it takes possession of the bus until that signal is canceled.

The order of priority of the bus masters is as follows:

(High) DTC > CPU (Low)



Port 2 pins	Pin functions in mode 1
P27/A15/PW15/CBLANK	A15 (Output)
P26/A14/PW14	A14 (Output)
P25/A13/PW13	A13 (Output)
P24/A12/PW12	A12 (Output)
P23/A11/PW11	A11 (Output)
P22/A10/PW10	A10 (Output)
P21/A9/PW9	A9 (Output)
P20/A8/PW8	A8 (Output)

Pin functions in modes 2 and 3 (EXPE = 1)

A15 (Output)/P27 (I/O)/PW15 (Output)/CBLANK (Output)
A14 (Output)/P26 (I/O)/PW14 (Output)
A13 (Output)/P25 (I/O)/PW13 (Output)
A12 (Output)/P24 (I/O)/PW12 (Output)
A11 (Output)/P23 (Input)/PW11 (Output)
A10 (Output)/P22 (Input)/PW10 (Output)
A9 (Output)/P21 (Input)/PW9 (Output)
A8 (Output)/P20 (Input)/PW8 (Output)

Pin functions in modes 2 and 3 (EXPE = 0)

P27 (I/O)/PW15 (Output)/CBLANK (Output)
P26 (I/O)/PW14 (Output)
P25 (I/O)/PW13 (Output)
P24 (I/O)/PW12 (Output)
P23 (I/O)/PW11 (Output)
P22 (I/O)/PW10 (Output)
P21 (I/O)/PW9 (Output)
P20 (I/O)/PW8 (Output)

Figure 8.5 Port 2 Pin Functions

8.6 Port 5

8.6.1 Overview

Port 5 is a 3-bit I/O port. Port 5 pins also function as SCI0 I/O pins (TxD0, RxD0, SCK0), and the IIC0 I/O pin (SCL0) (option in H8S/2138 Group only). In the H8S/2138 Group, P52 and SCK0 are NMOS push-pull outputs, and SCL0 is an NMOS open-drain output. Port 5 pin functions are the same in all operating modes.

Figure 8.13 shows the port 5 pin configuration.

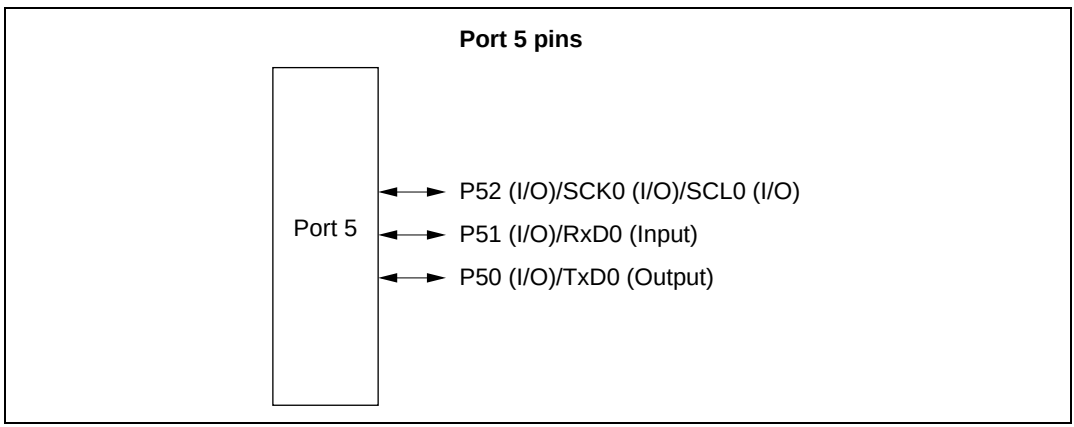


Figure 8.13 Port 5 Pin Functions

8.6.2 Register Configuration

Table 8.11 shows the port 5 register configuration.

Table 8.11 Port 5 Registers

Name	Abbreviation	R/W	Initial Value	Address*
Port 5 data direction register	P5DDR	W	H'F8	H'FFB8
Port 5 data register	P5DR	R/W	H'F8	H'FFBA

Note: * Lower 16 bits of the address.

10.2.3 PWM D/A Control Register (DACR)

Bit	7	6	5	4	3	2	1	0
	TEST	PWME	—	—	OEB	OEA	OS	CKS
Initial value	0	0	1	1	0	0	0	0
Read/Write	R/W	R/W	—	—	R/W	R/W	R/W	R/W

DACR is an 8-bit readable/writable register that selects test mode, enables the PWM outputs, and selects the output phase and operating speed.

DACR is initialized to H'30 by a reset, and in the standby modes, watch mode, subactive mode, subsleep mode, and module stop mode.

Bit 7—Test Mode (TEST): Selects test mode, which is used in testing the chip. Normally this bit should be cleared to 0.

Bit 7

TEST	Description	
0	PWM (D/A) in user state: normal operation	(Initial value)
1	PWM (D/A) in test state: correct conversion results unobtainable	

Bit 6—PWM Enable (PWME): Starts or stops the PWM D/A counter (DACNT).

Bit 6

PWME	Description	
0	DACNT operates as a 14-bit up-counter	(Initial value)
1	DACNT halts at H'0003	

Bits 5 and 4—Reserved: These bits cannot be modified and are always read as 1.

Bit 3—Output Enable B (OEB): Enables or disables output on PWM D/A channel B.

Bit 3

OEB	Description	
0	PWM (D/A) channel B output (at the PWX1 pin) is disabled	(Initial value)
1	PWM (D/A) channel B output (at the PWX1 pin) is enabled	

12.6.2 Contention between TCNT Write and Increment

If a timer counter clock pulse is generated during the T2 state of a TCNT write cycle, the write takes priority and the counter is not incremented. Figure 12.14 shows this operation.

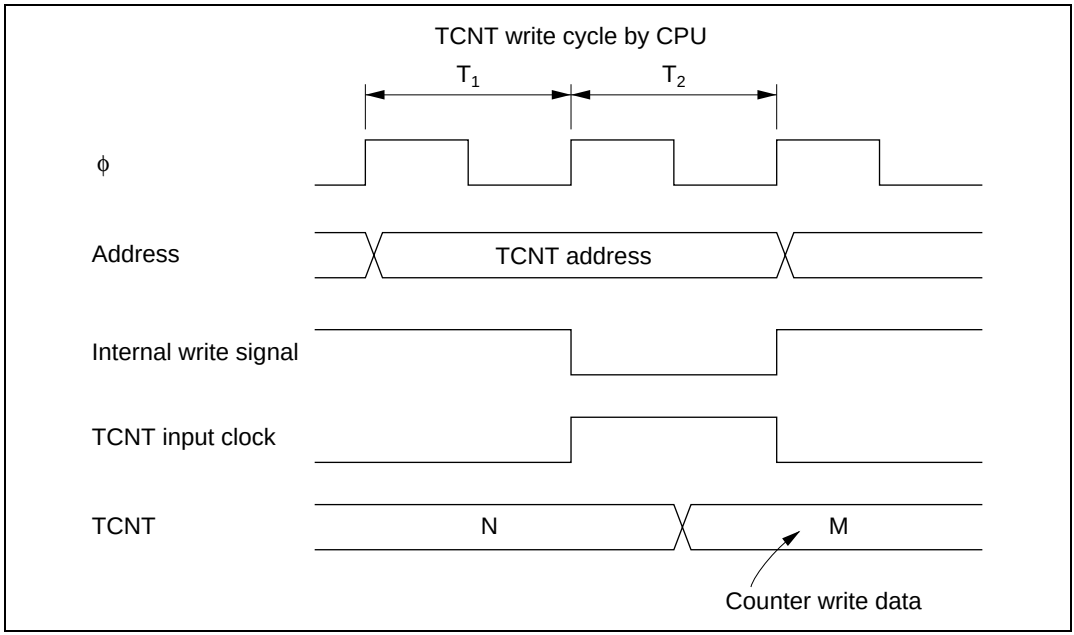


Figure 12.14 Contention between TCNT Write and Increment

Table 15.6 Maximum Bit Rate with External Clock Input (Asynchronous Mode)

ϕ (MHz)	External Input Clock (MHz)	Maximum Bit Rate (bits/s)
2	0.5000	31250
2.097152	0.5243	32768
2.4576	0.6144	38400
3	0.7500	46875
3.6864	0.9216	57600
4	1.0000	62500
4.9152	1.2288	76800
5	1.2500	78125
6	1.5000	93750
6.144	1.5360	96000
7.3728	1.8432	115200
8	2.0000	125000
9.8304	2.4576	153600
10	2.5000	156250
12	3.0000	187500
12.288	3.0720	192000
14	3.5000	218750
14.7456	3.6864	230400
16	4.0000	250000
17.2032	4.3008	268800
18	4.5000	281250
19.6608	4.9152	307200
20	5.0000	312500

Bit 0—Acknowledge Bit (ACKB): Stores acknowledge data. In transmit mode, after the receiving device receives data, it returns acknowledge data, and this data is loaded into ACKB. In receive mode, after data has been received, the acknowledge data set in this bit is sent to the transmitting device.

When this bit is read, in transmission (when TRS = 1), the value loaded from the bus line (returned by the receiving device) is read. In reception (when TRS = 0), the value set by internal software is read.

When this bit is written to, the acknowledge data transmitted at the receipt is rewritten regardless of the TRS value. The data loaded from the receiving device is retained, therefore take care of using bit-manipulation instructions.

Bit 0

ACKB	Description
0	Receive mode: 0 is output at acknowledge output timing (Initial value) Transmit mode: Indicates that the receiving device has acknowledged the data (signal is 0)
1	Receive mode: 1 is output at acknowledge output timing Transmit mode: Indicates that the receiving device has not acknowledged the data (signal is 1)

16.2.7 Serial Timer Control Register (STCR)

Bit	7	6	5	4	3	2	1	0
	—	IICX1	IICX0	IICE	FLSHE	—	ICKS1	ICKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

STCR is an 8-bit readable/writable register that controls register access, the I²C interface operating mode (when the on-chip IIC option is included), and on-chip flash memory (F-ZTAT versions), and selects the TCNT input clock source. For details of functions not related to the I²C bus interface, see section 3.2.4, Serial Timer Control Register (STCR), and the descriptions of the relevant modules. If a module controlled by STCR is not used, do not write 1 to the corresponding bit.

STCR is initialized to H'00 by a reset and in hardware standby mode.

Bit 7—Reserved: Do not write 1 to this bit.

Writing to ICDR and clearing of the IRIC flag must be executed continuously, so that no interrupt is inserted.

If a period of time that is equal to transfer one byte has elapsed by the time the IRlC flag is cleared, the end of transfer cannot be identified.

The master device sequentially sends the transmit clock and the data written to ICDR with the timing shown in figure 16.7. The selected slave device (i.e. , the slave device with the matching slave address) drives SDA low at the 9th transmit clock pulse and returns an acknowledge signal.

[7] When one frame of data has been transimitted, the IRIC flag is set to 1 at the rise of the 9th transmit clock pulse. After one frame has been transmitted, SCL is automatically fixed low in synchronization with the internal clock until the next transmit data is written.

[8] Read the ACKB bit to confirm that ACKB is 0. When the slave device has not returned an acknowledge signal and ACKB remains 1, execute the transmit end processing described in step [12] and perfrom transmit operation again.

[9] Write the next data to be transmitted in ICDR. To indicate the end of data transfer, clear the IRIC flag to 0.

As described in step [6] above, writing to ICDR and clearing of the IRIC flag must be executed continuously so that no interrupt is inserted.

The next frame is transmitted in synchronization with the internal clock.

[10] When one frame of data has been transmitted, the IRIC flag is set to 1 at the rise of the 9th transmit clock pulse. After one frame has been transmitted, SCL is automatically fixed low in synchronization with the internal clock until the next transmit data is written.

[11] Read the ACKB bit of ICSR. Confirm that the slave device has returned an acknowledge signal and ACKB is 0. When more data is to be transmitted, return to step [9] to execute next transmit operation. If the slave device has not returned an acknowledge signal and ACKB is 1, execute the transmit end processing described in step [12].

[12] Clear the IRIC flag to 0. Write BBSY and SCP of ICCR to 0. By doing so, SDA is changed from low to high while SCL is high and the transmit stop condition is generated.

[3] The IRIC flag is set to 1 at the fall of the 8th clock of a one-frame reception clock. At this point, if the IEIC bit of ICCR is set to 1, an interrupt request is generated to the CPU.

SCL is automatically fixed low in synchronization with the internal clock until the IRIC flag is cleared. If the first frame is the final reception frame, execute the end processing as described in [10].

[4] Clear the IRIC flag to 0 to release from the wait state.

The master device outputs the 9th receive clock pulse, sets SDA to low, and returns an acknowledge signal.

[5] When one frame of data has been transmitted, the IRIC and IRTR flags are set to 1 at the rise of the 9th transmit clock pulse.

The master device continues to output the receive clock for the next receive data.

[6] Read the ICDR receive data.

[7] Clear the IRIC flag to indicate the next wait.

From clearing of the IRIC flag to completion of data reception as described in steps [5], [6], and [7], must be performed within the time taken to transfer one byte because releasing of the wait state as described in step [4] (or [9]).

[8] The IRIC flag is set to 1 at the fall of the 8th receive clock pulse. SCL is automatically fixed low in synchronization with the internal clock until the IRIC flag is cleared. If this frame is the final reception frame, execute the end processing as described in [10].

[9] Clear the IRIC flag to 0 to release from the wait state. The master device outputs the 9th reception clock pulse, sets SDA to low, and returns an acknowledge signal.

By repeating steps [5] to [9] above, more data can be received.

[10] Set the ACKB bit of ICSR to 1 and set the acknowledge data for the final reception.

Set the TRS bit of ICCR to 1 to change receive mode to transmit mode.

[11] Clear the IRIC flag to release from the wait state.

[12] When one frame of data has been received, the IRIC flag is set to 1 at the rise of the 9th reception clock pulse.

[13] Clear the WAIT bit of ICMR to 0 to cancel wait mode. Read the ICDR receive data and clear the IRIC flag to 0.

Clear the IRIC flag only when WAIT = 0.

(If the stop-condition generation command is executed after clearing the IRIC flag to 0 and

Differences between Boot Mode and User Program Mode

	Boot Mode	User Program Mode
Entire memory erase	Yes	Yes
Block erase	No	Yes
Programming control program*	Program/program-verify	Erase/erase-verify Program/program-verify

Note: * To be provided by the user, in accordance with the recommended algorithm.

Block Configuration: The flash memory is divided into two 32-kbyte blocks, two 8-kbyte blocks, one 16-kbyte block, one 28-kbyte block, and four 1-kbyte blocks.

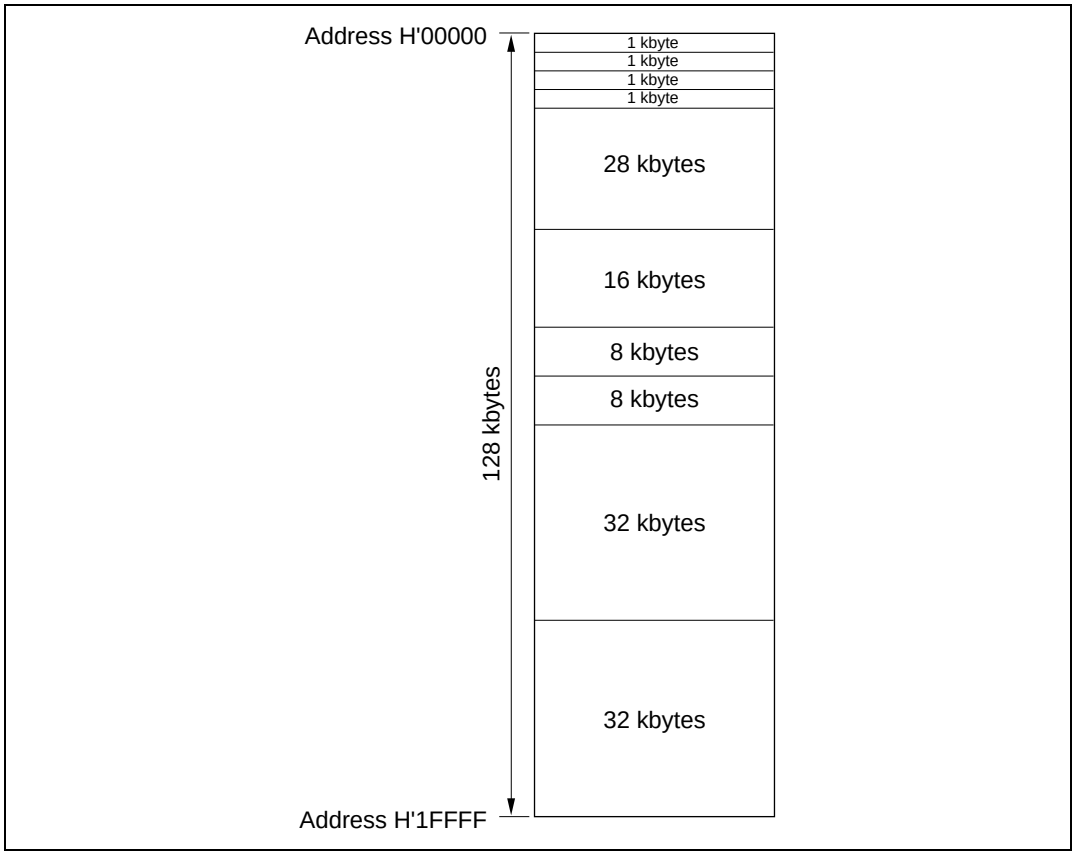
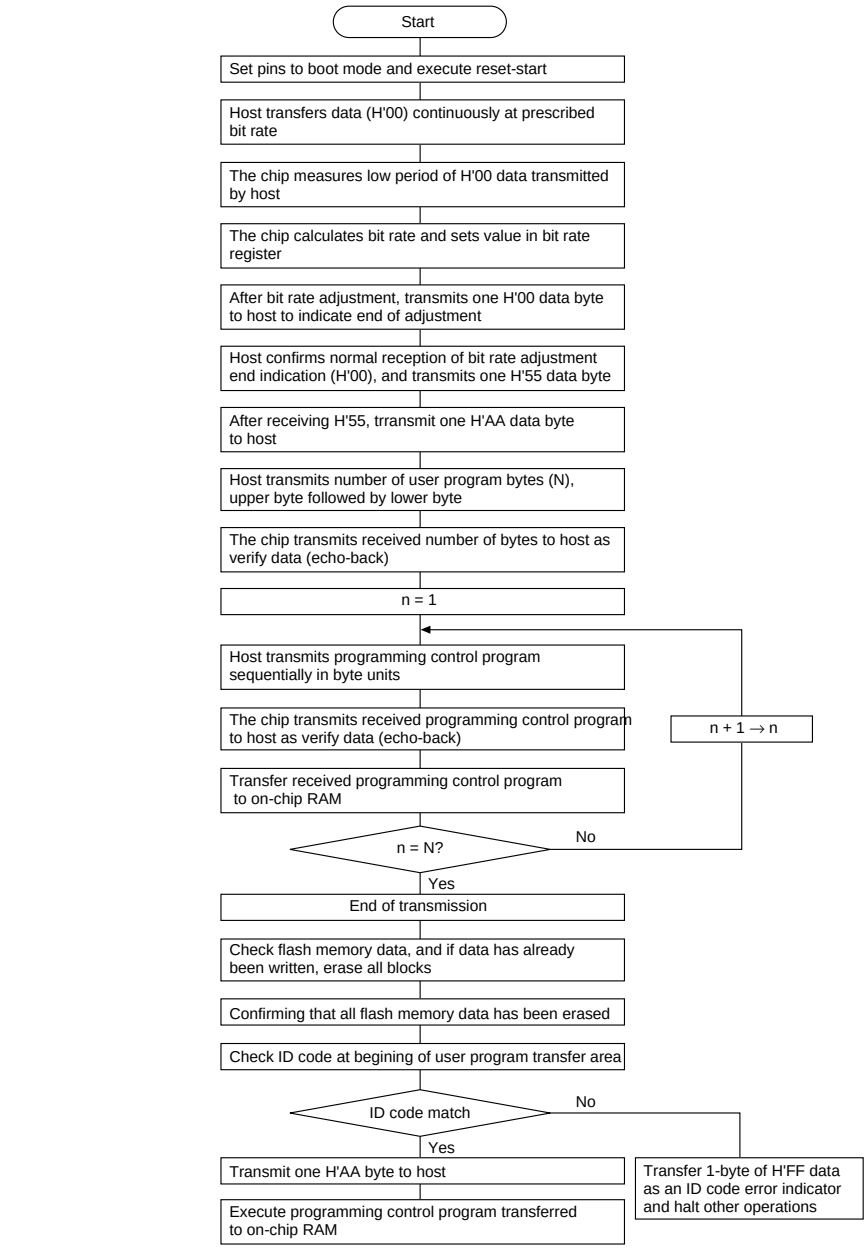


Figure 22.6 Flash Memory Block Configuration



Note: If a memory cell does not operate normally and cannot be erased, one H'FF byte is transmitted as an erase error, and the erase operation and subsequent operations are halted.

Figure 22.8 Boot Mode Execution Procedure

25.5.6 Flash Memory Characteristics

Table 25.49 shows the flash memory characteristics.

Table 25.49 Flash Memory Characteristics (Programming/Erasing Operating Range)

Conditions (5-V version): V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0 V, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

(3-V version): V_{CC} = 3.0 V to 3.6 V, V_{SS} = 0 V, T_a = –20 to +75°C

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Programming time*1 *2 *4		tP	—	10	200	ms/ 128 bytes	
Erase time*1 *3 *6		tE	—	100	1200	ms/block	
Reprogramming count		N_{WEC}	100*8	10000*9	—	Times	
Data retention time*10		t_{DRP}	10	—	—	Years	
Programming	Wait time after SWE-bit setting*1	x	1	—	—	µs	
	Wait time after PSU-bit setting*1	y	50	—	—	µs	
	Wait time after P-bit setting*1 *4	z1	28	30	32	µs	1 ≤ n ≤ 6
		z2	198	200	202	µs	7 ≤ n ≤ 1000
		z3	8	10	12	µs	Additional writing
	Wait time after P-bit clear*1	α	5	—	—	µs	
	Wait time after PSU-bit clear*1	β	5	—	—	µs	
	Wait time after PV-bit setting*1	γ	4	—	—	µs	
	Wait time after dummy write*1	ε	2	—	—	µs	
	Wait time after PV-bit clear*1	η	4	—	—	µs	
	Wait time after SWE-bit clear*1	θ	100	—	—	µs	
	Maximum programming count*1 *4 *5	N	—	—	1000	Times	
Erase	Wait time after SWE-bit setting*1	x	1	—	—	µs	
	Wait time after ESU-bit setting*1	y	100	—	—	µs	
	Wait time after E-bit setting*1 *6	z	10	—	100	ms	
	Wait time after E-bit clear*1	α	10	—	—	µs	
	Wait time after ESU-bit clear*1	β	10	—	—	µs	
	Wait time after EV-bit setting*1	γ	20	—	—	µs	
	Wait time after dummy write*1	ε	2	—	—	µs	
	Wait time after EV-bit clear*1	η	4	—	—	µs	
	Wait time after SWE-bit clear*1	θ	100	—	—	µs	
	Maximum erase count*1 *6 *7	N	—	—	120	Times	

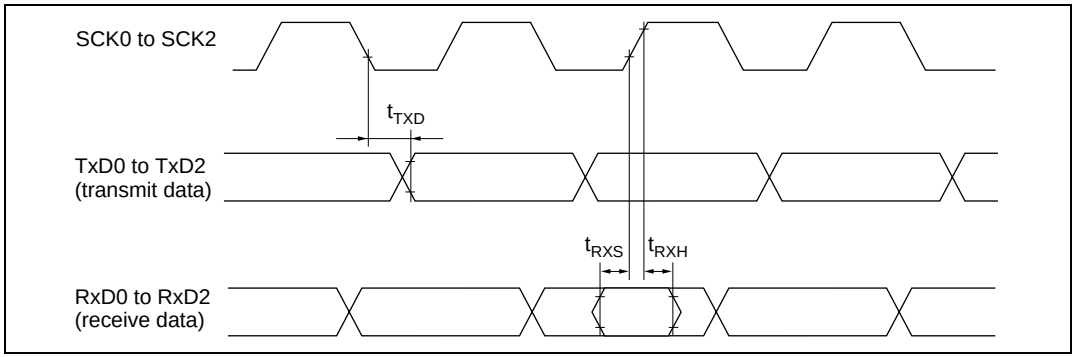


Figure 25.23 SCI Input/Output Timing (Synchronous Mode)

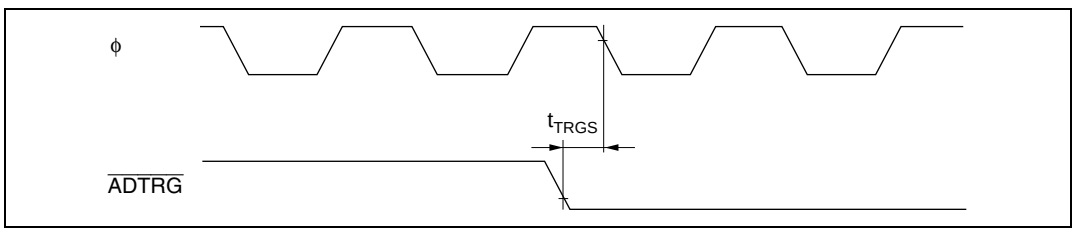


Figure 25.24 A/D Converter External Trigger Input Timing

Instruction	Mnemonic	Size	Instruction Format															
			1st Byte		2nd Byte		3rd Byte		4th Byte		5th Byte	6th Byte	7th Byte	8th Byte	9th Byte	10th Byte
LDC	LDC @aa:32,CCR	W	0	1	4	0	6	B	2	0	abs					
	LDC @aa:32,EXR	W	0	1	4	1	6	B	2	0	abs					
LDM*3	LDM.L @SP+, (ERn-ERn+1)	L	0	1	1	0	6	D	7	0 ern+1						
	LDM.L @SP+, (ERn-ERn+2)	L	0	1	2	0	6	D	7	0 ern+2						
	LDM.L @SP+, (ERn-ERn+3)	L	0	1	3	0	6	D	7	0 ern+3						
LDMAC	LDMAC ERs,MACH	L	Cannot be used with the H8S/2138 Group and H8S/2134 Group.													
	LDMAC ERs,MACL	L														
MAC	MAC @ERn+,@ERm+	—														
MOV	MOV.B #xx:8,Rd	B	F	rd	IMM											
	MOV.B Rs,Rd	B	0	C	rs	rd										
	MOV.B @ERs,Rd	B	6	8	0 ers	rd										
	MOV.B @(d:16,ERs),Rd	B	6	E	0 ers	rd	disp									
	MOV.B @(d:32,ERs),Rd	B	7	8	0 ers	0	6	A	2	rd	disp					
	MOV.B @ERs+,Rd	B	6	C	0 ers	rd										
	MOV.B @aa:8,Rd	B	2	rd	abs											
	MOV.B @aa:16,Rd	B	6	A	0	rd	abs									
	MOV.B @aa:32,Rd	B	6	A	2	rd	abs									
	MOV.B Rs,@ERd	B	6	8	1 erd	rs										
	MOV.B Rs,@(d:16,ERd)	B	6	E	1 erd	rs	disp									
	MOV.B Rs,@(d:32,ERd)	B	7	8	0 erd	0	6	A	A	rs	disp					
	MOV.B Rs,@-ERd	B	6	C	1 erd	rs										
	MOV.B Rs,@aa:8	B	3	rs	abs											
	MOV.B Rs,@aa:16	B	6	A	8	rs	abs									
	MOV.B Rs,@aa:32	B	6	A	A	rs	abs									
	MOV.W #xx:16,Rd	W	7	9	0	rd	IMM									
	MOV.W Rs,Rd	W	0	D	rs	rd										
	MOV.W @ERs,Rd	W	6	9	0 ers	rd										
	MOV.W @(d:16,ERs),Rd	W	6	F	0 ers	rd	disp									
	MOV.W @(d:32,ERs),Rd	W	7	8	0 ers	0	6	B	2	rd	disp					

STR1—Status Register 1 **H'FFF6** **HIF**
STR2—Status Register 2 **H'FFFE** **HIF**

Bit	7	6	5	4	3	2	1	0
	DBU	DBU	DBU	DBU	C/$\overline{D}$	DBU	IBF	OBF
Initial value	0	0	0	0	0	0	0	0
Slave R/W	R/W	R/W	R/W	R/W	R	R/W	R	R/(W)
Host R/W	R	R	R	R	R	R	R	R

User-defined bits

Output data register full

0	[Clearing condition] When the host processor reads ODR or the slave writes 0 in the OBF bit
1	[Setting condition] When the slave processor writes to ODR

Input data register full

0	[Clearing condition] When the slave processor reads IDR
1	[Setting condition] When the host processor writes to IDR

Command/data

0	Contents of input data register (IDR) are data
1	Contents of input data register (IDR) are a command

DADR0—D/A Data Register 0 **H'FFF8** **D/A Converter**
DADR1—D/A Data Register 1 **H'FFF9** **D/A Converter**

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores data for D/A conversion

C.9 Port 9 Block Diagrams

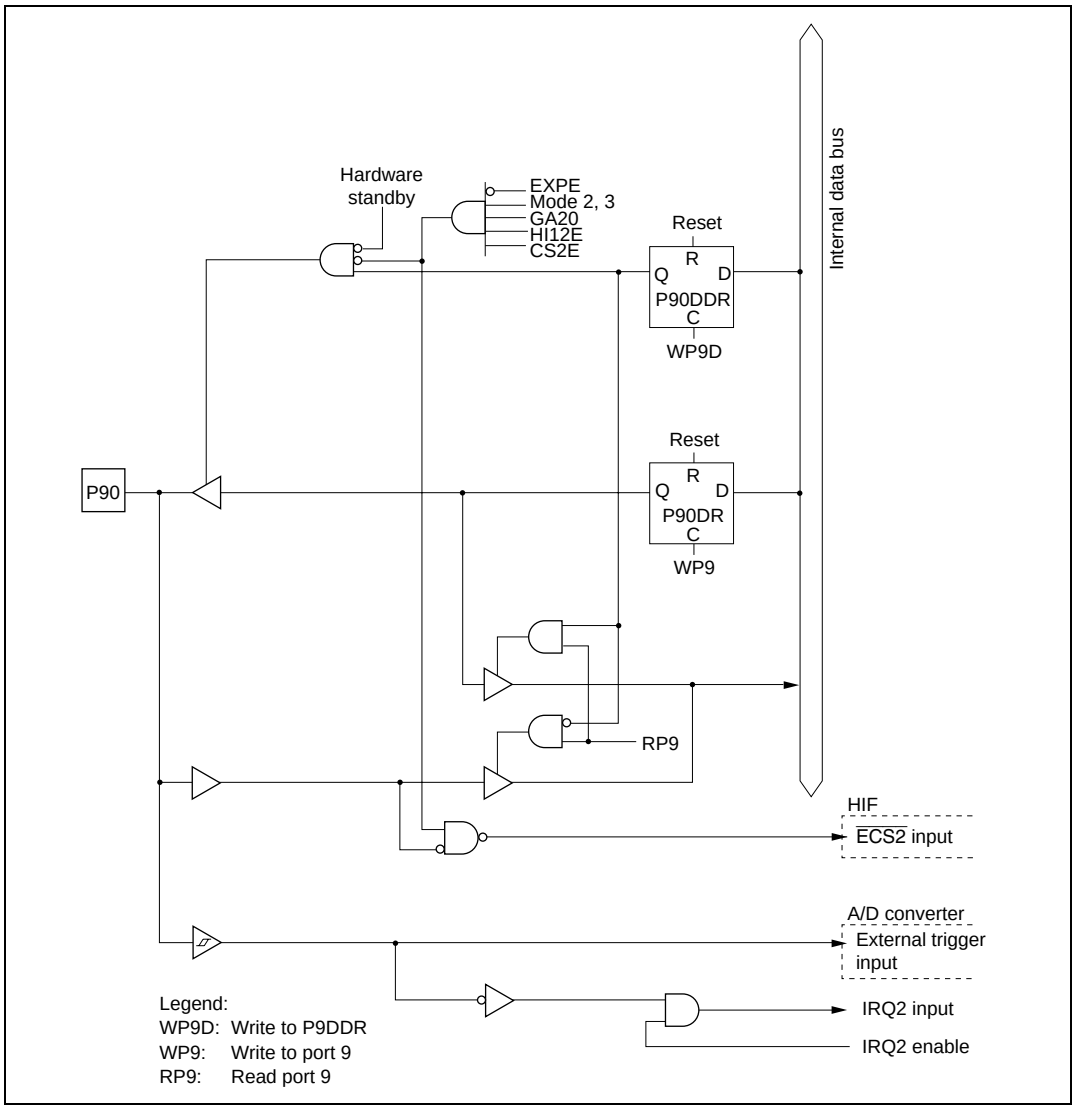


Figure C.29 Port 9 Block Diagram (Pin P90)

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