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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	IrDA, SCI
Peripherals	POR, PWM, WDT
Number of I/O	57
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2132rtf20v

Section 8 I/O Ports

Section 9 8-Bit PWM Timers [H8S/2138 Group]

Section 10 14-Bit PWM D/A

Stack Structure: In advanced mode, when the program counter (PC) is pushed onto the stack in a subroutine call, and the PC and condition-code register (CCR) are pushed onto the stack in exception handling, they are stored as shown in figure 2.5. The extended control register (EXR) is not pushed onto the stack. For details, see section 4, Exception Handling.

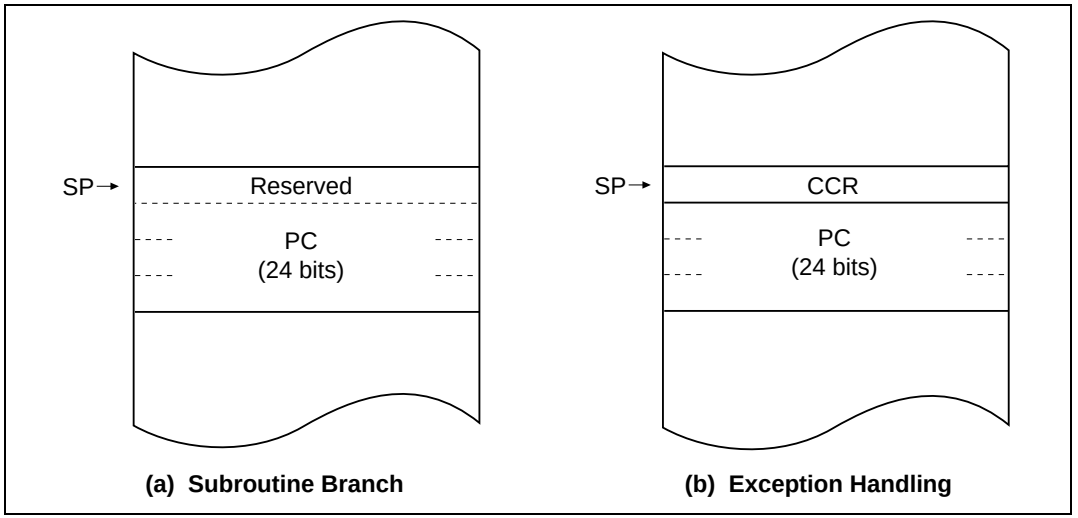


Figure 2.5 Stack Structure in Advanced Mode

Interrupt Source	Origin of Interrupt Source	Vector Number	Vector Address: Normal Mode	Vector Address: Advanced Mode	ICR	Priority
CMIA0 (compare-match A)	8-bit timer	64	H'0080	H'000100	ICRB3	High
CMIB0 (compare-match B)	channel 0	65	H'0082	H'000104		
OVI0 (overflow)		66	H'0084	H'000108		
Reserved		67	H'0086	H'00010C		
CMIA1 (compare-match A)	8-bit timer	68	H'0088	H'000110	ICRB2	
CMIB1 (compare-match B)	channel 1	69	H'008A	H'000114		
OVI1 (overflow)		70	H'008C	H'000118		
Reserved		71	H'008E	H'00011C		
CMIAY (compare-match A)	8-bit timer	72	H'0090	H'000120	ICRB1	
CMIBY (compare-match B)	channels	73	H'0092	H'000124		
OVIY (overflow)	Y, X	74	H'0094	H'000128		
ICIX (input capture X)		75	H'0096	H'00012C		
IBF1 (IDR1 reception completed)	Host	76	H'0098	H'000130	ICRB0	
IBF2 (IDR2 reception completed)	interface	77	H'009A	H'000134		
Reserved		78	H'009C	H'000138		
Reserved		79	H'009E	H'00013C		
ERI0 (receive error 0)	SCI	80	H'00A0	H'000140	ICRC7	
RXI0 (reception completed 0)	channel 0	81	H'00A2	H'000144		
TXI0 (transmit data empty 0)		82	H'00A4	H'000148		
TEI0 (transmission end 0)		83	H'00A6	H'00014C		
ERI1 (receive error 1)	SCI	84	H'00A8	H'000150	ICRC6	
RXI1 (reception completed 1)	channel 1	85	H'00AA	H'000154		
TXI1 (transmit data empty 1)		86	H'00AC	H'000158		
TEI1 (transmission end 1)		87	H'00AE	H'00015C		
ERI2 (receive error 2)	SCI	88	H'00B0	H'000160	ICRC5	
RXI2 (reception completed 2)	channel 2	89	H'00B2	H'000164		
TXI2 (transmit data empty 2)		90	H'00B4	H'000168		
TEI2 (transmission end 2)		91	H'00B6	H'00016C		
IICI0 (1-byte transmission/ reception completed)	IIC channel 0	92	H'00B8	H'000170	ICRC4	
DDCSWI (format switch)	(option)	93	H'00BA	H'000174		
IICI1 (1-byte transmission/ reception completed)	IIC channel 1	94	H'00BC	H'000178	ICRC3	
Reserved	(option)	95	H'00BE	H'00017C		
Reserved	—	96 to 103	H'00C0 to H'00CE	H'000180 to H'00019C		Low

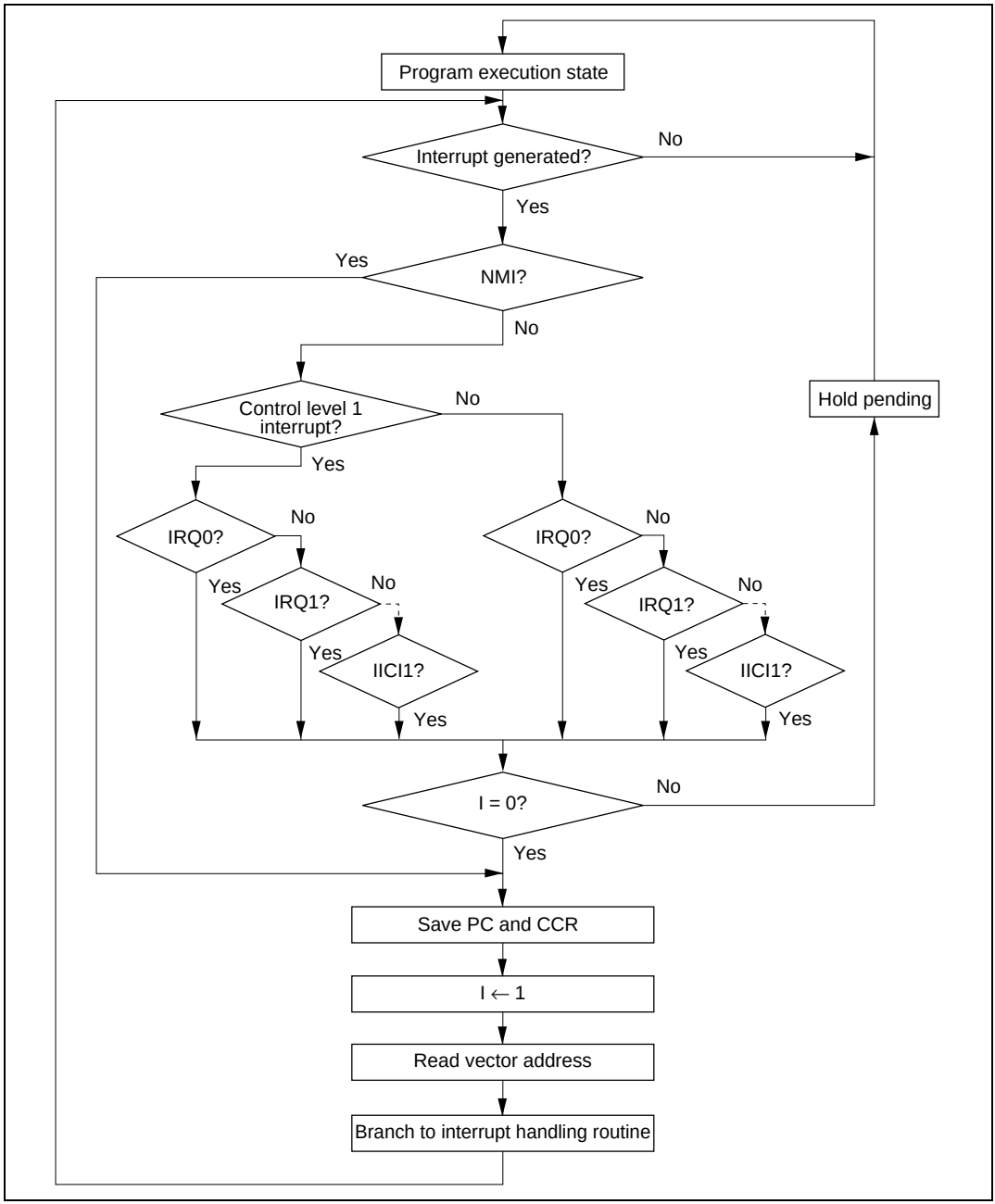


Figure 5.8 Flowchart of Procedure Up to Interrupt Acceptance in Interrupt Control Mode 0

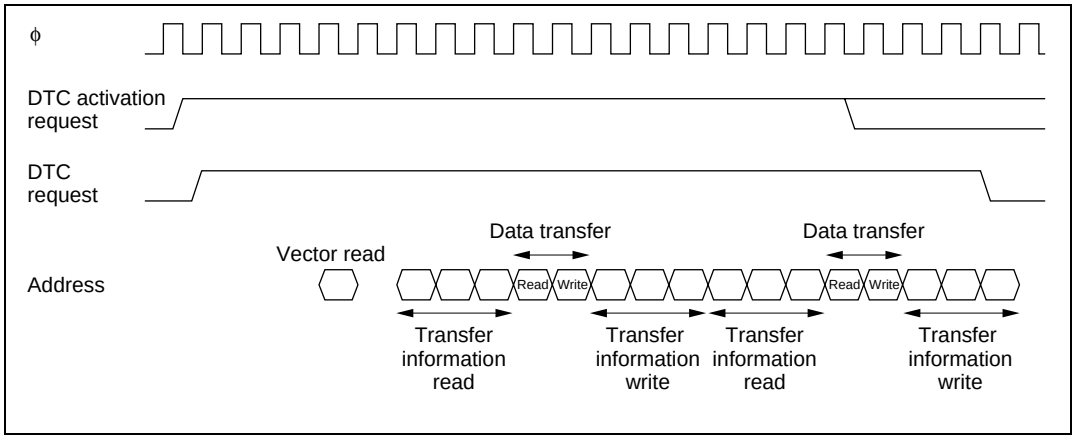


Figure 7.12 DTC Operation Timing (Chain Transfer)

7.3.10 Number of DTC Execution States

Table 7.8 lists execution phases for a single DTC data transfer, and table 7.9 shows the number of states required for each execution phase.

Table 7.8 DTC Execution Phases

Mode	Vector Read I	Register Information Read/Write J	Data Read K	Data Write L	Internal Operation M
Normal	1	6	1	1	3
Repeat	1	6	1	1	3
Block transfer	1	6	N	N	3

N: Block size (initial setting of CRAH and CRAL)

8.4 Port 3

8.4.1 Overview

Port 3 is an 8-bit I/O port. Port 3 pins also function as host data bus I/O pins (HDB7 to HDB0) (H8S/2138 Group only), and as data bus I/O pins. Port 3 functions change according to the operating mode. Port 3 has an on-chip MOS input pull-up function that can be controlled by software.

Figure 8.9 shows the port 3 pin configuration.

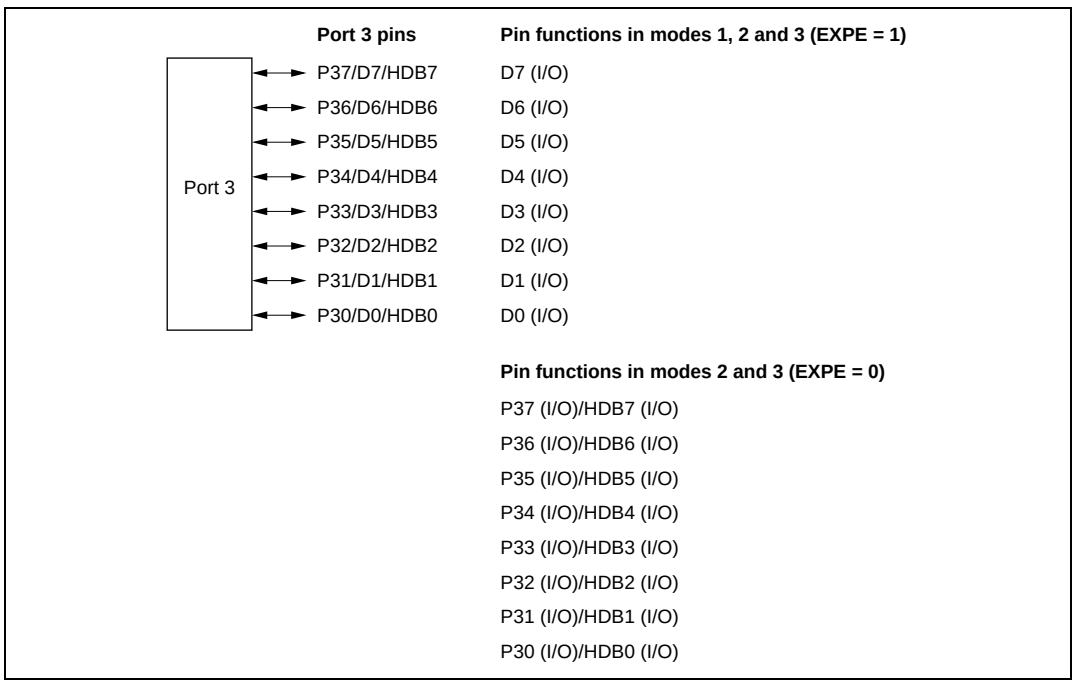
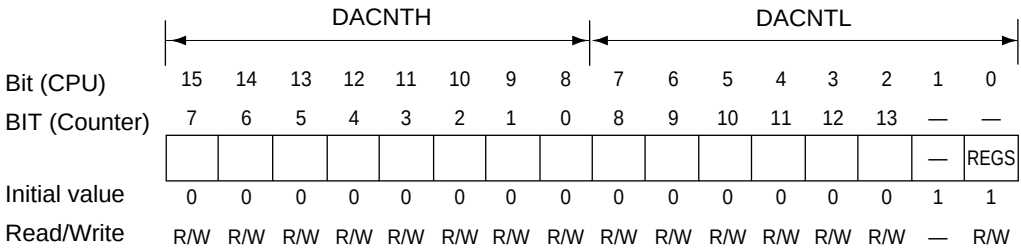


Figure 8.9 Port 3 Pin Functions

10.2 Register Descriptions

10.2.1 PWM D/A Counter (DACNT)



DACNT is a 14-bit readable/writable up-counter that increments on an input clock pulse. The input clock is selected by the clock select bit (CKS) in DACR. The CPU can read and write the DACNT value, but since DACNT is a 16-bit register, data transfers between it and the CPU are performed using a temporary register (TEMP). See section 10.3, Bus Master Interface, for details.

DACNT functions as the time base for both PWM D/A channels. When a channel operates with 14-bit precision, it uses all DACNT bits. When a channel operates with 12-bit precision, it uses the lower 12 (counter) bits and ignores the upper two (counter) bits.

DACNT is initialized to H'0003 by a reset, in the standby modes, watch mode, subactive mode, subsleep mode, and module stop mode, and by the PWME bit.

Bit 1 of DACNTL (CPU) is not used, and is always read as 1.

DACNTL Bit 0—Register Select (REGS): DADRA and DACR, and DADRB and DACNT, are located at the same addresses. The REGS bit specifies which registers can be accessed. The REGS bit can be accessed regardless of whether DADRB or DACNT is selected.

Bit 0

REGS	Description	
0	DADRA and DADRB can be accessed	
1	DACR and DACNT can be accessed	(Initial value)

TCSR0

Bit 4—A/D Trigger Enable (ADTE): Enables or disables A/D converter start requests by compare-match A.

Bit 4

ADTE	Description	
0	A/D converter start requests by compare-match A are disabled	(Initial value)
1	A/D converter start requests by compare-match A are enabled	

TCSR1

Bit 4—Reserved: This bit cannot be modified and is always read as 1.

TCSRX

Bit 4—Input Capture Flag (ICF): Status flag that indicates detection of a rising edge followed by a falling edge in the external reset signal after the ICST bit in TCONRI has been set to 1.

Bit 4

ICF	Description	
0	[Clearing condition] Read ICF when ICF = 1, then write 0 in ICF	(Initial value)
1	[Setting condition] When a rising edge followed by a falling edge is detected in the external reset signal after the ICST bit in TCONRI has been set to 1	

TCSRY

Bit 4—Input Capture Interrupt Enable (ICIE): Selects enabling or disabling of the interrupt request by ICF (ICIX) when the ICF bit in TCSRX is set to 1.

Bit 4

ICIE	Description	
0	Interrupt request by ICF (ICIX) is disabled	(Initial value)
1	Interrupt request by ICF (ICIX) is enabled	

13.1.3 Input and Output Pins

Table 13.1 lists the timer connection input and output pins.

Table 13.1 Timer Connection Input and Output Pins

Name	Abbreviation	Input/ Output	Function
Vertical synchronization signal input pin	VSYNCI	Input	Vertical synchronization signal input pin or FTIA input pin/TMIY input pin
Horizontal synchronization signal input pin	HSYNCI	Input	Horizontal synchronization signal input pin or TMCI1 input pin
Composite synchronization signal input pin	CSYNCI	Input	Composite synchronization signal input pin or TMRI1 input pin
Spare vertical synchronization signal input pin	VFBACKI	Input	Spare vertical synchronization signal input pin or FTIB input pin
Spare horizontal synchronization signal input pin	HFBACKI	Input	Spare horizontal synchronization signal input pin or FTCI input pin/TMIX input pin
Vertical synchronization signal output pin	VSYNCO	Output	Vertical synchronization signal output pin or FTOA output pin
Horizontal synchronization signal output pin	HSYNCO	Output	Horizontal synchronization signal output pin or TMO1 output pin
Clamp waveform output pin	CLAMPO	Output	Clamp waveform output pin or FTIC input pin
Blanking waveform output pin	CBLANK	Output	Blanking waveform output pin

Bit 2

TEIE	Description	
0	Transmit-end interrupt (TEI) request disabled*	(Initial value)
1	Transmit-end interrupt (TEI) request enabled*	

Note: * TEI cancellation can be performed by reading 1 from the TDRE flag in SSR, then clearing it to 0 and clearing the TEND flag to 0, or clearing the TEIE bit to 0.

Bits 1 and 0—Clock Enable 1 and 0 (CKE1, CKE0): These bits are used to select the SCI clock source and enable or disable clock output from the SCK pin. The combination of the CKE1 and CKE0 bits determines whether the SCK pin functions as an I/O port, the serial clock output pin, or the serial clock input pin.

The setting of the CKE0 bit, however, is only valid for internal clock operation (CKE1 = 0) in asynchronous mode. The CKE0 bit setting is invalid in synchronous mode, and in the case of external clock operation (CKE1 = 1). The setting of bits CKE1 and CKE0 must be carried out before the SCI's operating mode is determined using SMR.

For details of clock source selection, see table 15.9 in section 15.3, Operation.

Bit 1	Bit 0		
CKE1	CKE0	Description	
0	0	Asynchronous mode	Internal clock/SCK pin functions as I/O port*1
		Synchronous mode	Internal clock/SCK pin functions as serial clock output*1
	1	Asynchronous mode	Internal clock/SCK pin functions as clock output*2
		Synchronous mode	Internal clock/SCK pin functions as serial clock output
1	0	Asynchronous mode	External clock/SCK pin functions as clock input*3
		Synchronous mode	External clock/SCK pin functions as serial clock input
	1	Asynchronous mode	External clock/SCK pin functions as clock input*3
		Synchronous mode	External clock/SCK pin functions as serial clock input

Notes: 1. Initial value
2. Outputs a clock of the same frequency as the bit rate.
3. Inputs a clock with a frequency 16 times the bit rate.

Bit 5	Bit 4		
MST	**TRS**	**Operating Mode**	
0	0	Slave receive mode	(Initial value)
	1	Slave transmit mode	
1	0	Master receive mode	
	1	Master transmit mode	

Bit 5

MST	Description
0	Slave mode (Initial value) [Clearing conditions] 1. When 0 is written by software 2. When bus arbitration is lost after transmission is started in I²C bus format master mode
1	Master mode [Setting conditions] 1. When 1 is written by software (in cases other than clearing condition 2) 2. When 1 is written in MST after reading MST = 0 (in case of clearing condition 2)

Bit 4

TRS	Description
0	Receive mode (Initial value) [Clearing conditions] 1. When 0 is written by software (in cases other than setting condition 3) 2. When 0 is written in TRS after reading TRS = 1 (in case of clearing condition 3) 3. When bus arbitration is lost after transmission is started in I²C bus format master mode 4. When the SW bit in DDCSWR changes from 1 to 0
1	Transmit mode [Setting conditions] 1. When 1 is written by software (in cases other than clearing conditions 3 and 4) 2. When 1 is written in TRS after reading TRS = 0 (in case of clearing conditions 3 and 4) 3. When a 1 is received as the R/$\overline{W}$ bit of the first frame in I²C bus format slave mode

16.2.9 Module Stop Control Register (MSTPCR)

	MSTPCRH								MSTPCRL							
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	MSTP15	MSTP14	MSTP13	MSTP12	MSTP11	MSTP10	MSTP9	MSTP8	MSTP7	MSTP6	MSTP5	MSTP4	MSTP3	MSTP2	MSTP1	MSTP0
Initial value	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MSTPCR comprises two 8-bit readable/writable registers, and is used to perform module stop mode control.

When the MSTP4 or MSTP3 bit is set to 1, operation of the corresponding IIC channel is halted at the end of the bus cycle, and a transition is made to module stop mode. For details, see section 24.5, Module Stop Mode.

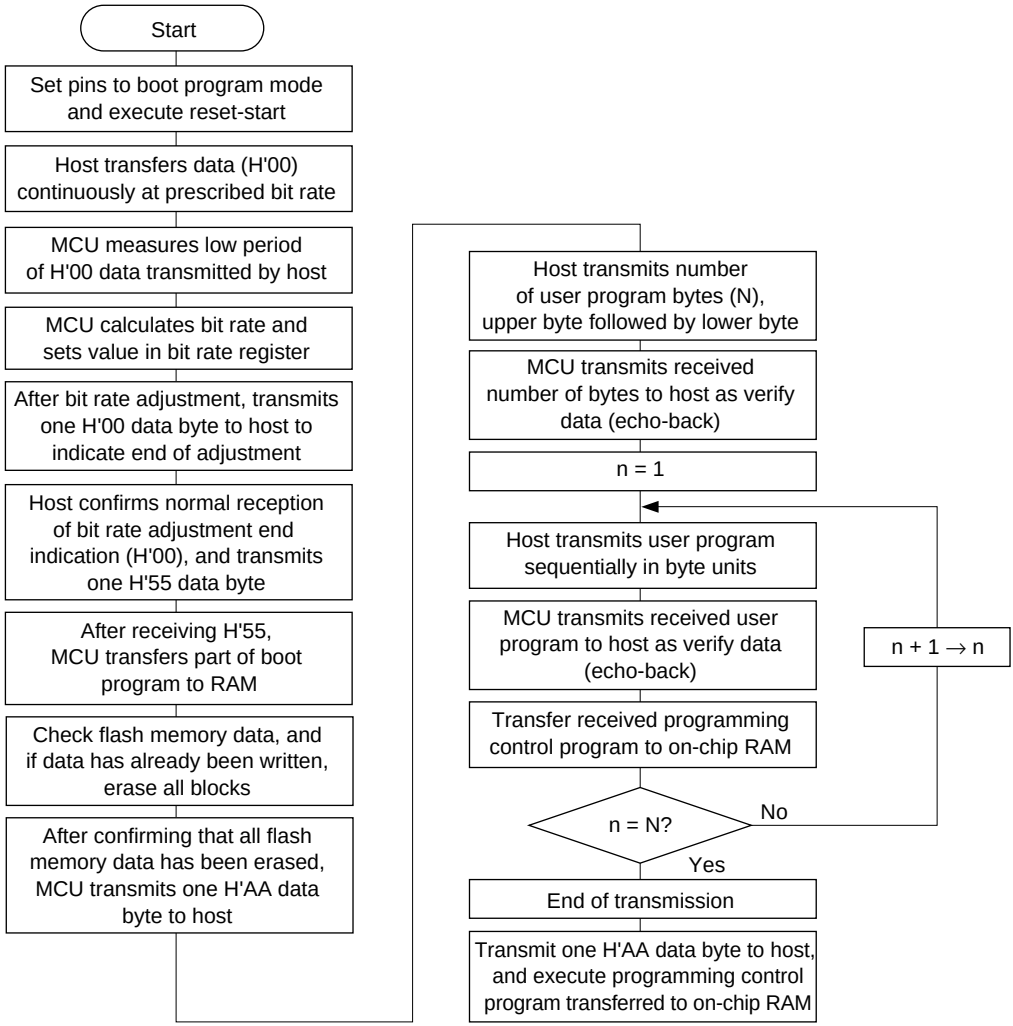
MSTPCR is initialized to H'3FFF by a reset and in hardware standby mode. It is not initialized in software standby mode.

MSTPCRL Bit 4—Module Stop (MSTP4): Specifies IIC channel 0 module stop mode.

MSTPCRL Bit 4		
MSTP4	**Description**	
0	IIC channel 0 module stop mode is cleared	
1	IIC channel 0 module stop mode is set	(Initial value)

MSTPCRL Bit 3—Module Stop (MSTP3): Specifies IIC channel 1 module stop mode.

MSTPCRL Bit 3		
MSTP3	**Description**	
0	IIC channel 1 module stop mode is cleared	
1	IIC channel 1 module stop mode is set	(Initial value)



Note: If a memory cell does not operate normally and cannot be erased, one H'FF byte is transmitted as an erase error, and the erase operation and subsequent operations are halted.

Figure 21.8 Boot Mode Execution Procedure

21.6.2 User Program Mode

When set to user program mode, the chip can program and erase its flash memory by executing a user program/erase control program. Therefore, on-board reprogramming of the on-chip flash memory can be carried out by providing on-board supply of programming data, and storing a program/erase control program in part of the program area as necessary.

To select user program mode, select a mode that enables the on-chip flash memory (mode 2 or 3). In this mode, on-chip supporting modules other than flash memory operate as they normally would in mode 2 and 3.

The flash memory itself cannot be read while the SWE bit is set to 1 to perform programming or erasing, so the control program that performs programming and erasing should be run in on-chip RAM or external memory.

Figure 21.11 shows the procedure for executing the program/erase control program when transferred to on-chip RAM.

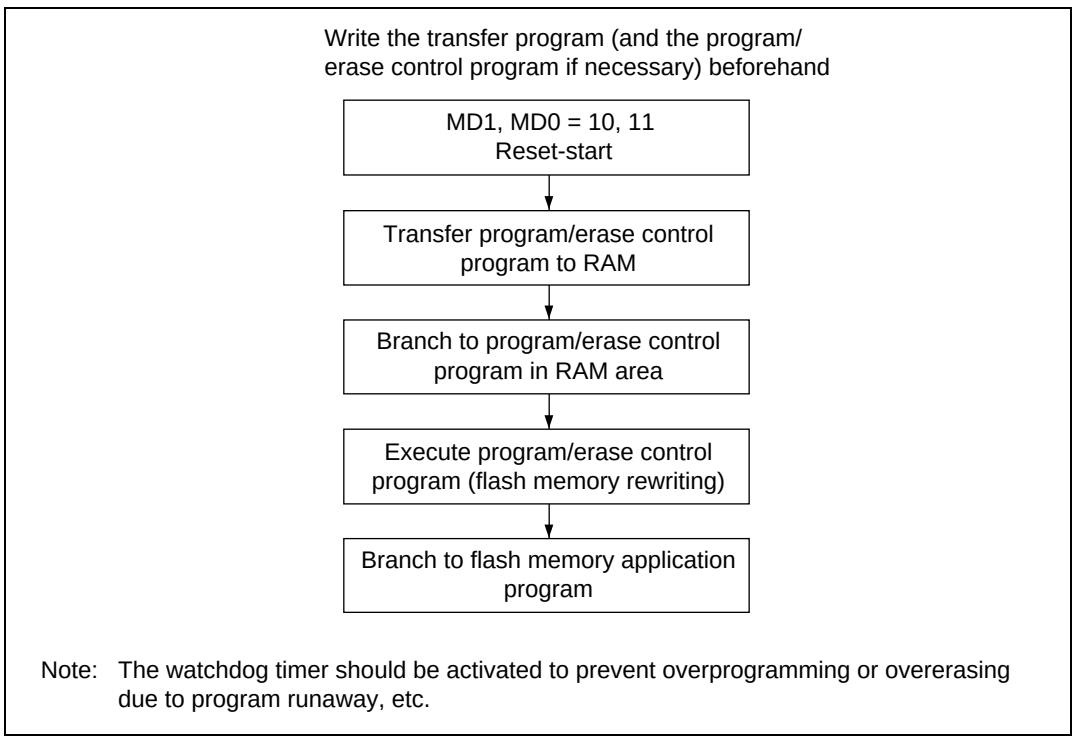


Figure 21.11 User Program Mode Execution Procedure

22.5 Register Descriptions

22.5.1 Flash Memory Control Register 1 (FLMCR1)

Bit	7	6	5	4	3	2	1	0
	FWE	SWE	—	—	EV	PV	E	P
Initial value	1	0	0	0	0	0	0	0
Read/Write	R	R/W	—	—	R/W	R/W	R/W	R/W

FLMCR1 is an 8-bit register used for flash memory operating mode control. Program-verify mode or erase-verify mode is entered by setting SWE to 1. Program mode is entered by setting SWE to 1, then setting the PSU bit in FLMCR2, and finally setting the P bit. Erase mode is entered by setting SWE to 1, then setting the ESU bit in FLMCR2, and finally setting the E bit. FLMCR1 is initialized to H'80 by a reset, and in hardware standby mode, software standby mode, subactive mode, subsleep mode, and watch mode. When on-chip flash memory is disabled, a read will return H'00, and writes are invalid.

Writes to the EV and PV bits in FLMCR1 are enabled only when SWE=1; writes to the E bit only when SWE = 1, and ESU = 1; and writes to the P bit only when SWE = 1, and PSU = 1.

Bit 7—Flash Write Enable (FWE): Sets hardware protection against flash memory programming/erasing. This bit cannot be modified and is always read as 1.

Bit 6—Software Write Enable (SWE): Enables or disables flash memory programming. SWE should be set before setting bits ESU, PSU, EV, PV, E, P, and EB7 to EB0, and should not be cleared at the same time as these bits.

Bit 6		
SWE	**Description**	
0	Writes disabled	(Initial value)
1	Writes enabled	

Bit 5 and 4—Reserved: These bits cannot be modified and are always read as 0.

25.2 Electrical Characteristics of H8S/2138 F-ZTAT

25.2.1 Absolute Maximum Ratings

Table 25.2 lists the absolute maximum ratings.

Table 25.2 Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power supply voltage*	V_{CC}	–0.3 to +7.0	V
Input voltage (except ports 6 and 7)	V_{in}	–0.3 to V_{CC} +0.3	V
Input voltage (CIN input not selected for port 6)	V_{in}	–0.3 to V_{CC} +0.3	V
Input voltage (CIN input selected for port 6)	V_{in}	Lower voltage of –0.3 to V_{CC} +0.3 and AV_{CC} +0.3	V
Input voltage (port 7)	V_{in}	–0.3 to AV_{CC} +0.3	V
Analog power supply voltage	AV_{CC}	–0.3 to +7.0	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} +0.3	V
Operating temperature	T_{opr}	Regular specifications: –20 to +75	°C
		Wide-range specifications: –40 to +85	°C
Operating temperature (flash memory programming/erasing)	T_{opr}	Regular specifications: 0 to +75	°C
		Wide-range specifications: 0 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution: Permanent damage to the chip may result if absolute maximum ratings are exceeded.

* Voltage applied to the VCC1 and VCC2 pins.

Mnemonic		Size	Addressing Mode and Instruction Length (Bytes)									Operation	Condition Code						No. of States*1	
			#xx	Rn	@ERn	@(d,ERn)	@-ERn/@ERn+	@aa	@(d,PC)	@@aa	—		I	H	N	Z	V	C	Normal	Advanced
MAC	MAC @ERn+,@ERm+	Cannot be used with the H8S/2138 Group and H8S/2134 Group.																	[2]	
CLRMAC	CLRMAC																			
LDMAC	LDMAC ERs,MACH																			
	LDMAC ERs,MACL																			
STMAC	STMAC MACH,ERd																			
	STMAC MACL,ERd																			

Instruction	Mnemonic	Instruction Fetch I	Branch Address Read J	Stack Operation K	Byte Data Access L	Word Data Access M	Internal Operation N
SHLL	SHLL.B Rd	1					
	SHLL.B #2,Rd	1					
	SHLL.W Rd	1					
	SHLL.W #2,Rd	1					
	SHLL.L ERd	1					
	SHLL.L #2,ERd	1					
SHLR	SHLR.B Rd	1					
	SHLR.B #2,Rd	1					
	SHLR.W Rd	1					
	SHLR.W #2,Rd	1					
	SHLR.L ERd	1					
	SHLR.L #2,ERd	1					
SLEEP	SLEEP	1					1
STC	STC.B CCR,Rd	1					
	STC.B EXR,Rd	1					
	STC.W CCR,@ERd	2				1	
	STC.W EXR,@ERd	2				1	
	STC.W CCR,@(d:16,ERd)	3				1	
	STC.W EXR,@(d:16,ERd)	3				1	
	STC.W CCR,@(d:32,ERd)	5				1	
	STC.W EXR,@(d:32,ERd)	5				1	
	STC.W CCR,@-ERd	2				1	1
	STC.W EXR,@-ERd	2				1	1
	STC.W CCR,@aa:16	3				1	
	STC.W EXR,@aa:16	3				1	
	STC.W CCR,@aa:32	4				1	
	STC.W EXR,@aa:32	4				1	
STM*4	STM.L (ERn-ERn+1),@-SP	2		4			1
	STM.L (ERn-ERn+2),@-SP	2		6			1
	STM.L (ERn-ERn+3),@-SP	2		8			1
SUB	SUB.B Rs,Rd	1					
	SUB.W #xx:16,Rd	2					
	SUB.W Rs,Rd	1					
	SUB.L #xx:32,ERd	3					
	SUB.L ERs,ERd	1					