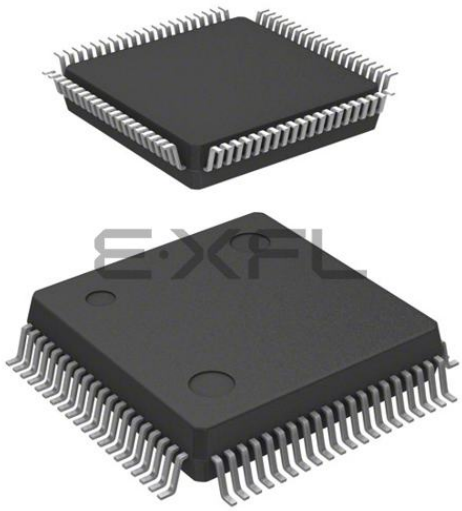

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	IrDA, SCI
Peripherals	POR, PWM, WDT
Number of I/O	58
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2134afa20v

Item	Page	Revision (See Manual for Details)
25.3.2 DC Characteristics Table 25.16 DC Characteristics (3)	740	Table 25.16 (3) amended

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Output high voltage	All output pins (except P97, and P52[*4])[*5]	V_{OH}	V_{CC} –0.5	—	—	V	I_{OH} = –200 µA
			V_{CC} –1.0	—	—	V	I_{OH} = –1 mA
	P97, P52[*4]		0.5	—	—	V	I_{OH} = –200 µA, V_{CC} = 2.7 to 3.5 V

	742	Note *4 amended Note: 4. P52/SCK0/SCL0 and P97/SDA0 are NMOS push-pull outputs in H8S/2138. ... P52/SCK0 and P97 (ICE = 0) high levels are driven by NMOS in H8S/2138.
25.3.6 Flash Memory Characteristics Table 25.27 Flash Memory Characteristics (Programming/Erasing Operating Range)	756	Table 25.27 amended

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Reprogramming count	N_{WEC}	100[*8]	10000[*9]	—	Times	
Data retention time[*10]	t_{DRP}	10	—	—	Years	

	757	Notes 8 to 10 added Notes: 8. Minimum number of times for which all characteristics are guaranteed after rewriting (Guarantee range is 1 to minimum value). 9. Reference value for 25C° (as a guide line, rewriting should normally function up to this value). 10. Data retention characteristics when rewriting is performed within the specification range, including the minimum value.
25.4.2 DC Characteristics Table 25.29 DC Characteristics (1)	761	Table 25.29 (1) amended

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Three-state leakage current (off state)	Ports 1 to 6, 8, 9	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0.5 to V_{CC} –0.5 V
Input pull-up MOS current	Ports 1 to 3	$-I_P$	50	—	300	µA	V_{in} = 0 V, V_{CC} = 5 V ±10%
	Port 6		60	—	500	µA	

Table 25.29 DC Characteristics (3)	766	Note *5 added to test conditions for input pull-up MOS current V_{in} = 0 V, V_{CC} = 2.7 V[*5] to 3.6 V
25.5.2 DC Characteristics Table 25.40 DC Characteristics (1)	782	Table 25.40 (1) amended

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input pull-up MOS current	Ports 1 to 3	$-I_P$	30	—	300	µA	V_{in} = 0 V, V_{CC} = 5 V ±10%
	Port 6		60	—	600	µA	

2.5 Data Formats

The CPU can process 1-bit, 4-bit (BCD), 8-bit (byte), 16-bit (word), and 32-bit (longword) data. Bit-manipulation instructions operate on 1-bit data by accessing bit n (n = 0, 1, 2, …, 7) of byte operand data. The DAA and DAS decimal-adjust instructions treat byte data as two digits of 4-bit BCD data.

2.5.1 General Register Data Formats

Figure 2.10 shows the data formats in general registers.

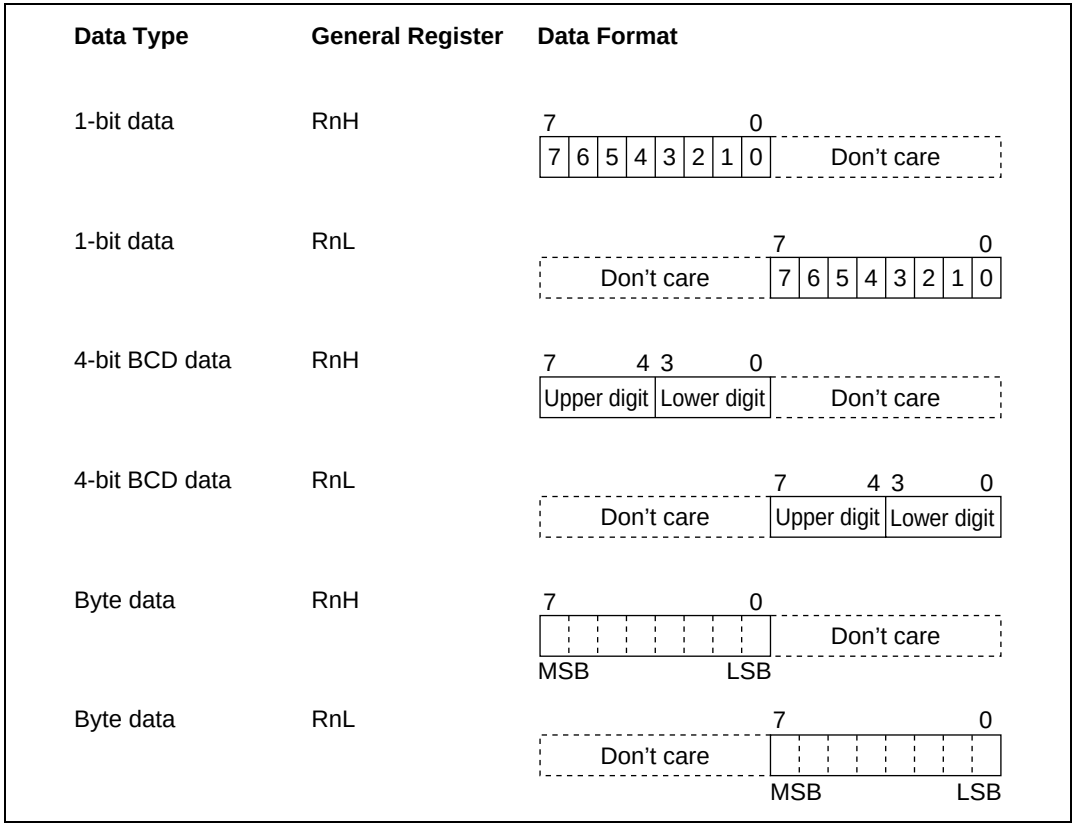
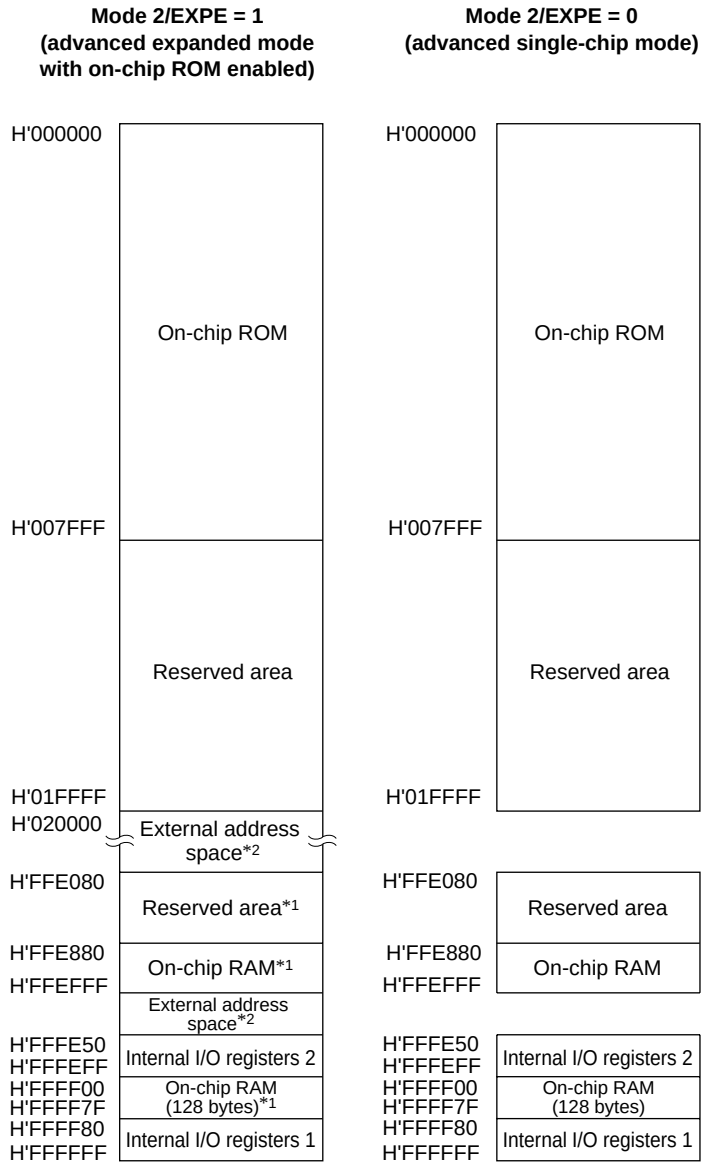


Figure 2.10 General Register Data Formats



Notes: 1. External addresses can be accessed by clearing the RAME bit in SYSCR to 0.
2. For these models, the maximum number of external address pins is 16. An external address can only be specified correctly for an area that uses the I/O strobe function.

Figure 3.5 H8S/2130 Memory Map in Each Operating Mode (cont)

5.7.3 Operation

The interrupt controller has three main functions in DTC control.

Selection of Interrupt Source: It is possible to select DTC activation request or CPU interrupt request with the DTCE bit of DTCERA to DTCERE in the DTC.

After a DTC data transfer, the DTCE bit can be cleared to 0 and an interrupt request sent to the CPU in accordance with the specification of the DISEL bit of MRB in the DTC.

When the DTC performs the specified number of data transfers and the transfer counter reaches 0, following the DTC data transfer the DTCE bit is cleared to 0 and an interrupt request is sent to the CPU.

Determination of Priority: The DTC activation source is selected in accordance with the default priority order, and is not affected by mask or priority levels. See section 7.3.3, DTC Vector Table, for the respective priorities.

Operation Order: If the same interrupt is selected as a DTC activation source and a CPU interrupt source, the DTC data transfer is performed first, followed by CPU interrupt exception handling.

Table 5.10 summarizes interrupt source selection and interrupt source clearance control according to the settings of the DTCE bit of DTCERA to DTCERE in the DTC and the DISEL bit of MRB in the DTC.

Table 5.10 Interrupt Source Selection and Clearing Control

Settings			
DTC		Interrupt Source Selection/Clearing Control	
DTCE	DISEL	DTC	CPU
0	*	×	Δ
1	0	Δ	×
	1	O	Δ

Legend:

Δ: The relevant interrupt is used. Interrupt source clearing is performed.
(The CPU should clear the source flag in the interrupt handling routine.)

O: The relevant interrupt is used. The interrupt source is not cleared.

×: The relevant bit cannot be used.

*: Don't care

11.3.5 Timing of Input Capture Flag (ICF) Setting

The input capture flag ICFx (x = A, B, C, D) is set to 1 by the internal input capture signal. The FRC value is simultaneously transferred to the corresponding input capture register (ICRx). Figure 11.11 shows the timing of this operation.

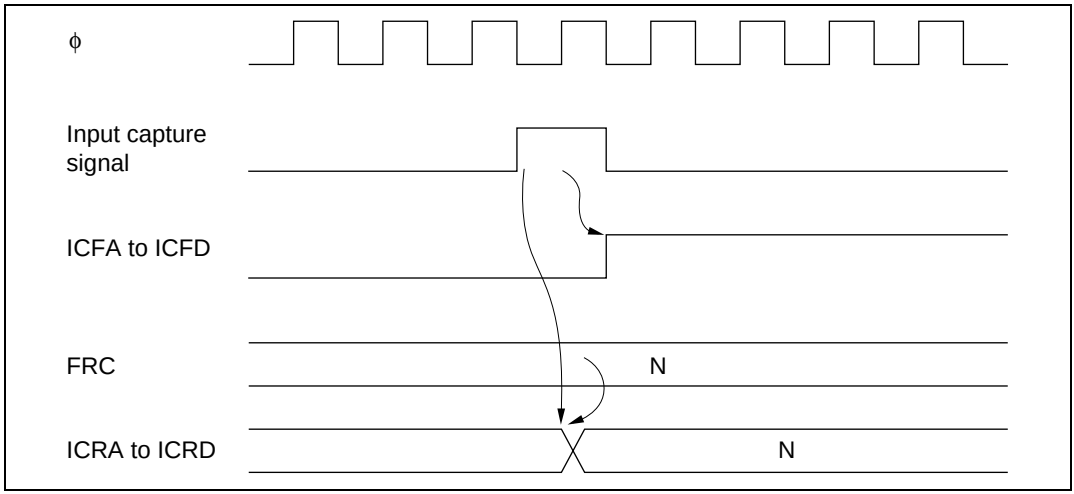


Figure 11.11 Setting of Input Capture Flag (ICFA to ICFD)

Contention between FRC Write and Increment: If an FRC increment pulse is generated during the state after an FRC write cycle, the write takes priority and FRC is not incremented.

Figure 11.19 shows this type of contention.

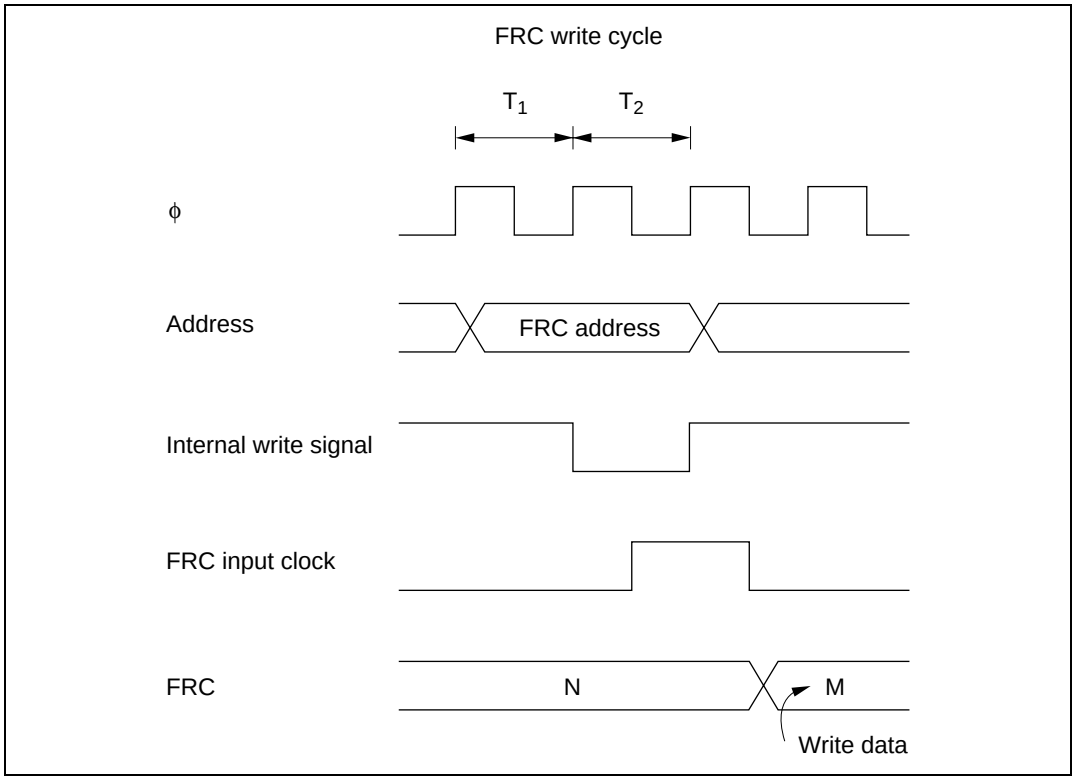


Figure 11.19 FRC Write-Increment Contention

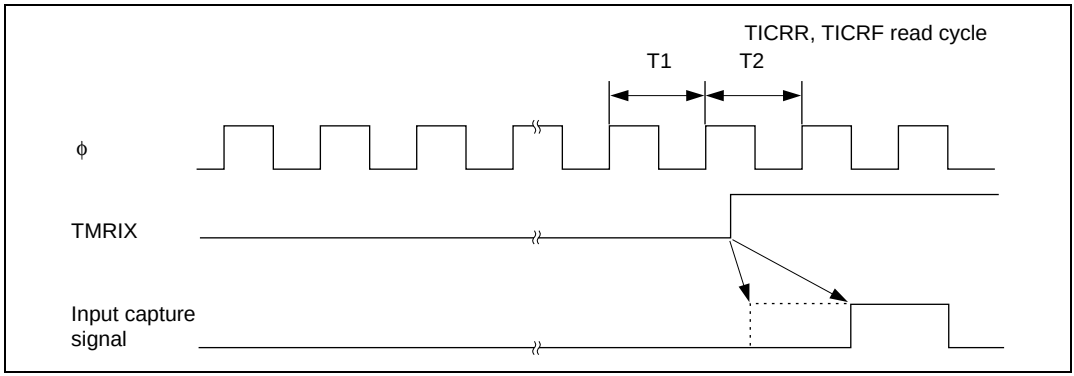


Figure 12.10 Timing of Input Capture Signal (When Input Capture Input Signal Enters while TICRR and TICRF Are Being Read)

(2) Input capture signal input selection

Input capture input signal (TMRIX) in TMRX is switched by setting bits in the TCONRI register.

Figure 12.11 and table 12.3 show the input capture signal selections.

See section 13.2.1, Timer Connection Register I (TCONRI), for details.

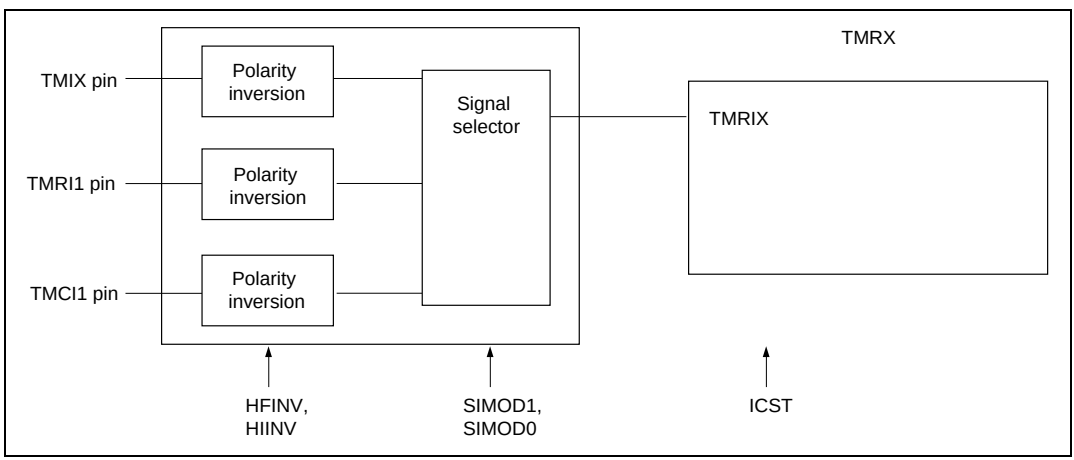


Figure 12.11 Switching of Input Capture Signal

Table 15.11 Receive Errors and Conditions for Occurrence

Receive Error	Abbreviation	Occurrence Condition	Data Transfer
Overrun error	ORER	When the next data reception is completed while the RDRF flag in SSR is set to 1	Receive data is not transferred from RSR to RDR
Framing error	FER	When the stop bit is 0	Receive data is transferred from RSR to RDR
Parity error	PER	When the received data differs from the parity (even or odd) set in SMR	Receive data is transferred from RSR to RDR

Figure 15.8 shows an example of the operation for reception in asynchronous mode.

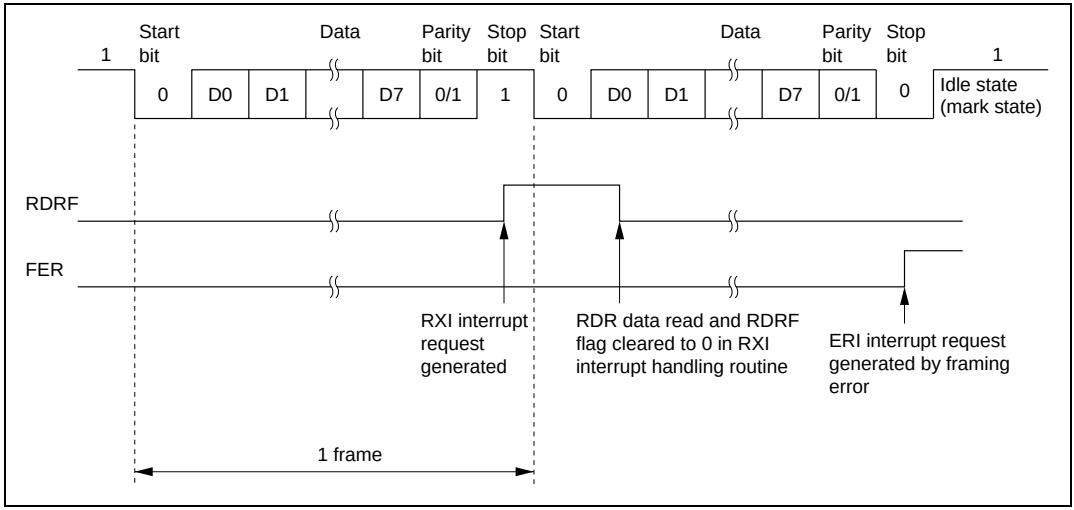


Figure 15.8 Example of SCI Operation in Reception (Example with 8-Bit Data, Parity, One Stop Bit)

Bit 7

ICE	Description
0	I²C bus interface module disabled, with SCL and SDA signal pins set to port function (Initial value)
	Internal state initialization of I²C bus interface module
	SAR and SARX can be accessed
1	I²C bus interface module enabled for transfer operations (pins SCL and SCA are driving the bus)
	ICMR and ICDR can be accessed

Bit 6—I²C Bus Interface Interrupt Enable (IEIC): Enables or disables interrupts from the I²C bus interface to the CPU.

Bit 6

IEIC	Description
0	Interrupts disabled (Initial value)
1	Interrupts enabled

Bit 5—Master/Slave Select (MST)

Bit 4—Transmit/Receive Select (TRS)

MST selects whether the I²C bus interface operates in master mode or slave mode.

TRS selects whether the I²C bus interface operates in transmit mode or receive mode.

In master mode with the I²C bus format, when arbitration is lost, MST and TRS are both reset by hardware, causing a transition to slave receive mode. In slave receive mode with the addressing format (FS = 0 or FSX = 0), hardware automatically selects transmit or receive mode according to the R/$\overline{W}$ bit in the first frame after a start condition.

Modification of the TRS bit during transfer is deferred until transfer of the frame containing the acknowledge bit is completed, and the changeover is made after completion of the transfer.

MST and TRS select the operating mode as follows.

Table 16.8 I²C Bus Timing (with Maximum Influence of t_{Sr}/t_{Sf})

			Time Indication (at Maximum Transfer Rate) [ns]						
Item	t_{cyc} Indication		t_{Sr}/t_{Sf} Influence (Max.)	I²C Bus Specification (Min.)	ϕ = 5 MHz	ϕ = 8 MHz	ϕ = 10 MHz	ϕ = 16 MHz	ϕ = 20 MHz
t_{SCLHO}	$0.5t_{SCLO}$ $(-t_{Sr})$	Standard mode	–1000	4000	4000	4000	4000	4000	4000
		High-speed mode	–300	600	950	950	950	950	950
t_{SCLLO}	$0.5t_{SCLO}$ $(-t_{Sr})$	Standard mode	–250	4700	4750	4750	4750	4750	4750
		High-speed mode	–250	1300	1000*1	1000*1	1000*1	1000*1	1000*1
t_{BUFO}	$0.5t_{SCLO} - 1t_{cyc}$ $(-t_{Sr})$	Standard mode	–1000	4700	3800*1	3875*1	3900*1	3938*1	3950*1
		High-speed mode	–300	1300	750*1	825*1	850*1	888*1	900*1
t_{STAHO}	$0.5t_{SCLO} - 1t_{cyc}$ $(-t_{Sr})$	Standard mode	–250	4000	4550	4625	4650	4688	4700
		High-speed mode	–250	600	800	875	900	938	950
t_{STASO}	$1t_{SCLO}$ $(-t_{Sr})$	Standard mode	–1000	4700	9000	9000	9000	9000	9000
		High-speed mode	–300	600	2200	2200	2200	2200	2200
t_{STOSO}	$0.5t_{SCLO} + 2t_{cyc}$ $(-t_{Sr})$	Standard mode	–1000	4000	4400	4250	4200	4125	4100
		High-speed mode	–300	600	1350	1200	1150	1075	1050
t_{SDASO} (master)	$1t_{SCLLO}$ *3 $- 3t_{cyc}$ $(-t_{Sr})$	Standard mode	–1000	250	3100	3325	3400	3513	3550
		High-speed mode	–300	100	400	625	700	813	850
t_{SDASO} (slave)	$1t_{SCLL}$ *3 $- 12t_{cyc}$ *2 $(-t_{Sr})$	Standard mode	–1000	250	1300	2200	2500	2950	3100
		High-speed mode	–300	100	–1400*1	–500*1	–200*1	250	400

Section 17 Host Interface [H8S/2138 Group]

Provided in the H8S/2138 Group; not provided in the H8S/2134 Group.

17.1 Overview

The H8S/2138 Group has an on-chip host interface (HIF) that enables connection to an ISA bus, widely used as the internal bus in personal computers. The host interface provides a dual-channel parallel interface between the on-chip CPU and a host processor. The host interface is available only when the HI12E bit is set to 1 in SYSCR2. This mode is called slave mode, because it is designed for a master-slave communication system in which the H8S/2138 Group chip is slaved to a host processor.

17.1.1 Features

The features of the host interface are summarized below.

The host interface consists of 4-byte data registers, 2-byte status registers, a 1-byte control register, fast A20 gate logic, and a host interrupt request circuit. Communication is carried out via five control signals from the host processor ($\overline{CS1}$, $\overline{CS2}$ or $\overline{ECS2}$, HA0, $\overline{IOR}$, and $\overline{IOW}$), four output signals to the host processor (GA20, HIRQ1, HIRQ11, and HIRQ12), and an 8-bit bidirectional command/data bus (HDB7 to HDB0). The $\overline{CS1}$ and $\overline{CS2}$ (or $\overline{ECS2}$) signals select one of the two interface channels.

functions of these pins (input block) are similarly fixed internally. As a result, the host interface I/O pins (HDB7 to HDB0) also go to the high-impedance state.

This state is maintained while the HIFSD pin is low, and when the HIFSD pin returns to the high-level state, the pins are restored to their normal operation as host interface pins.

Table 17.9 shows the scope of HIF pin shutdown in slave mode.

Table 17.9 Scope of HIF Pin Shutdown in Slave Mode

Abbreviation	Port	Scope of Shutdown in Slave Mode	I/O	Selection Conditions
$\overline{\text{IOR}}$	P93	O	Input	Slave mode
$\overline{\text{IOW}}$	P94	O	Input	Slave mode
$\overline{\text{CS1}}$	P95	O	Input	Slave mode
$\overline{\text{CS2}}$	P81	Δ	Input	Slave mode and CS2E = 1 and FGA20E = 0
$\overline{\text{ECS2}}$	P90	Δ	Input	Slave mode and CS2E = 1 and FGA20E = 1
HA0	P80	O	Input	Slave mode
HDB7 to HDB0	P37 to P30	O	I/O	Slave mode
HIRQ11	P43	Δ	Output	Slave mode and CS2E = 1 and P43DDR = 1
HIRQ1	P44	Δ	Output	Slave mode and P44DDR = 1
HIRQ12	P45	Δ	Output	Slave mode and P45DDR = 1
GA20	P81	Δ	Output	Slave mode and FGA20E = 1
HIFSD	P82	—	Input	Slave mode and SDE = 1

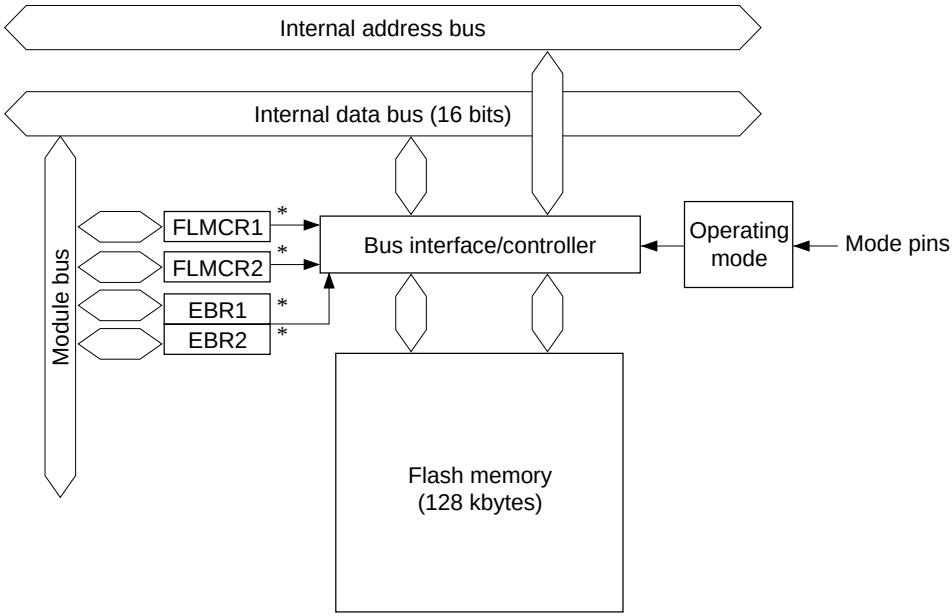
Notes: Slave mode: Single-chip mode and HI12E = 1

O: Pins shut down by shutdown function
The $\overline{\text{IRQ2}}$/$\overline{\text{ADTRG}}$ input signal is also fixed in the case of P90 shutdown, the TMCI1/HSYNCI signal in the case of P43 shutdown, and the TMRI/CSYNCI in the case of P45 shutdown.

Δ: Pins shut down only when the HIF function is selected by means of a register setting

—: Pin not shut down

22.4.2 Block Diagram



Legend:
FLMCR1: Flash memory control register 1
FLMCR2: Flash memory control register 2
EBR1: Erase block register 1
EBR2: Erase block register 2

Note: * These registers are used only in the flash memory version. In the mask ROM version, a read at any of these addresses will return an undefined value, and writes are invalid.

Figure 22.2 Block Diagram of Flash Memory

Automatic SCI Bit Rate Adjustment

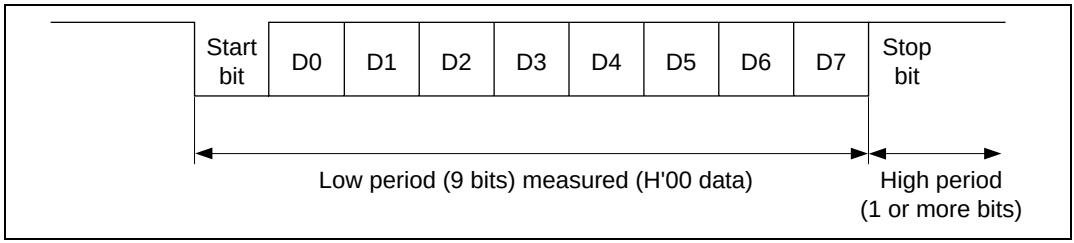


Figure 22.9 Automatic SCI Bit Rate Adjustment

When boot mode is initiated, the chip measures the low period of the asynchronous SCI communication data (H'00) transmitted continuously from the host. The SCI transmit/receive format should be set as follows: 8-bit data, 1 stop bit, no parity. The chip calculates the bit rate of the transmission from the host from the measured low period, and transmits one H'00 byte to the host to indicate the end of bit rate adjustment. The host should confirm that this adjustment end indication (H'00) has been received normally, and transmit one H'55 byte to the chip. If reception cannot be performed normally, initiate boot mode again (reset), and repeat the above operations. Depending on the host's transmission bit rate and the chip's system clock frequency, there will be a discrepancy between the bit rates of the host and the chip. To ensure correct SCI operation, the host's transfer bit rate should be set to (4800, 9600, or 19200) bps.

Table 22.7 shows typical host transfer bit rates and system clock frequencies for which automatic adjustment of the chip's bit rate is possible. The boot program should be executed within this system clock range.

Table 22.7 System Clock Frequencies for which Automatic Adjustment of the Chip's Bit Rate Is Possible

Host Bit Rate	System Clock Frequency for which Automatic Adjustment of Bit Rate Is Possible
19200 bps	8 MHz to 20 MHz
9600 bps	4 MHz to 20 MHz
4800 bps	2 MHz to 18 MHz

On-Chip RAM Area Divisions in Boot Mode: In boot mode, the 1920-byte area from H'(FF)E880 to H'(FF) EFFF and the 128-byte area from H'(FF)FF00 to H'(FF)FF7F is reserved for use by the boot program, as shown in figure 22.10. The area to which the programming control program is transferred is H'(FF)E080 to H'(FF)E87F (2048 bytes). However, the 8-byte area from H'(FF)E080 to H'(FF)E087 is reserved for ID codes as shown in figure 22.10. The boot program

23.3 Oscillator

Clock pulses can be supplied by connecting a crystal resonator, or by input of an external clock.

23.3.1 Connecting a Crystal Resonator

Circuit Configuration: A crystal resonator can be connected as shown in the example in figure 23.2. Select the damping resistance R_d according to table 23.2. An AT-cut parallel-resonance crystal should be used.

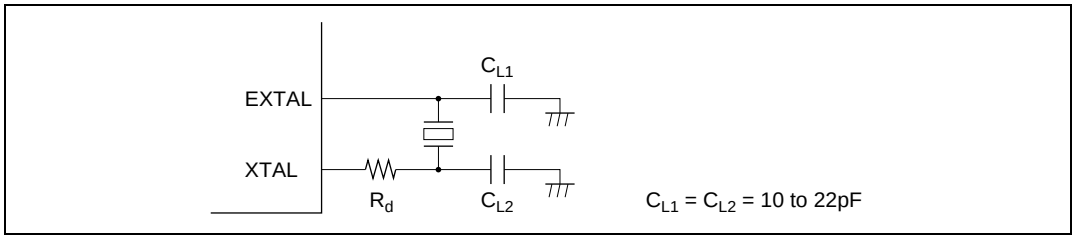


Figure 23.2 Connection of Crystal Resonator (Example)

Table 23.2 Damping Resistance Value

Frequency (MHz)	2	4	8	10	12	16	20
R_d (Ω)	1k	500	200	0	0	0	0

Crystal resonator: Figure 23.3 shows the equivalent circuit of the crystal resonator. Use a crystal resonator that has the characteristics shown in table 23.3 and the same frequency as the system clock (ϕ).

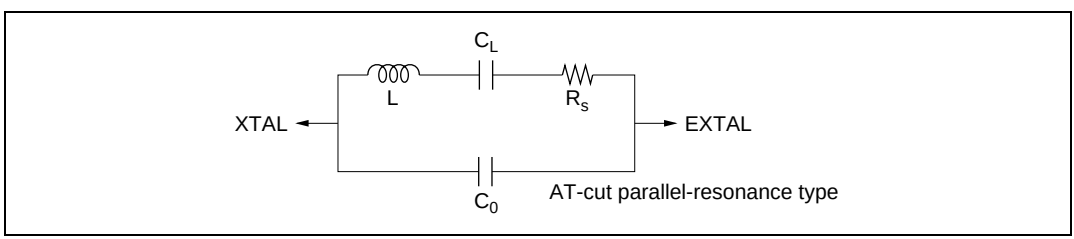


Figure 23.3 Crystal Resonator Equivalent Circuit

Bit 5—Noise Elimination Sampling Frequency Select (NESEL): Selects the frequency at which the subclock (ϕSUB) input from the EXCL pin is sampled with the clock (ϕ) generated by the system clock oscillator. When ϕ = 5 MHz or higher, clear this bit to 0.

Bit 5

NESEL	Description	
0	Sampling at ϕ divided by 32	(Initial value)
1	Sampling at ϕ divided by 4	

Bit 4—Subclock Input Enable (EXCLE): Controls subclock input from the EXCL pin.

Bit 4

EXCLE	Description	
0	Subclock input from EXCL pin is disabled	(Initial value)
1	Subclock input from EXCL pin is enabled	

Bits 3 to 0—Reserved: These bits cannot be modified and are always read as 0.

24.2.3 Timer Control/Status Register (TCSR)

TCSR1

Bit	7	6	5	4	3	2	1	0
	OVF	WT/$\overline{IT}$	TME	PSS	RST/$\overline{NMI}$	CKS2	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Only 0 can be written in bit 7, to clear the flag.

TCSR1 is an 8-bit readable/writable register that performs selection of the WDT1 TCNT input clock, mode, etc.

Only bit 4 is described here. For details of the other bits, see section 14.2.2, Timer Control/Status Register (TCSR).

TCSR is initialized to H'00 by a reset and in hardware standby mode. It is not initialized in software standby mode.

DDCSWR—DDC Switch Register H'FEE6 IIC0

Bit	7	6	5	4	3	2	1	0
	SWE	SW	IE	IF	CLR3	CLR2	CLR1	CLR0
Initial value	0	0	0	0	1	1	1	1
Read/Write	R/W	R/W	R/W	R/(W)*1	W*2	W*2	W*2	W*2

IIC clear bits

Bit 3	Bit 2	Bit 1	Bit 0	Description
CLR3	CLR2	CLR1	CLR0	
0	0	—	—	Setting prohibited
	1	0	0	Setting prohibited
			1	IIC0 internal latch cleared
		1	0	IIC1 internal latch cleared
			1	IIC0 and IIC1 internal latches cleared
1	—	—	—	Invalid setting

DDC mode switch interrupt flag

0	No interrupt is requested when automatic format switching is executed [Clearing condition] When 0 is written in IF after reading IF = 1
1	An interrupt is requested when automatic format switching is executed [Setting condition] When a falling edge is detected on the SCL pin when SWE = 1

DDC mode switch interrupt enable bit

0	Interrupt when automatic format switching is executed is disabled
1	Interrupt when automatic format switching is executed is enabled

DDC mode switch

0	IIC channel 0 is used with the I^2C bus format [Clearing conditions] • When 0 is written by software • When a falling edge is detected on the SCL pin when SWE = 1
1	IIC channel 0 is used in formatless mode [Setting condition] When 1 is written in SW after reading SW = 0

DDC mode switch enable

0	Automatic switching of IIC channel 0 from formatless mode to I^2C bus format is disabled
1	Automatic switching of IIC channel 0 from formatless mode to I^2C bus format is enabled

Notes: 1. Only 0 can be written, to clear the flag.
2. Always read as 1.

FLMCR1—Flash Memory Control Register 1 H'FF80 Flash Memory

Bit	7	6	5	4	3	2	1	0
	FWE	SWE	—	—	EV	PV	E	P
Initial value	1	0	0	0	0	0	0	0
Read/Write	R	R/W	—	—	R/W	R/W	R/W	R/W

Program

0	Program mode cleared
1	Transition to program mode [Setting condition] When SWE = 1, and PSU = 1

Erase

0	Erase mode cleared
1	Transition to erase mode [Setting condition] When SWE = 1, and ESU = 1

Program-verify

0	Program-verify mode cleared
1	Transition to program-verify mode [Setting condition] When SWE = 1

Erase-verify

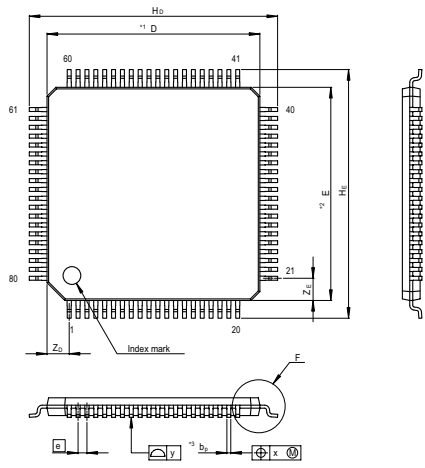
0	Erase-verify mode cleared
1	Transition to erase-verify mode [Setting condition] When SWE = 1

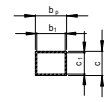
Software write enable

0	Writes disabled
1	Writes enabled

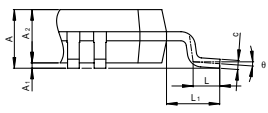
Reserved bit

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TQFP80-12x12-0.50	PTQP0080KC-A	TFP-80C/TFP-80CV	0.4g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS"*1"AND"*2" DO NOT INCLUDE MOLD FLASH
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	12	—
E	—	12	—
A_2	—	1.00	—
H_D	13.8	14.0	14.2
H_1	13.8	14.0	14.2
A	—	—	1.20
A_1	0.00	0.10	0.20
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.12	0.17	0.22
c_1	—	0.15	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.10
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.4	0.5	0.6
L_1	—	1.0	—

Figure G.2 Package Dimensions (TFP-80C)