Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	IrDA, SCI
Peripherals	POR, PWM, WDT
Number of I/O	58
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2134atf20v

Item	Specifications
14-bit PWM timer (PWMX)	• Up to 2 outputs • Resolution: 1/16384 • 312.5 kHz maximum carrier frequency (20-MHz operation)
Serial communication interface (SCI: 2 channels, SCI0 and SCI1)	• Asynchronous mode or synchronous mode selectable • Multiprocessor communication function
SCI with IrDA: 1 channel (SCI2)	• Asynchronous mode or synchronous mode selectable • Multiprocessor communication function • Compatible with IrDA specification version 1.0 • TxD and RxD encoding/decoding in IrDA format
Host interface (HIF) (H8S/2138 Group)	• 8-bit host interface (ISA) port • Three host interrupt requests (HIRQ11, HIRQ1, HIRQ12) • Normal and fast A20 gate output • Two register sets (each comprising two data registers and two status registers)
Keyboard controller	• Matrix keyboard control using keyboard scan with wakeup interrupt and sense port configuration
A/D converter	• Resolution: 10 bits • Input: — 8 channels (dedicated analog pins) — 8 channels (same pins as keyboard sense port) • High-speed conversion: 6.7 µs minimum conversion time (20-MHz operation) • Single or scan mode selectable • Sample-and-hold function • A/D conversion can be activated by external trigger or timer trigger
D/A converter	• Resolution: 8 bits • Output: 2 channels
I/O ports	• 58 input/output pins (including 24 with LED drive capability) • 8 input-only pins

7.2.2 DTC Mode Register B (MRB)

Bit	7	6	5	4	3	2	1	0
	CHNE	DISEL	—	—	—	—	—	—
Initial value	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
Read/Write	—	—	—	—	—	—	—	—

MRB is an 8-bit register that controls the DTC operating mode.

Bit 7—DTC Chain Transfer Enable (CHNE): Specifies chain transfer. In chain transfer, multiple data transfers can be performed consecutively in response to a single transfer request. With data transfer for which CHNE is set to 1, there is no determination of the end of the specified number of transfers, clearing of the interrupt source flag, or clearing of DTCER.

Bit 7

CHNE	Description
0	End of DTC data transfer (activation waiting state is entered)
1	DTC chain transfer (new register information is read, then data is transferred)

Bit 6—DTC Interrupt Select (DISEL): Specifies whether interrupt requests to the CPU are disabled or enabled after a data transfer.

Bit 6

DISEL	Description
0	After a data transfer ends, the CPU interrupt is disabled unless the transfer counter is 0 (the DTC clears the interrupt source flag of the activating interrupt to 0)
1	After a data transfer ends, the CPU interrupt is enabled (the DTC does not clear the interrupt source flag of the activating interrupt to 0)

Bits 5 to 0—Reserved: In the H8S/2138 Group these bits have no effect on DTC operation, and should always be written with 0.

7.3.9 Operation Timing

Figures 7.10 to 7.12 show examples of DTC operation timing.

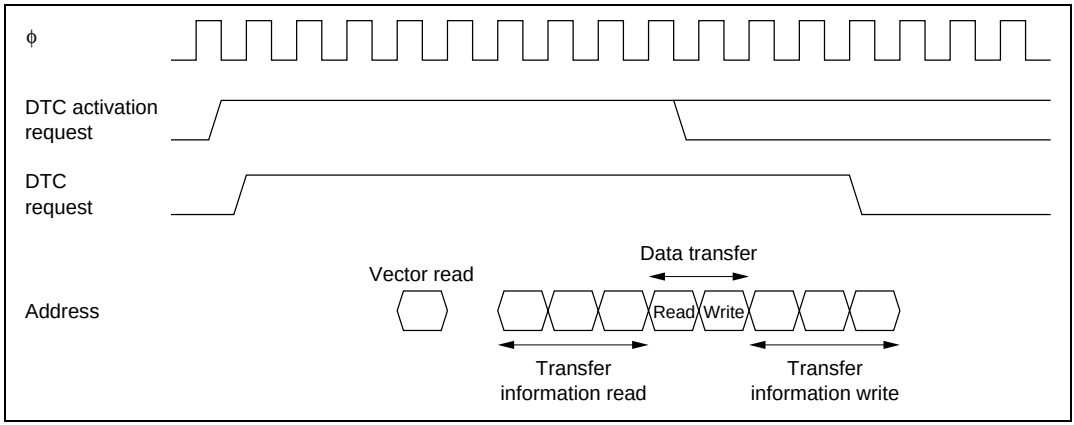


Figure 7.10 DTC Operation Timing (Normal Mode or Repeat Mode)

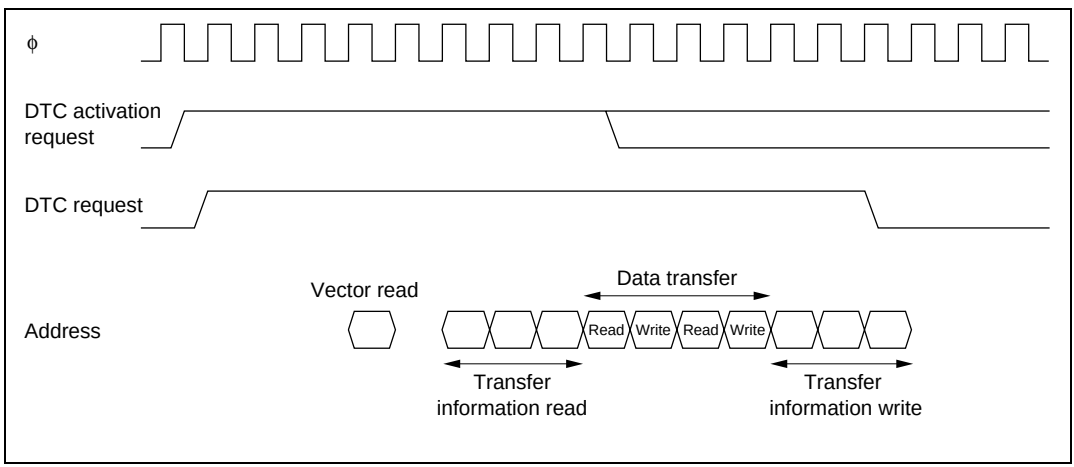


Figure 7.11 DTC Operation Timing (Block Transfer Mode, with Block Size of 2)

12.6.2 Contention between TCNT Write and Increment

If a timer counter clock pulse is generated during the T2 state of a TCNT write cycle, the write takes priority and the counter is not incremented. Figure 12.14 shows this operation.

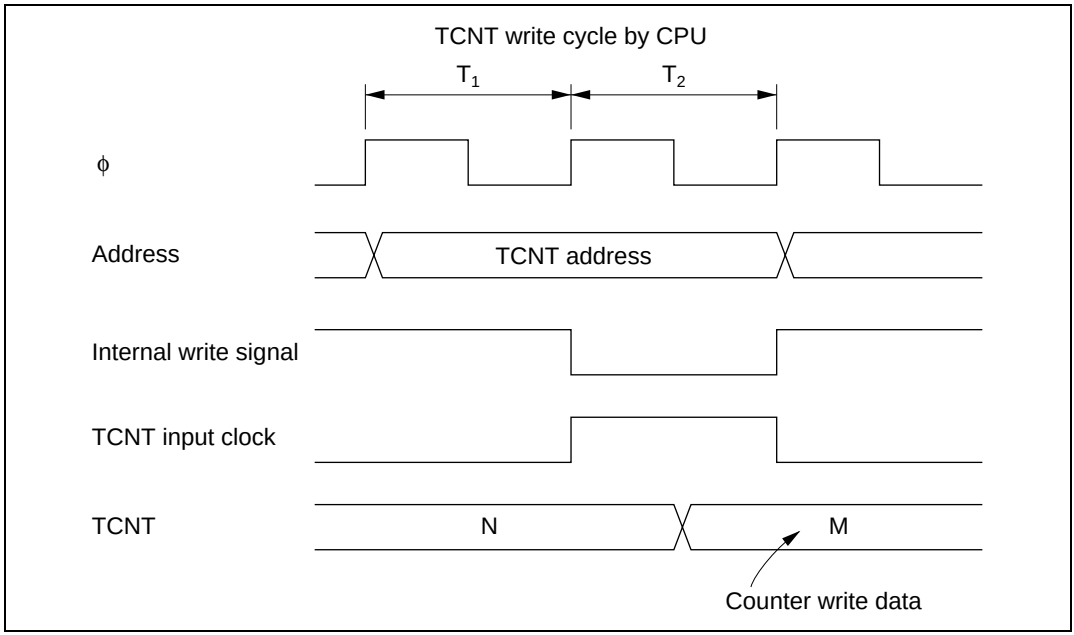
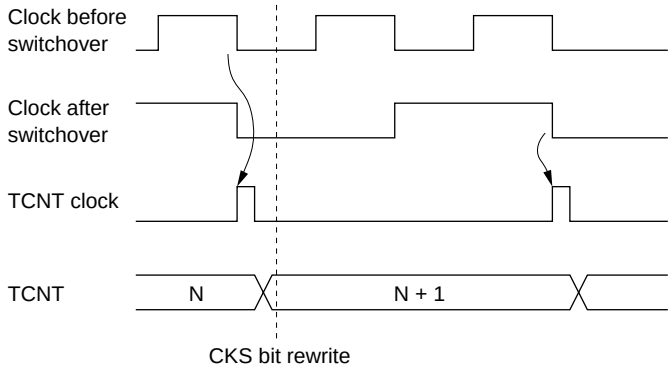
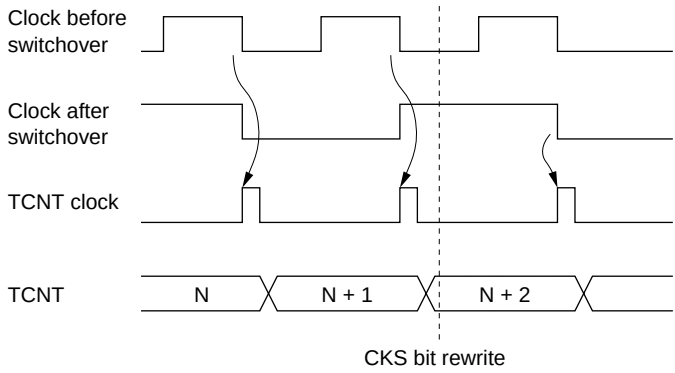


Figure 12.14 Contention between TCNT Write and Increment

Table 12.8 Switching of Internal Clock and TCNT Operation

No.	Timing of Switchover by Means of CKS1 and CKS0 Bits	TCNT Clock Operation
1	Switching from low to low*1	
2	Switching from low to high*2	

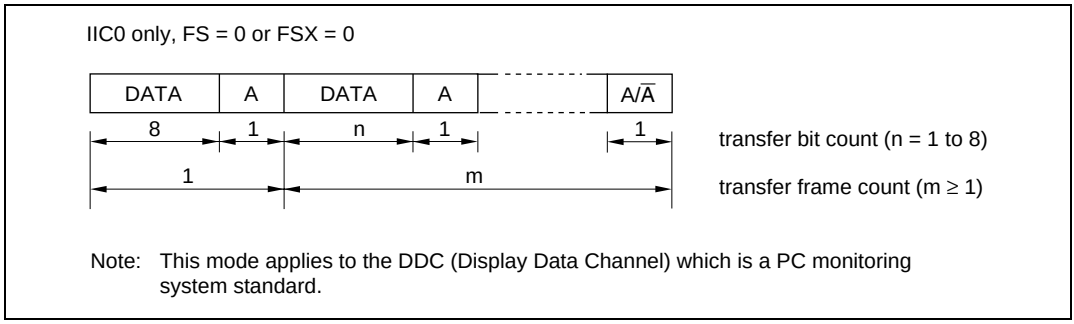


Figure 16.4 Formatless

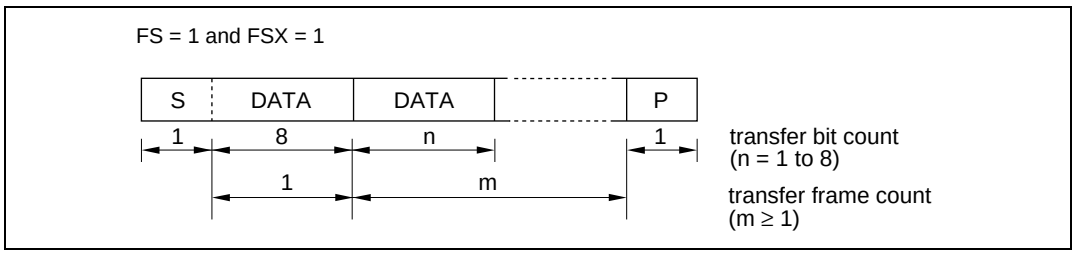


Figure 16.5 I²C Bus Data Format (Serial Format)

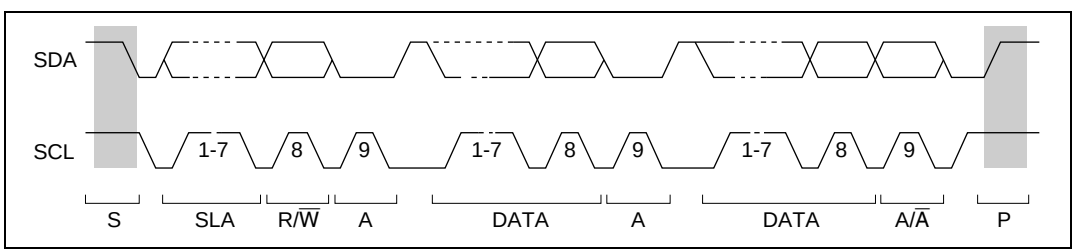


Figure 16.6 I²C Bus Timing

17.1.4 Register Configuration

Table 17.2 lists the host interface registers. Host interface registers HICR, IDR1, IDR2, ODR1, ODR2, STR1, and STR2 can only be accessed when the HIE bit is set to 1 in SYSCR.

Table 17.2 Host Interface Registers

Name	Abbreviation	R/W		Initial Value	Slave Address*3	Master Address*4		
		Slave	Host			$\overline{CS1}$	$\overline{CS2}$	HA0
System control register	SYSCR	R/W*1	—	H'09	H'FFC4	—	—	—
System control register 2	SYSCR2	R/W	—	H'00	H'FF83	—	—	—
Host interface control register	HICR	R/W	—	H'F8	H'FFF0	—	—	—
Input data register 1	IDR1	R	W	—	H'FFF4	0	1	0/1*5
Output data register 1	ODR1	R/W	R	—	H'FFF5	0	1	0
Status register 1	STR1	R/(W)*2	R	H'00	H'FFF6	0	1	1
Input data register 2	IDR2	R	W	—	H'FFFC	1	0	0/1*5
Output data register 2	ODR2	R/W	R	—	H'FFFD	1	0	0
Status register 2	STR2	R/(W)*2	R	H'00	H'FFFE	1	0	1
Module stop control register	MSTPCRH	R/W	—	H'3F	H'FF86	—	—	—
	MSTPCRL	R/W	—	H'FF	H'FF87	—	—	—

Notes: 1. Bits 5 and 3 are read-only bits.
2. The user-defined bits (bits 7 to 4 and 2) are read/write accessible from the slave processor.
3. Address when accessed from the slave processor. The lower 16 bits of the address are shown.
4. Pin inputs used in access from the host processor.
5. The HA0 input discriminates between writing of commands and data.

17.2 Register Descriptions

17.2.1 System Control Register (SYSCR)

Bit	7	6	5	4	3	2	1	0
	CS2E	IOSE	INTM1	INTM0	XRST	NMIEG	HIE	RAME
Initial value	0	0	0	0	1	0	0	1
Read/Write	R/W	R/W	R	R/W	R	R/W	R/W	R/W

SYSCR is an 8-bit readable/writable register which controls H8S/2138 Group chip operations. Of the host interface registers, HICR, IDR1, ODR1, STR1, IDR2, ODR2, and STR2 can only be accessed when the HIE bit is set to 1. The host interface $\overline{CS2}$ and $\overline{ECS2}$ pins are controlled by the CS2E bit in SYSCR and the FGA20E bit in HICR. See section 3.2.2, System Control Register (SYSCR), and section 5.2.1, System Control Register (SYSCR), for information on other SYSCR bits. SYSCR is initialized to H'09 by a reset and in hardware standby mode.

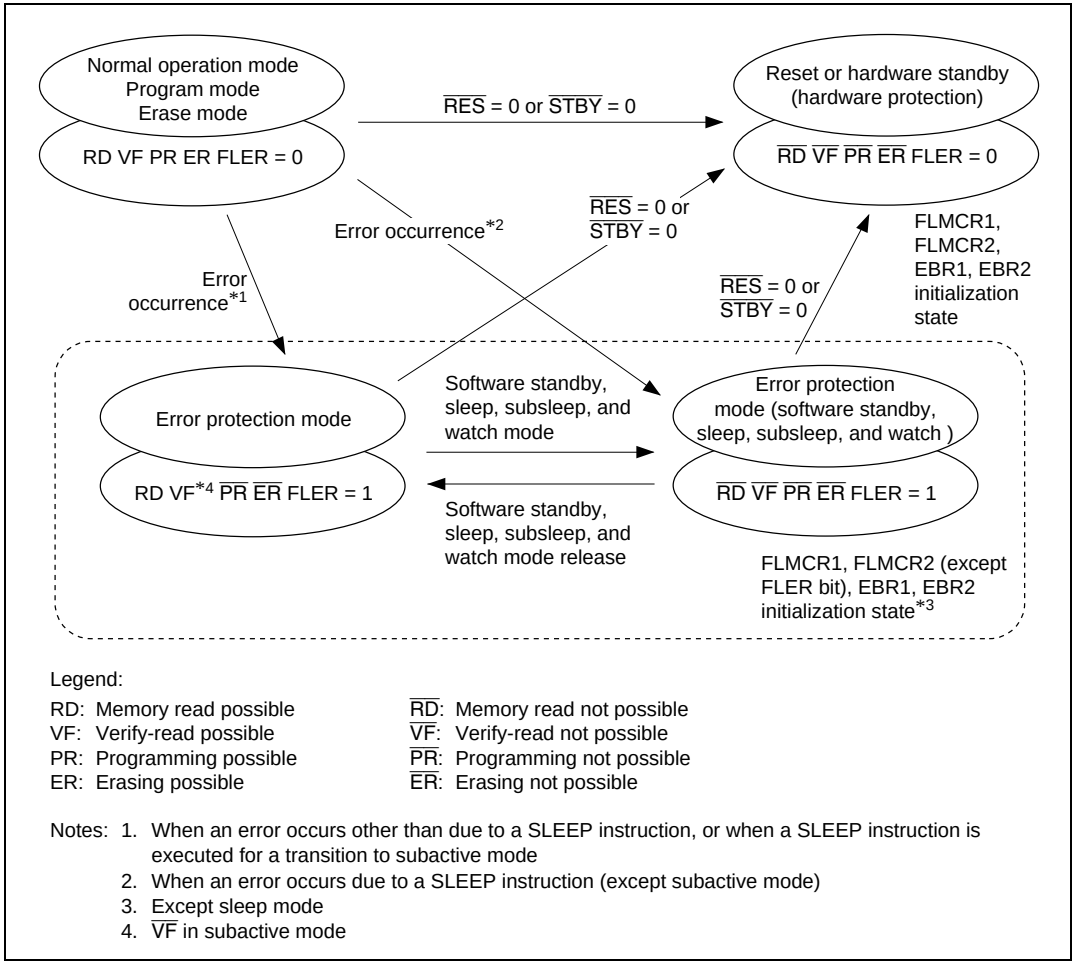
Bit 7—CS2 Enable Bit (CS2E): Used together with the FGA20E bit in HICR to select the pin that performs the $\overline{CS2}$ function.

SYSCR Bit 7	HICR Bit 0	
CS2E	**FGA20E**	**Description**
0	0	$\overline{CS2}$ pin function halted ($\overline{CS2}$ fixed high internally) (Initial value)
	1	
1	0	$\overline{CS2}$ pin function selected for P81/$\overline{CS2}$ pin
	1	$\overline{CS2}$ pin function selected for P90/$\overline{ECS2}$ pin

Bit 1—Host Interface Enable (HIE): Enables or disables CPU access to the host interface registers. When enabled, the host interface registers (HICR, IDR1, ODR1, STR1, IDR2, ODR2, and STR2) can be accessed.

Bit 1	
HIE	**Description**
0	Host interface register (HICR, IDR1, ODR1, STR1, IDR2, ODR2, STR2), CPU access is disabled (Initial value)
1	Host interface register (HICR, IDR1, ODR1, STR1, IDR2, ODR2, STR2), CPU access is enabled

Figure 22.14 shows the flash memory state transition diagram.



Legend:

RD: Memory read possible
VF: Verify-read possible
PR: Programming possible
ER: Erasing possible

$\overline{RD}$: Memory read not possible
$\overline{VF}$: Verify-read not possible
$\overline{PR}$: Programming not possible
$\overline{ER}$: Erasing not possible

Notes: 1. When an error occurs other than due to a SLEEP instruction, or when a SLEEP instruction is executed for a transition to subactive mode
2. When an error occurs due to a SLEEP instruction (except subactive mode)
3. Except sleep mode
4. $\overline{VF}$ in subactive mode

Figure 22.14 Flash Memory State Transitions

(2) Control Signal Timing

Table 25.7 shows the control signal timing. The only external interrupts that can operate on the subclock (ϕ = 32.768 kHz) are NMI and IRQ0, IRQ1, IRQ2, IRQ6, and IRQ7.

Table 25.7 Control Signal Timing

Condition A: V_{CC} = 5.0 V ±10%, V_{SS} = 0 V, ϕ = 32.768 kHz, 2 MHz to maximum operating frequency, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Condition B: V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0 V, ϕ = 32.768 kHz, 2 MHz to maximum operating frequency, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Condition C: V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0 V, ϕ = 32.768 kHz, 2 MHz to maximum operating frequency, T_a = –20 to +75°C

		Condition A		Condition B		Condition C			
		20 MHz		16 MHz		10 MHz			
Item	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
$\overline{RES}$ setup time	t_{RESS}	200	—	200	—	300	—	ns	Figure 25.8
$\overline{RES}$ pulse width	t_{RESW}	20	—	20	—	20	—	t_{cyc}	
NMI setup time (NMI)	t_{NMIS}	150	—	150	—	250	—	ns	Figure 25.9
NMI hold time (NMI)	t_{NMIH}	10	—	10	—	10	—		
NMI pulse width (exiting software standby mode)	t_{NMIW}	200	—	200	—	200	—	ns	
IRQ setup time ($\overline{IRQ7}$ to $\overline{IRQ0}$)	t_{IRQS}	150	—	150	—	250	—	ns	
IRQ hold time ($\overline{IRQ7}$ to $\overline{IRQ0}$)	t_{IRQH}	10	—	10	—	10	—	ns	
IRQ pulse width ($\overline{IRQ7}$, $\overline{IRQ6}$, $\overline{IRQ2}$ to $\overline{IRQ0}$) (exiting software standby mode)	t_{IRQW}	200	—	200	—	200	—	ns	

Table 25.41 Permissible Output Currents

Conditions: V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0 V, Ta = –20 to +75°C (regular specifications),
T_a = –40 to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin)	Ports 1, 2, 3	I_{OL}	—	—	10	mA
	Other output pins		—	—	2	mA
Permissible output low current (total)	Total of ports 1 to 3	$\sum I_{OL}$	—	—	80	mA
	Total of all output pins, including the above		—	—	120	mA
Permissible output high current (per pin)	All output pins	$-I_{OH}$	—	—	2	mA
Permissible output high current (total)	Total of all output pins	$\sum -I_{OH}$	—	—	40	mA

Conditions: V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0 V, T_a = –20 to +75°C

Item		Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin)	Ports 1, 2, 3	I_{OL}	—	—	2	mA
	Other output pins		—	—	1	mA
Permissible output low current (total)	Total of ports 1 to 3	$\sum I_{OL}$	—	—	40	mA
	Total of all output pins, including the above		—	—	60	mA
Permissible output high current (per pin)	All output pins	$-I_{OH}$	—	—	2	mA
Permissible output high current (total)	Total of all output pins	$\sum -I_{OH}$	—	—	30	mA

Notes: 1. To protect chip reliability, do not exceed the output current values in table 25.41.
2. When driving a Darlington pair or LED, always insert a current-limiting resistor in the output line, as show in figures 25.1 and 25.2.

25.5.3 AC Characteristics

Clock timing, control signal timing, bus timing, and timing of on-chip supporting modules list the following.

Figure 25.4 shows the test conditions for the AC characteristics.

Instruction	Mnemonic	Size	Instruction Format																	
			1st Byte		2nd Byte		3rd Byte		4th Byte		5th Byte		6th Byte		7th Byte		8th Byte		9th Byte	10th Byte
BOR	BOR #xx:3,Rd	B	7	4	0 IMM	rd														
	BOR #xx:3,@ERd	B	7	C	0 erd	0	7	4	0 IMM	0										
	BOR #xx:3,@aa:8	B	7	E	abs		7	4	0 IMM	0										
	BOR #xx:3,@aa:16	B	6	A	1	0	abs				7	4	0 IMM	0						
	BOR #xx:3,@aa:32	B	6	A	3	0	abs								7	4	0 IMM	0		
BSET	BSET #xx:3,Rd	B	7	0	0 IMM	rd														
	BSET #xx:3,@ERd	B	7	D	0 erd	0	7	0	0 IMM	0										
	BSET #xx:3,@aa:8	B	7	F	abs		7	0	0 IMM	0										
	BSET #xx:3,@aa:16	B	6	A	1	8	abs				7	0	0 IMM	0						
	BSET #xx:3,@aa:32	B	6	A	3	8	abs								7	0	0 IMM	0		
	BSET Rn,Rd	B	6	0	rn	rd														
	BSET Rn,@ERd	B	7	D	0 erd	0	6	0	rn	0										
	BSET Rn,@aa:8	B	7	F	abs		6	0	rn	0										
	BSET Rn,@aa:16	B	6	A	1	8	abs				6	0	rn	0						
	BSET Rn,@aa:32	B	6	A	3	8	abs								6	0	rn	0		
BSR	BSR d:8	—	5	5	disp															
	BSR d:16	—	5	C	0	0	disp													
BST	BST #xx:3,Rd	B	6	7	0 IMM	rd														
	BST #xx:3,@ERd	B	7	D	0 erd	0	6	7	0 IMM	0										
	BST #xx:3,@aa:8	B	7	F	abs		6	7	0 IMM	0										
	BST #xx:3,@aa:16	B	6	A	1	8	abs				6	7	0 IMM	0						
	BST #xx:3,@aa:32	B	6	A	3	8	abs								6	7	0 IMM	0		
BTST	BTST #xx:3,Rd	B	7	3	0 IMM	rd														
	BTST #xx:3,@ERd	B	7	C	0 erd	0	7	3	0 IMM	0										
	BTST #xx:3,@aa:8	B	7	E	abs		7	3	0 IMM	0										
	BTST #xx:3,@aa:16	B	6	A	1	0	abs				7	3	0 IMM	0						
	BTST #xx:3,@aa:32	B	6	A	3	0	abs								7	3	0 IMM	0		
	BTST Rn,Rd	B	6	3	rn	rd														
	BTST Rn,@ERd	B	7	C	0 erd	0	6	3	rn	0										

Instruction	Mnemonic		Instruction Fetch I	Branch Address Read J	Stack Operation K	Byte Data Access L	Word Data Access M	Internal Operation N
BXOR	BXOR #xx:3,Rd		1					
	BXOR #xx:3,@ERd		2			1		
	BXOR #xx:3,@aa:8		2			1		
	BXOR #xx:3,@aa:16		3			1		
	BXOR #xx:3,@aa:32		4			1		
CLRMAC	CLRMAC		Cannot be used with the H8S/2138 Group and H8S/2134 Group.					
CMP	CMP.B #xx:8,Rd		1					
	CMP.B Rs,Rd		1					
	CMP.W #xx:16,Rd		2					
	CMP.W Rs,Rd		1					
	CMP.L #xx:32,ERd		3					
	CMP.L ERs,ERd		1					
DAA	DAA Rd		1					
DAS	DAS Rd		1					
DEC	DEC.B Rd		1					
	DEC.W #1/2,Rd		1					
	DEC.L #1/2,ERd		1					
DIVXS	DIVXS.B Rs,Rd		2					11
	DIVXS.W Rs,ERd		2					19
DIVXU	DIVXU.B Rs,Rd		1					11
	DIVXU.W Rs,ERd		1					19
EEPMOV	EEPMOV.B		2			2n+2*2		
	EEPMOV.W		2			2n+2*2		
EXTS	EXTS.W Rd		1					
	EXTS.L ERd		1					
EXTU	EXTU.W Rd		1					
	EXTU.L ERd		1					
INC	INC.B Rd		1					
	INC.W #1/2,Rd		1					
	INC.L #1/2,ERd		1					
JMP	JMP @ERn		2					
	JMP @aa:24		2					1
	JMP @@aa:8	Normal	2	1				1
		Advanced	2	2				1

Lower Address	Register Name	H8S/2138 Group Register Selection Conditions		H8S/2134 Group Register Selection Conditions	Module Name
H'FFF0	HICR	MSTP2 = 0, HIE = 1 in SYSCR		—	HIF
	TCRX	MSTP8 = 0, HIE = 0 in SYSCR	TMRX/Y = 0 in TCONRS		TMRX
	TCRY		TMRX/Y = 1 in TCONRS	MSTP8 = 0, HIE = 0 in SYSCR	TMRY
H'FFF1	KMIMR	MSTP2 = 0, HIE = 1 in SYSCR		MSTP2 = 0, HIE = 1 in SYSCR	Interrupt controller
	TCSRX	MSTP8 = 0, HIE = 0 in SYSCR	TMRX/Y = 0 in TCONRS	—	TMRX
	TCSRY		TMRX/Y = 1 in TCONRS	MSTP8 = 0, HIE = 0 in SYSCR	TMRY
H'FFF2	KMPCR	MSTP2 = 0, HIE = 1 in SYSCR		MSTP2 = 0, HIE = 1 in SYSCR	Ports
	TICRR	MSTP8 = 0, HIE = 0 in SYSCR	TMRX/Y = 0 in TCONRS	—	TMRX
	TCORAY		TMRX/Y = 1 in TCONRS	MSTP8 = 0, HIE = 0 in SYSCR	TMRY
H'FFF3	TICRF	MSTP8 = 0, HIE = 0 in SYSCR	TMRX/Y = 0 in TCONRS	—	TMRX
	TCORBY		TMRX/Y = 1 in TCONRS	MSTP8 = 0, HIE = 0 in SYSCR	TMRY
H'FFF4	IDR1	MSTP2 = 0, HIE = 1 in SYSCR		—	HIF
	TCNTX	MSTP8 = 0, HIE = 0 in SYSCR	TMRX/Y = 0 in TCONRS		TMRX
	TCNTY		TMRX/Y = 1 in TCONRS	MSTP8 = 0, HIE = 0 in SYSCR	TMRY
H'FFF5	ODR1	MSTP2 = 0, HIE = 1 in SYSCR		—	HIF
	TCORC	MSTP8 = 0, HIE = 0 in SYSCR	TMRX/Y = 0 in TCONRS		TMRX
	TISR		TMRX/Y = 1 in TCONRS	MSTP8 = 0, HIE = 0 in SYSCR	TMRY
H'FFF6	STR1	MSTP2 = 0, HIE = 1 in SYSCR		—	HIF
	TCORAX	MSTP8 = 0, HIE = 0 in SYSCR	TMRX/Y = 0 in TCONRS		TMRX
H'FFF7	TCORBX				
H'FFF8	DADR0	MSTP10 = 0		MSTP10 = 0	D/A
H'FFF9	DADR1				
H'FFFA	DACR				

ISCRH—IRQ Sense Control Register H **H'FEEC** **Interrupt Controller**
ISCRL—IRQ Sense Control Register L **H'FEED** **Interrupt Controller**

ISCRH

Bit	15	14	13	12	11	10	9	8
	IRQ7SCB	IRQ7SCA	IRQ6SCB	IRQ6SCA	IRQ5SCB	IRQ5SCA	IRQ4SCB	IRQ4SCA
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IRQ7 to IRQ4 sense control A and B

ISCRL

Bit	7	6	5	4	3	2	1	0
	IRQ3SCB	IRQ3SCA	IRQ2SCB	IRQ2SCA	IRQ1SCB	IRQ1SCA	IRQ0SCB	IRQ0SCA
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IRQ3 to IRQ0 sense control A and B

ISCRH bits 7 to 0 ISCRL bits 7 to 0		Description
IRQ7SCB to IRQ0SCB	IRQ7SCA to IRQ0SCA	
0	0	Interrupt request generated at $\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$ input at low level
	1	Interrupt request generated at falling edge of $\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$ input
1	0	Interrupt request generated at rising edge of $\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$ input
	1	Interrupt request generated at both falling and rising edges of $\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$ input

TOCR—Timer Output Compare Control Register H'FF97 FRT

Bit	7	6	5	4	3	2	1	0
	ICRDMS	OCRAMS	ICRS	OCRS	OEA	OEB	OLVLA	OLVLB
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Output level B

0	A 0 logic level is output for compare-match B
1	A 1 logic level is output for compare-match B

Output level A

0	A 0 logic level is output for compare-match A
1	A 1 logic level is output for compare-match A

Output enable B

0	Output compare B output disabled
1	Output compare B output enabled

Output enable A

0	Output compare A output disabled
1	Output compare A output enabled

Output compare register select

0	OCRA register selected
1	OCRB register selected

Input capture register select

0	ICRA, ICRB, and ICRC registers selected
1	OCRAR, OCRAF, and OCRDM registers selected

Output compare A mode select

0	OCRA set to normal operating mode
1	OCRA set to operating mode using OCRAR and OCRAF

Input capture D mode select

0	ICRD set to normal operating mode
1	ICRD set to operating mode using OCRDM

P8DDR—Port 8 Data Direction Register **H'FFBD** **Port 8**

Bit	7	6	5	4	3	2	1	0
	—	P86DDR	P85DDR	P84DDR	P83DDR	P82DDR	P81DDR	P80DDR
Initial value	1	0	0	0	0	0	0	0
Read/Write	—	W	W	W	W	W	W	W

Specification of input or output for port 8 pins

P7PIN—Port 7 Input Data Register **H'FFBE** **Port 7**

Bit	7	6	5	4	3	2	1	0
	P77PIN	P76PIN	P75PIN	P74PIN	P73PIN	P72PIN	P71PIN	P70PIN
Initial value	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write	R	R	R	R	R	R	R	R

Port 7 pin states

Note: * Determined by state of pins P77 to P70.

P8DR—Port 8 Data Register **H'FFBF** **Port 8**

Bit	7	6	5	4	3	2	1	0
	—	P86DR	P85DR	P84DR	P83DR	P82DR	P81DR	P80DR
Initial value	1	0	0	0	0	0	0	0
Read/Write	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Output data for port 8 pins

C.7 Port 7 Block Diagrams

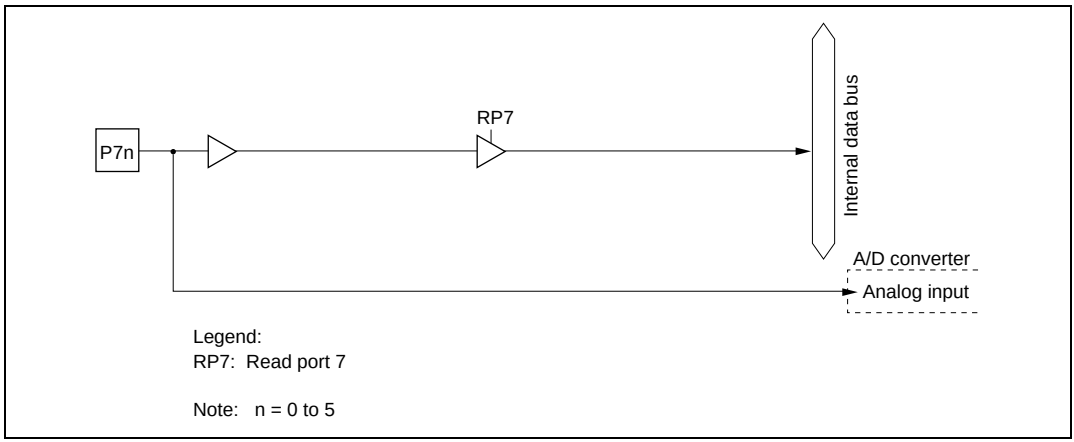


Figure C.21 Port 7 Block Diagram (Pins P70 to P75)

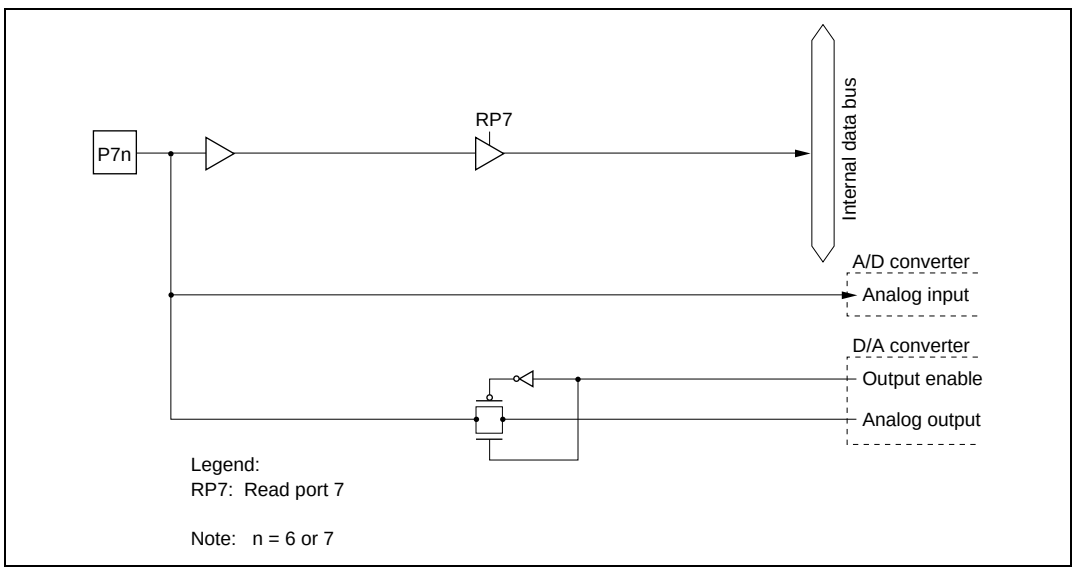


Figure C.22 Port 7 Block Diagram (Pins P76, P77)

Port Name Pin Name	MCU Operating Mode	Reset	Hardware Standby Mode	Software Standby Mode	Watch Mode	Sleep Mode	Sub-sleep Mode	Subactive Mode	Program Execution State
Port 96 ϕ EXCL	1	Clock output	T	[DDR = 1] H [DDR = 0] T	EXCL input	[DDR = 1] clock output [DDR = 0] T	EXCL input	EXCL input	Clock output/ EXCL input/ input port
	2, 3 (EXPE = 1)	T							
	2, 3 (EXPE = 0)								
Port 95 to 93 $\overline{AS}$, $\overline{WR}$, $\overline{RD}$	1	H	T	H	H	H	H	$\overline{AS}$, $\overline{WR}$, $\overline{RD}$	$\overline{AS}$, $\overline{WR}$, $\overline{RD}$
	2, 3 (EXPE = 1)	T							
	2, 3 (EXPE = 0)			keep	keep	keep	keep	I/O port	I/O port
Port 92 to 90	1	T	T	keep	keep	keep	keep	I/O port	I/O port
	2, 3 (EXPE = 1)								
	2, 3 (EXPE = 0)								

Legend:

H: High

L: Low

T: High-impedance state

keep: Input ports are in the high-impedance state (when DDR = 0 and PCR = 1, MOS input pull-ups remain on).

Output ports maintain their previous state.

Depending on the pins, the on-chip supporting modules may be initialized and the I/O port function determined by DDR and DR used.

DDR: Data direction register

Note: * In the case of address output, the last address accessed is retained.

H8S/2138 Group, H8S/2134 Group, H8S/2138F-ZTAT™, H8S/2134F-ZTAT™, H8S/2132F-ZTAT™

Hardware Manual

Renesas Electronics Corporation
1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan

REJ09B0301-0400