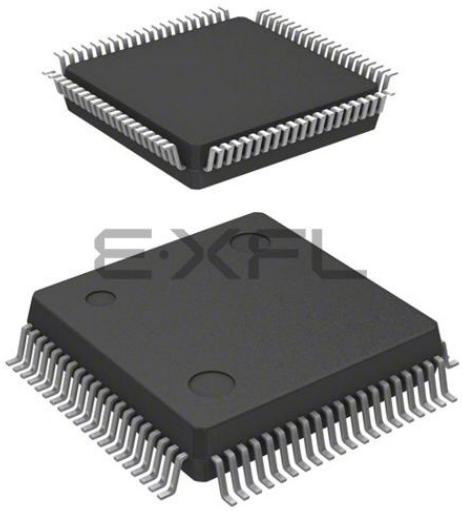

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Details	
Product Status	Not For New Designs
Core Processor	H8S/2000
Core Size	16-Bit
Speed	10MHz
Connectivity	IrDA, SCI
Peripherals	POR, PWM, WDT
Number of I/O	58
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2134avfa10v

Section 9 8-Bit PWM Timers [H8S/2138 Group]

Section 10 14-Bit PWM D/A

Section 11 16-Bit Free-Running Timer

Section 12 8-Bit Timers

Section 13 Timer Connection [H8S/2138 Group]

1.3.2 Pin Functions in Each Operating Mode

Tables 1.2 and 1.3 show the pin functions of the H8S/2138 Group and H8S/2134 Group in each of the operating modes.

Table 1.2 H8S/2138 Group Pin Functions in Each Operating Mode

Pin No.	Pin Name			
	Expanded Modes		Single-Chip Modes	Flash Memory Programmer Mode
FP-80A TFP-80C	Mode 1	Mode 2 (EXPE = 1) Mode 3 (EXPE = 1)	Mode 2 (EXPE = 0) Mode 3 (EXPE = 0)	
1	$\overline{RES}$	$\overline{RES}$	$\overline{RES}$	$\overline{RES}$
2	XTAL	XTAL	XTAL	XTAL
3	EXTAL	EXTAL	EXTAL	EXTAL
4	MD1	MD1	MD1	VSS
5	MD0	MD0	MD0	VSS
6	NMI	NMI	NMI	FA9
7	$\overline{STBY}$	$\overline{STBY}$	$\overline{STBY}$	VCC
8	VCC2 (VCL)	VCC2 (VCL)	VCC2 (VCL)	VCC
9	P52/SCK0/SCL0	P52/SCK0/SCL0	P52/SCK0/SCL0	NC
10	P51/RxD0	P51/RxD0	P51/RxD0	FA17
11	P50/TxD0	P50/TxD0	P50/TxD0	NC
12	VSS	VSS	VSS	VSS
13	P97/$\overline{WAIT}$/SDA0	P97/$\overline{WAIT}$/SDA0	P97/SDA0	VCC
14	ϕ/P96/EXCL	ϕ/P96/EXCL	P96/ϕ/EXCL	NC
15	$\overline{AS}$/$\overline{IOS}$	$\overline{AS}$/$\overline{IOS}$	P95/$\overline{CS1}$	FA16
16	$\overline{WR}$	$\overline{WR}$	P94/$\overline{IOW}$	FA15
17	$\overline{RD}$	$\overline{RD}$	P93/$\overline{IOR}$	$\overline{WE}$
18	P92/$\overline{IRQ0}$	P92/$\overline{IRQ0}$	P92/$\overline{IRQ0}$	VSS
19	P91/$\overline{IRQ1}$	P91/$\overline{IRQ1}$	P91/$\overline{IRQ1}$	VCC
20	P90/$\overline{IRQ2}$/ $\overline{ADTRG}$	P90/$\overline{IRQ2}$/$\overline{ADTRG}$	P90/$\overline{IRQ2}$/$\overline{ADTRG}$/ $\overline{ECS2}$	VCC
21	P60/FTCI/CIN0/ $\overline{KIN0}$/TMIX/ HFBACKI	P60/FTCI/CIN0/ $\overline{KIN0}$/TMIX/ HFBACKI	P60/FTCI/CIN0/ $\overline{KIN0}$/TMIX/ HFBACKI	NC
22	P61/FTOA/CIN1/ $\overline{KIN1}$/VSYNCO	P61/FTOA/CIN1/ $\overline{KIN1}$/VSYNCO	P61/FTOA/CIN1/ $\overline{KIN1}$/VSYNCO	NC

5.5.2 Interrupt Control Mode 0

Enabling and disabling of IRQ interrupts and on-chip supporting module interrupts can be set by means of the I bit in the CPU's CCR, and ICR. Interrupts are enabled when the I bit is cleared to 0, and disabled when set to 1. Control level 1 interrupt sources have higher priority.

Figure 5.8 shows a flowchart of the interrupt acceptance operation in this case.

1. If an interrupt source occurs when the corresponding interrupt enable bit is set to 1, an interrupt request is sent to the interrupt controller.

2. When interrupt requests are sent to the interrupt controller, a control level 1 interrupt, according to the control level set in ICR, has priority for selection, and other interrupt requests are held pending. If a number of interrupt requests with the same control level setting are generated at the same time, the interrupt request with the highest priority according to the priority system shown in table 5.4 is selected.

3. The I bit is then referenced. If the I bit is cleared to 0, the interrupt request is accepted. If the I bit is set to 1, only NMI and address break interrupts are accepted, and other interrupt requests are held pending.

4. When an interrupt request is accepted, interrupt exception handling starts after execution of the current instruction has been completed.

5. The PC and CCR are saved to the stack area by interrupt exception handling. The PC saved on the stack shows the address of the first instruction to be executed after returning from the interrupt handling routine.

6. Next, the I bit in CCR is set to 1. This disables all interrupts except NMI and address break interrupts.

7. A vector address is generated for the accepted interrupt, and execution of the interrupt handling routine starts at the address indicated by the contents of that vector address.

6.7 Bus Arbitration

6.7.1 Overview

The H8S/2138 Group and H8S/2134 Group have a bus arbiter that arbitrates bus master operations.

There are two bus masters, the CPU and the DTC, which perform read/write operations when they have possession of the bus. Each bus master requests the bus by means of a bus request signal. The bus arbiter determines priorities at the prescribed timing, and permits use of the bus by means of a bus request acknowledge signal. The selected bus master then takes possession of the bus and begins its operation.

6.7.2 Operation

The bus arbiter detects the bus masters' bus request signals, and if the bus is requested, sends a bus request acknowledge signal to the bus master making the request. If there are bus requests from both bus masters, the bus request acknowledge signal is sent to the one with the higher priority. When a bus master receives the bus request acknowledge signal, it takes possession of the bus until that signal is canceled.

The order of priority of the bus masters is as follows:

(High) DTC > CPU (Low)

Table 7.9 Number of States Required for Each Execution Phase

Object of Access			On-Chip RAM	On-Chip ROM	Internal I/O Registers		External Devices	
Bus width			32	16	8	16	8	8
Access states			1	1	2	2	2	3
Execution phase	Vector read	S_I	—	1	—	—	4	6+2m
	Register information read/write	S_J	1	—	—	—	—	—
	Byte data read	S_K	1	1	2	2	2	3+m
	Word data read	S_K	1	1	4	2	4	6+2m
	Byte data write	S_L	1	1	2	2	2	3+m
	Word data write	S_L	1	1	4	2	4	6+2m
	Internal operation	S_M	1	1	1	1	1	1

The number of execution states is calculated from the formula below. Note that Σ means the sum of all transfers activated by one activation event (the number for which the CHNE bit is set to one, plus 1).

$$\text{Number of execution states} = I \cdot S_I + \Sigma (J \cdot S_J + K \cdot S_K + L \cdot S_L) + M \cdot S_M$$

For example, when the DTC vector address table is located in on-chip ROM, normal mode is set, and data is transferred from the on-chip ROM to an internal I/O register, the time required for the DTC operation is 13 states. The time from activation to the end of the data write is 10 states.

Port 3 Data Register (P3DR)

Bit	7	6	5	4	3	2	1	0
	P37DR	P36DR	P35DR	P34DR	P33DR	P32DR	P31DR	P30DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P3DR is an 8-bit readable/writable register that stores output data for the port 3 pins (P37 to P30). If a port 3 read is performed while P3DDR bits are set to 1, the P3DR values are read directly, regardless of the actual pin states. If a port 3 read is performed while P3DDR bits are cleared to 0, the pin states are read.

P3DR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Port 3 MOS Pull-Up Control Register (P3PCR)

Bit	7	6	5	4	3	2	1	0
	P37PCR	P36PCR	P35PCR	P34PCR	P33PCR	P32PCR	P31PCR	P30PCR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P3PCR is an 8-bit readable/writable register that controls the port 3 on-chip MOS input pull-ups on a bit-by-bit basis.

In modes 2 and 3 (when EXPE = 0), the MOS input pull-up is turned on when a P3PCR bit is set to 1 while the corresponding P3DDR bit is cleared to 0 (input port setting).

P3PCR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode.

The MOS input pull-up function cannot be used in slave mode (when the host interface is enabled).

8.8 Port 7

8.8.1 Overview

Port 7 is an 8-bit input port. Port 7 pins also function as the A/D converter analog input pins (AN0 to AN7) and D/A converter analog output pins (DA0, DA1). Port 7 functions are the same in all operating modes.

Figure 8.15 shows the port 7 pin configuration.

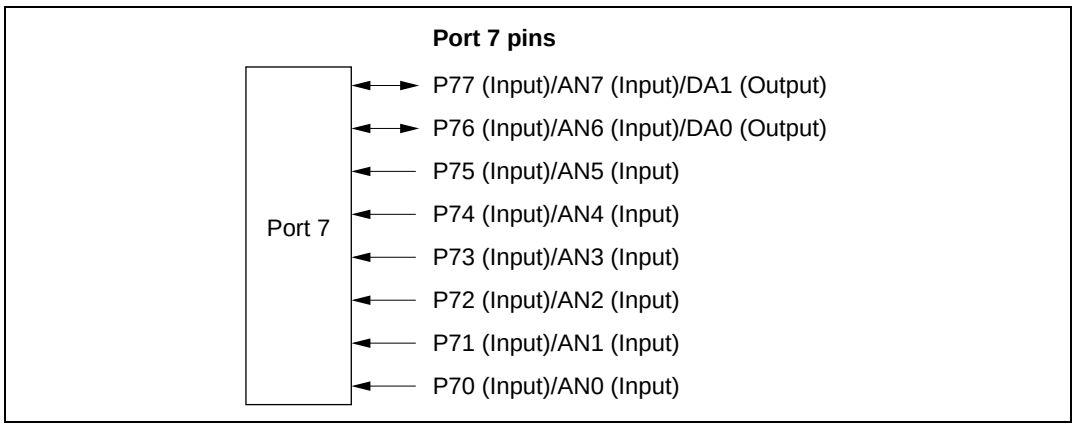


Figure 8.15 Port 7 Pin Functions

8.8.2 Register Configuration

Table 8.16 shows the port 7 register configuration. Port 7 is an input-only port, and does not have a data direction register or data register.

Table 8.16 Port 7 Registers

Name	Abbreviation	R/W	Initial Value	Address*
Port 7 input data register	P7PIN	R	Undefined	H'FFBE

Note: * Lower 16 bits of the address.

Bit 2—Transmit End (TEND): Indicates that there is no valid data in TDR when the last bit of the transmit character is sent, and transmission has been ended.

The TEND flag is read-only and cannot be modified.

Bit 2

TEND	Description
0	[Clearing conditions] • When 0 is written in TDRE after reading TDRE = 1 • When the DTC is activated by a TXI interrupt and writes data to TDR
1	[Setting conditions] (Initial value) • When the TE bit in SCR is 0 • When TDRE = 1 at transmission of the last bit of a 1-byte serial transmit character

Bit 1—Multiprocessor Bit (MPB): When reception is performed using a multiprocessor format in asynchronous mode, MPB stores the multiprocessor bit in the receive data.

MPB is a read-only bit, and cannot be modified.

Bit 1

MPB	Description
0	[Clearing condition] (Initial value)* When data with a 0 multiprocessor bit is received
1	[Setting condition] When data with a 1 multiprocessor bit is received

Note: * Retains its previous state when the RE bit in SCR is cleared to 0 with multiprocessor format.

Bit 5	Bit 4		
MST	**TRS**	**Operating Mode**	
0	0	Slave receive mode	(Initial value)
	1	Slave transmit mode	
1	0	Master receive mode	
	1	Master transmit mode	

Bit 5

MST	Description
0	Slave mode (Initial value) [Clearing conditions] 1. When 0 is written by software 2. When bus arbitration is lost after transmission is started in I²C bus format master mode
1	Master mode [Setting conditions] 1. When 1 is written by software (in cases other than clearing condition 2) 2. When 1 is written in MST after reading MST = 0 (in case of clearing condition 2)

Bit 4

TRS	Description
0	Receive mode (Initial value) [Clearing conditions] 1. When 0 is written by software (in cases other than setting condition 3) 2. When 0 is written in TRS after reading TRS = 1 (in case of clearing condition 3) 3. When bus arbitration is lost after transmission is started in I²C bus format master mode 4. When the SW bit in DDCSWR changes from 1 to 0
1	Transmit mode [Setting conditions] 1. When 1 is written by software (in cases other than clearing conditions 3 and 4) 2. When 1 is written in TRS after reading TRS = 0 (in case of clearing conditions 3 and 4) 3. When a 1 is received as the R/$\overline{W}$ bit of the first frame in I²C bus format slave mode

Bit 2—Bus Busy (BBSY): The BBSY flag can be read to check whether the I²C bus (SCL, SDA) is busy or free. In master mode, this bit is also used to issue start and stop conditions.

A high-to-low transition of SDA while SCL is high is recognized as a start condition, setting BBSY to 1. A low-to-high transition of SDA while SCL is high is recognized as a stop condition, clearing BBSY to 0.

To issue a start condition, use a MOV instruction to write 1 in BBSY and 0 in SCP. A retransmit start condition is issued in the same way. To issue a stop condition, use a MOV instruction to write 0 in BBSY and 0 in SCP. It is not possible to write to BBSY in slave mode; the I²C bus interface must be set to master transmit mode before issuing a start condition. MST and TRS should both be set to 1 before writing 1 in BBSY and 0 in SCP.

Bit 2

BBSY	Description	
0	Bus is free	(Initial value)
	[Clearing condition]	
	When a stop condition is detected	
1	Bus is busy	
	[Setting condition]	
	When a start condition is detected	

Bit 1—I²C Bus Interface Interrupt Request Flag (IRIC): Indicates that the I²C bus interface has issued an interrupt request to the CPU. IRIC is set to 1 at the end of a data transfer, when a slave address or general call address is detected in slave receive mode, when bus arbitration is lost in master transmit mode, and when a stop condition is detected. IRIC is set at different times depending on the FS bit in SAR and the WAIT bit in ICMR. See section 16.3.6, IRIC Setting Timing and SCL Control. The conditions under which IRIC is set also differ depending on the setting of the ACKE bit in ICCR.

IRIC is cleared by reading IRIC after it has been set to 1, then writing 0 in IRIC.

When the DTC is used, IRIC is cleared automatically and transfer can be performed continuously without CPU intervention.

Bit 1—Input Buffer Full (IBF): Set to 1 when the host processor writes to IDR2. This bit is an internal interrupt source to the slave processor. IBF is cleared to 0 when the slave processor reads IDR2.

The IBF flag setting and clearing conditions are different when the fast A20 gate is used. For details see table 17.8, Fast A20 Gate Output Signals.

Bit 1

IBF	Description
0	[Clearing condition]
	When the slave processor reads IDR2 (Initial value)
1	[Setting condition]
	When the host processor writes to IDR2

Bit 0—Output Buffer Full (OBF): Set to 1 when the slave processor writes to ODR2. Cleared to 0 when the host processor reads ODR2. The IBF flag setting and clearing conditions are different when the fast A20 gate is used. For details see table 17.8, Fast A20 Gate Output Signals.

Bit 0

OBF	Description
0	[Clearing condition]
	When the host processor reads ODR2 or the slave writes 0 in the OBF bit (Initial value)
1	[Setting condition]
	When the slave processor writes to ODR2

Table 17.4 shows the conditions for setting and clearing the STR2 flags.

17.3 Operation

17.3.1 Host Interface Operation

The host interface is activated by setting the HI12E bit (bit 0) to 1 in SYSCR2 in single-chip mode, establishing slave mode. Activation of the host interface (entry to slave mode) appropriates the related I/O lines in port 3 (data), port 8 or 9 (control), and port 4 (host interrupt requests) for interface use.

Table 17.5 shows HIF host interface channel selection and pin operation.

Table 17.5 Host Interface Channel Selection and Pin Operation

HI12E	CS2E	Operation
0	—	Host interface functions halted
1	0	Host interface channel 1 only operating Operation of channel 2 halted (No operation as $\overline{CS2}$ or $\overline{ECS2}$ input. Pins P43, P81, and P90 operate as I/O ports.)
	1	Host interface channel 1 and 2 functions operating

For host read/write timing, see section 25.6.4, Timing of On-Chip Supporting Modules.

17.3.2 Control States

Table 17.6 indicates the slave operations carried out in response to host interface signals from the host processor.

Bits 6 to 2—Reserved: These bits cannot be modified and are always read as 0.

Bits 1 and 0—Mode Select 1 and 0 (MDS1, MDS0): These bits indicate values that reflects the input levels of mode pins MD1 and MD0 (the current operating mode). Bits MDS1 and MDS0 correspond to pins MD1 and MD0, respectively. These are read-only bits, and cannot be modified. When MDCR is read, the input levels of mode pins MD1 and MD0 are latched in these bits.

21.3 Operation

The on-chip ROM is connected to the CPU by a 16-bit data bus, and both byte and word data is accessed in one state. Even addresses are connected to the upper 8 bits, and odd addresses to the lower 8 bits. Word data must start at an even address.

The mode pins (MD1 and MD0) and the EXPE bit in MDCR can be set to enable or disable the on-chip ROM, as shown in table 21.2.

In normal mode, the maximum amount of ROM that can be used is 56 kbytes.

Table 21.2 Operating Modes and ROM

Operating Mode						
MCU Operating Mode	CPU Operating Mode	Description	Mode Pins MD1	Mode Pins MD0	MDCR EXPE	On-Chip ROM
Mode 1	Normal	Expanded mode with on-chip ROM disabled	0	1	1	Disabled
Mode 2	Advanced	Single-chip mode	1	0	0	Enabled*
	Advanced	Expanded mode with on-chip ROM enabled			1	
Mode 3	Normal	Single-chip mode		1	0	Enabled (max. 56 kbytes)
	Normal	Expanded mode with on-chip ROM enabled			1	

Note: * 128 kbytes in the H8S/2138 and H8S/2134, 96 kbytes in the H8S/2133, 64 kbytes in the H8S/2137 and H8S/2132, and 32 kbytes in the H8S/2130.

Bit 3—Flash Memory Control Register Enable (FLSHE): Setting the FLSHE bit to 1 enables read/write access to the flash memory control registers. If FLSHE is cleared to 0, the flash memory control registers are deselected. In this case, the flash memory control register contents are retained.

Bit 3		
FLSHE	**Description**	
0	Flash memory control registers deselected	(Initial value)
1	Flash memory control registers selected	

Bit 2—Reserved: Do not write 1 to this bit.

Bits 1 and 0—Internal Clock Select 1 and 0 (ICKS1, ICKS0): These bits control 8-bit timer operation. See section 12, 8-Bit Timers, for details.

21.6 On-Board Programming Modes

When pins are set to on-board programming mode, program/erase/verify operations can be performed on the on-chip flash memory. There are two on-board programming modes: boot mode and user program mode. The pin settings for transition to each of these modes are shown in table 21.6. For a diagram of the transitions to the various flash memory modes, see figure 21.3.

Only advanced mode setting is possible for boot mode.

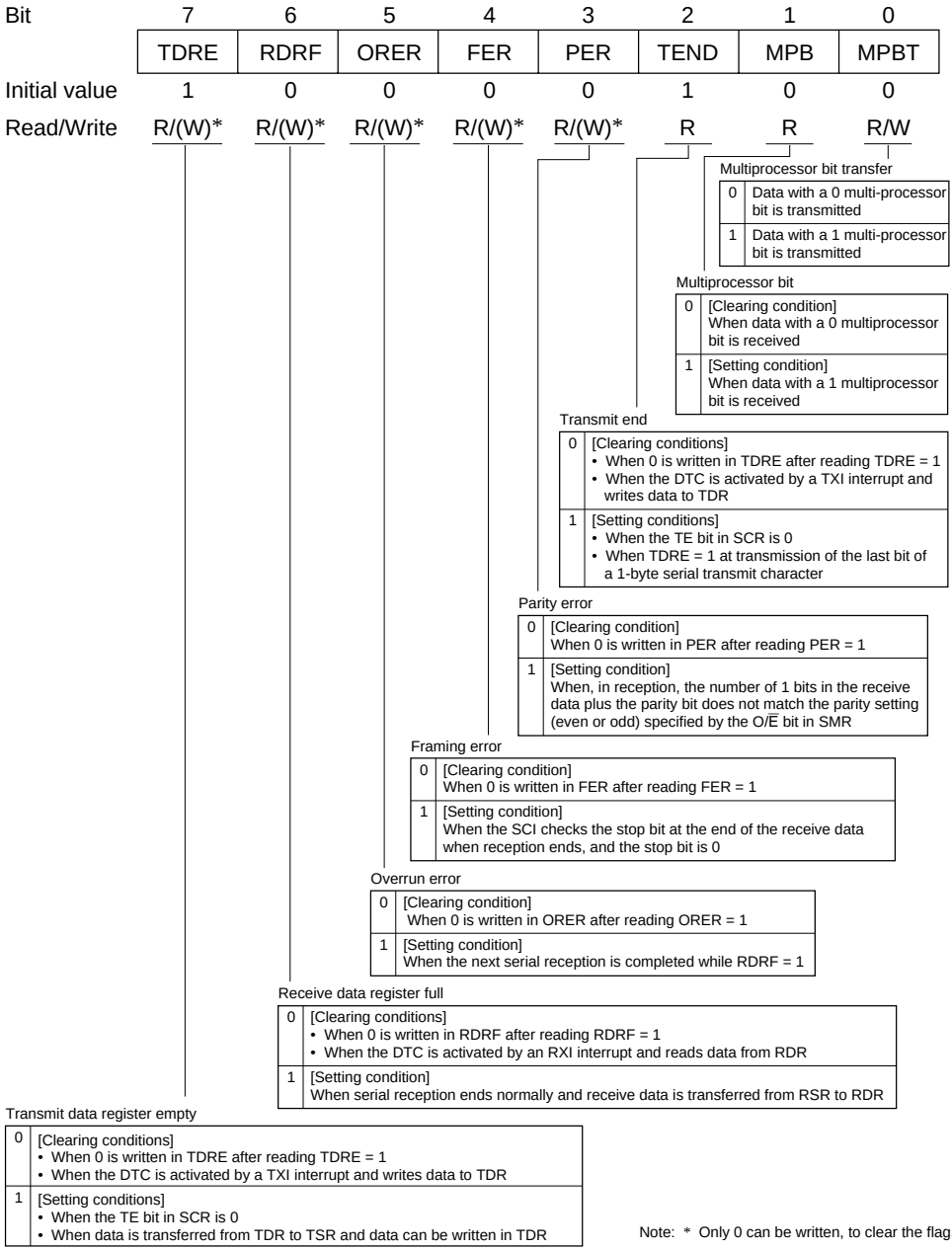
In the case of user program mode, established in advanced mode or normal mode, depending on the setting of the MD0 pin. In normal mode, only programming of a 56-kbyte area of flash memory is possible.

Table 21.6 Setting On-Board Programming Modes

	Mode					
Mode Name	**CPU Operating Mode**	**MD1**	**MD0**	**P92**	**P91**	**P90**
Boot mode	Advanced mode	0	0	1*	1*	1*
User program mode	Advanced mode	1	0	—	—	—
	Normal mode		1	—	—	—

Note: * Can be used as I/O ports after boot mode is initiated.

SSR1—Serial Status Register 1 **H'FF8C** **SCI1**
SSR2—Serial Status Register 2 **H'FFA4** **SCI2**
SSR0—Serial Status Register 0 **H'FFDC** **SCI0**



Note: * Only 0 can be written, to clear the flag.

SYSCR—System Control Register H'FFC4 System

Bit	7	6	5	4	3	2	1	0
	CS2E	IOSE	INTM1	INTM0	XRST	NMIEG	HIE	RAME
Initial value	0	0	0	0	1	0	0	1
Read/Write	R/W	R/W	R	R/W	R	R/W	R/W	R/W

RAM Enable

0	On-chip RAM is disabled
1	On-chip RAM is enabled

Host interface enable

0	Addresses H'(FF)FFF0 to H'(FF)FFF7 and H'(FF)FFFC to H'(FF)FFFF are used for access to 8-bit timer (channel X and Y) data registers and control registers, and timer connection control registers
1	Addresses H'(FF)FFF0 to H'(FF)FFF7 and H'(FF)FFFC to H'(FF)FFFF are used for access to host interface data registers and control registers, and keyboard controller and MOS input pull-up control registers

NMI edge select

0	Falling edge
1	Rising edge

External reset

0	Reset generated by watchdog timer overflow
1	Reset generated by an external reset

Interrupt control selection mode 1 and 0

Bit 5 INTM1	Bit 4 INTM0	Interrupt control mode	Description
0	0	0	Interrupts controlled by I bit (Initial value)
	1	1	Interrupts controlled by I and UI bits, and ICR
1	0	2	Cannot be used in the LSI
	1	3	Cannot be used in the LSI

IOS enable

0	The $\overline{AS}$/$\overline{IOS}$ pin functions as the address strobe pin (Low output when accessing an external area)
1	The $\overline{AS}$/$\overline{IOS}$ pin functions as the I/O strobe pin (Low output when accessing a specified address from H'(FF)F000 to H'(FF)FE4F)*

Note: * In the H8S/2138 F-ZTAT A-mask version, the address range is from H'(FF)F000 to H'(FF)F7FF.

CS2 enable

SYSCR Bit 7 CS2E	HICR Bit 0 FGA20E	Description
0	0	$\overline{CS2}$ pin function halted ($\overline{CS2}$ fixed high internally)
	1	
1	0	$\overline{CS2}$ pin function selected for P81/$\overline{CS2}$ pin
	1	$\overline{CS2}$ pin function selected for P90/$\overline{ECS2}$ pin

BCR—Bus Control Register **H'FFC6** **Bus Controller**

Bit	7	6	5	4	3	2	1	0
	ICIS1	ICIS0	BRSTRM	BRSTS1	BRSTS0	—	IOS1	IOS0
Initial value	1	1	0	1	0	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IOS select

IOS1	IOS0	Addresses for which AS/IOS is low output when IOSE = 1
0	0	Low output when accessing addresses H'(FF)F000 to H'(FF)F03F
	1	Low output when accessing addresses H'(FF)F000 to H'(FF)F0FF
1	0	Low output when accessing addresses H'(FF)F000 to H'(FF)F3FF
	1	Low output when accessing addresses H'(FF)F000 to H'(FF)FE4F*

Note: * In the H8S/2138 F-ZTAT A-mask version, the address range is from H'(FF)F000 to H'(FF)F7FF.

Burst cycle select 0

0	Max. 4 words in burst access
1	Max. 8 words in burst access

Burst cycle select 1

0	Burst cycle comprises 1 state
1	Burst cycle comprises 2 states

Burst ROM enable

0	Basic bus interface
1	Burst ROM interface

Reserved

Idle cycle insert 0

0	Idle cycle not inserted in case of successive external read and external write cycles
1	Idle cycle inserted in case of successive external read and external write cycles

C.2 Port 2 Block Diagrams

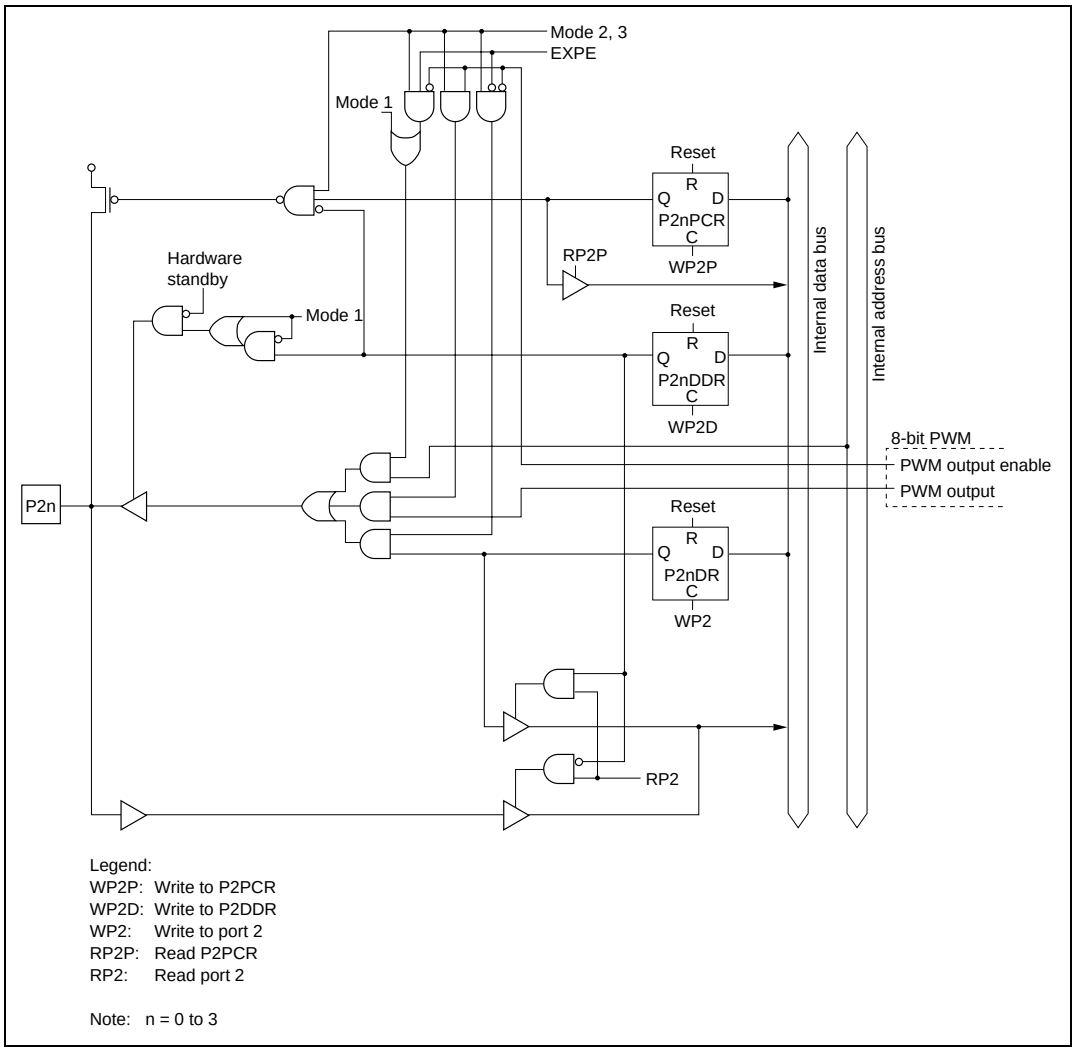


Figure C.2 Port 2 Block Diagram (Pins P20 to P23)

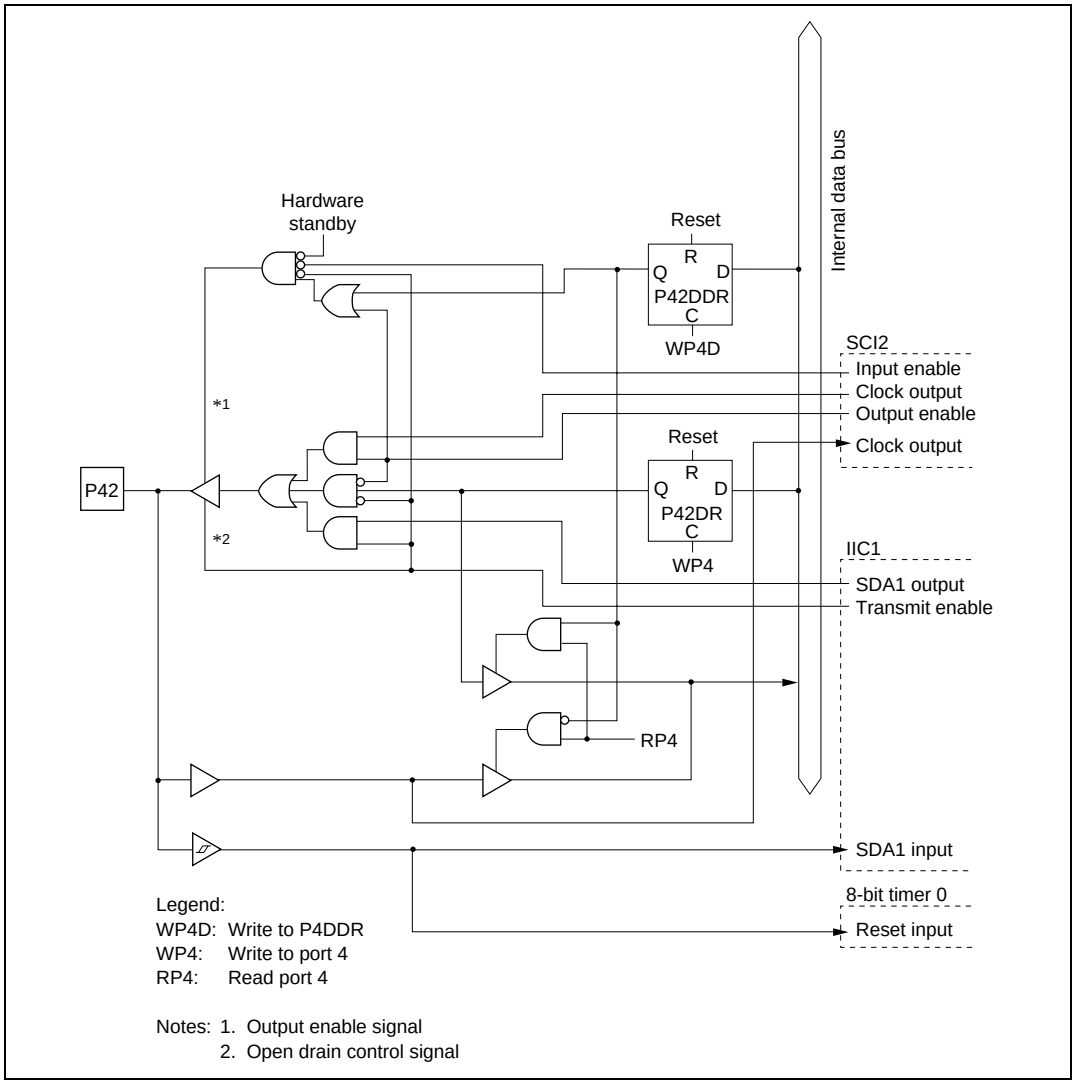


Figure C.8 Port 4 Block Diagram (Pin P42)