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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	10MHz
Connectivity	IrDA, SCI
Peripherals	POR, PWM, WDT
Number of I/O	58
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2134avtf10v

Item	Specifications
Bus controller	• 2-state or 3-state access space can be designated for external expansion areas • Number of program wait states can be set for external expansion areas
Data transfer controller (DTC) (H8S/2138 Group)	• Can be activated by internal interrupt or software • Multiple transfers or multiple types of transfer possible for one activation source • Transfer possible in repeat mode, block transfer mode, etc. • Request can be sent to CPU for interrupt that activated DTC
16-bit free-running timer module (FRT: 1 channel)	• One 16-bit free-running counter (also usable for external event counting) • Two output compare outputs • Four input capture inputs (with buffer operation capability)
8-bit timer module (2 channels: TMR0, TMR1)	Each channel has: • One 8-bit up-counter (also usable for external event counting) • Two time constant registers • The two channels can be connected
Timer connection and 8-bit timer (TMR) module (2 channels: TMRX, TMRY) (Timer connection and TMRX provided in H8S/2138 Group)	Input/output and FRT, TMR1, TMRX, TMRY can be interconnected • Measurement of input signal or frequency-divided waveform pulse width and cycle (FRT, TMR1) • Output of waveform obtained by modification of input signal edge (FRT, TMR1) • Determination of input signal duty cycle (TMRX) • Output of waveform synchronized with input signal (FRT, TMRX, TMRY) • Automatic generation of cyclical waveform (FRT, TMRY)
Watchdog timer module (WDT: 2 channels)	• Watchdog timer or interval timer function selectable • Subclock operation capability (channel 1 only)
8-bit PWM timer (PWM) (H8S/2138 Group)	• Up to 16 outputs • Pulse duty cycle settable from 0 to 100% • Resolution: 1/256 • 1.25 MHz maximum carrier frequency (20-MHz operation)

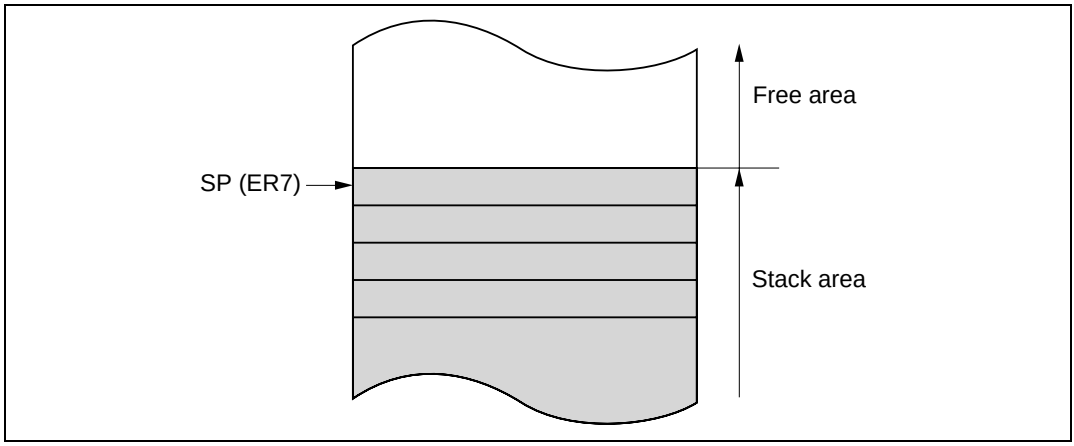


Figure 2.9 Stack

2.4.3 Control Registers

The control registers are the 24-bit program counter (PC), 8-bit extended control register (EXR), and 8-bit condition-code register (CCR).

(1) Program Counter (PC)

This 24-bit counter indicates the address of the next instruction the CPU will execute. The length of all CPU instructions is 2 bytes (one word), so the least significant PC bit is ignored. (When an instruction is fetched, the least significant PC bit is regarded as 0.)

(2) Extended Control Register (EXR)

An 8-bit register. In the H8S/2138 Group and H8S/2134 Group, this register does not affect operation.

Bit 7—Trace Bit (T): This bit is reserved. In the H8S/2138 Group and H8S/2134 Group, this bit does not affect operation.

Bits 6 to 3—Reserved: These bits are reserved. They are always read as 1.

Bits 2 to 0—Interrupt Mask Bits (I2 to I0): These bits are reserved. In the H8S/2138 Group and H8S/2134 Group, these bits do not affect operation.

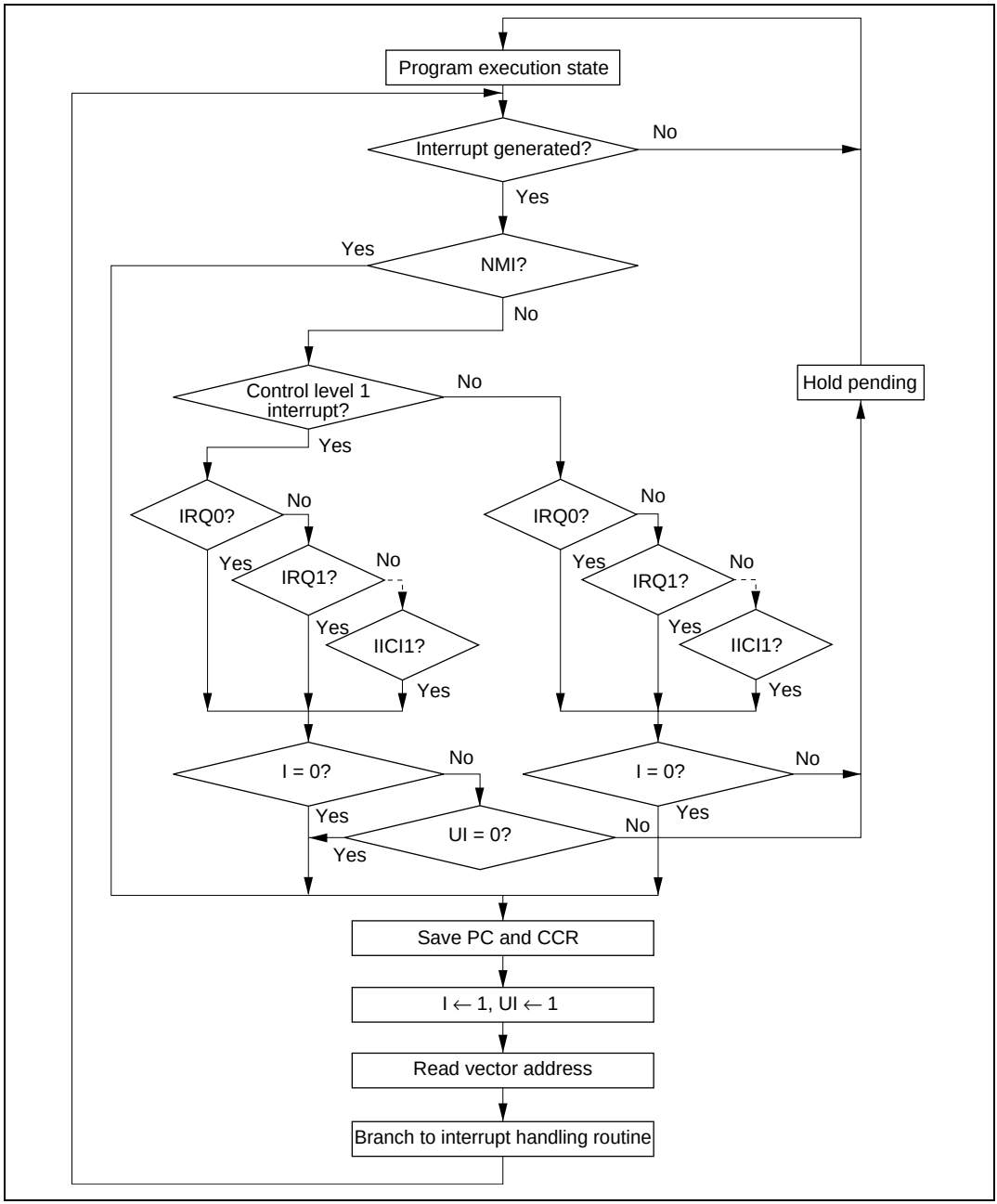


Figure 5.10 Flowchart of Procedure Up to Interrupt Acceptance in Interrupt Control Mode 1

Port	Description	Pins	Expanded Modes		Single-Chip Mode
			Mode 1	Mode 2, Mode 3 (EXPE = 1)	Mode 2, Mode 3 (EXPE = 0)
Port 6	• 8-bit I/O port	P67/$\overline{\text{IRQ7}}$/$\overline{\text{KIN7}}$/CIN7 P66/$\overline{\text{IRQ6}}$/FTOB/$\overline{\text{KIN6}}$/CIN6 P65/FTID/$\overline{\text{KIN5}}$/CIN5 P64/FTIC/$\overline{\text{KIN4}}$/CIN4 P63/FTIB/$\overline{\text{KIN3}}$/CIN3 P62/FTIA/TMIY/$\overline{\text{KIN2}}$/CIN2 P61/FTOA/$\overline{\text{KIN1}}$/CIN1 P60/FTCI/$\overline{\text{KIN0}}$/CIN0	I/O port also functioning as external interrupt input ($\overline{\text{IRQ7}}$, $\overline{\text{IRQ6}}$), FRT input/output (FTCI, FTOA, FTIA, FTIB, FTIC, FTID, FTOB), 8-bit timer Y input (TMIY), key-sense interrupt input ($\overline{\text{KIN7}}$ to $\overline{\text{KIN0}}$), and expansion A/D converter input (CIN7 to CIN0)		
Port 7	• 8-bit input port	P77/AN7/DA1 P76/AN6/DA0 P75/AN5 P74/AN4 P73/AN3 P72/AN2 P71/AN1 P70/AN0	Input port also functioning as A/D converter analog input (AN7 to AN0) and D/A converter analog output (DA1, DA0)		
Port 8	• 7-bit I/O port	P86/$\overline{\text{IRQ5}}$/SCK1 P85/$\overline{\text{IRQ4}}$/RxD1 P84/$\overline{\text{IRQ3}}$/TxD1 P83 P82 P81 P80	I/O port also functioning as external interrupt input ($\overline{\text{IRQ5}}$, $\overline{\text{IRQ4}}$, $\overline{\text{IRQ3}}$) and SCI1 input/output (TxD1, RxD1, SCK1)		

9.1.3 Pin Configuration

Table 9.1 shows the PWM output pin.

Table 9.1 Pin Configuration

Name	Abbreviation	I/O	Function
PWM output pin 0 to 15	PW0 to PW15	Output	PWM timer pulse output 0 to 15

9.1.4 Register Configuration

Table 9.2 lists the registers of the PWM timer module.

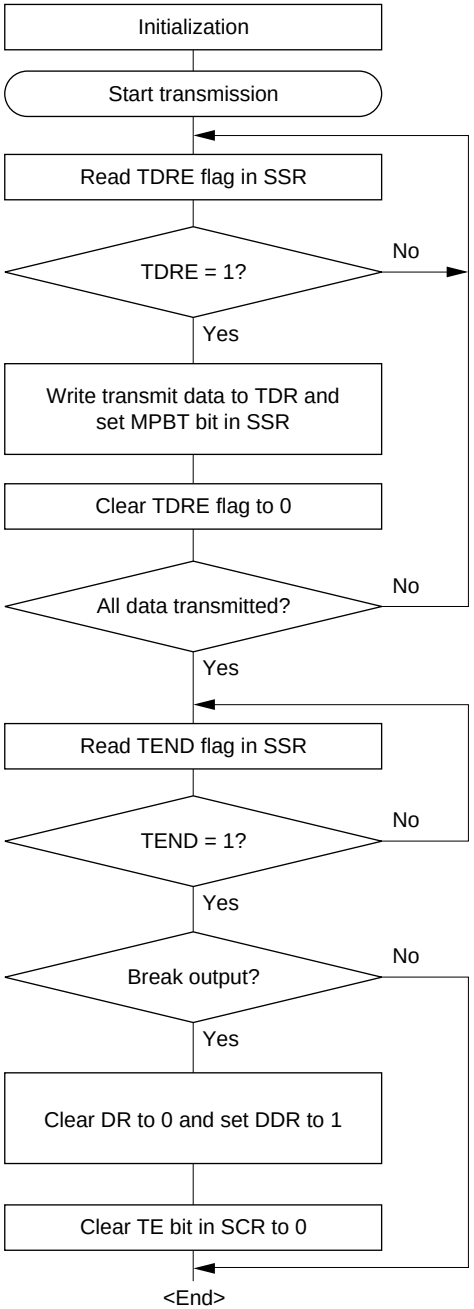
Table 9.2 PWM Timer Module Registers

Name	Abbreviation	R/W	Initial Value	Address*1
PWM register select	PWSL	R/W	H'20	H'FFD6
PWM data registers 0 to 15	PWDR0 to PWDR15	R/W	H'00	H'FFD7
PWM data polarity register A	PWDPRA	R/W	H'00	H'FFD5
PWM data polarity register B	PWDPRB	R/W	H'00	H'FFD4
PWM output enable register A	PWOERA	R/W	H'00	H'FFD3
PWM output enable register B	PWOERB	R/W	H'00	H'FFD2
Port 1 data direction register	P1DDR	W	H'00	H'FFB0
Port 2 data direction register	P2DDR	W	H'00	H'FFB1
Port 1 data register	P1DR	R/W	H'00	H'FFB2
Port 2 data register	P2DR	R/W	H'00	H'FFB3
Peripheral clock select register	PCSR	R/W	H'00	H'FF82*2
Module stop control register	MSTPCRH	R/W	H'3F	H'FF86
	MSTPCRL	R/W	H'FF	H'FF87

Notes: 1. Lower 16 bits of the address.
2. Some registers in the 8-bit timer are assigned in the same addresses as other registers. In this case, register selection is performed by the FLSHE bit in the serial timer control register (STCR).

	Operating Frequency φ (MHz)											
	φ = 6 MHz			φ = 6.144 MHz			φ = 7.3728 MHz			φ = 8 MHz		
Bit Rate (bits/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	106	–0.44	2	108	0.08	2	130	–0.07	2	141	0.03
150	2	77	0.16	2	79	0.00	2	95	0.00	2	103	0.16
300	1	155	0.16	1	159	0.00	1	191	0.00	1	207	0.16
600	1	77	0.16	1	79	0.00	1	95	0.00	1	103	0.16
1200	0	155	0.16	0	159	0.00	0	191	0.00	0	207	0.16
2400	0	77	0.16	0	79	0.00	0	95	0.00	0	103	0.16
4800	0	38	0.16	0	39	0.00	0	47	0.00	0	51	0.16
9600	0	19	–2.34	0	19	0.00	0	23	0.00	0	25	0.16
19200	0	9	–2.34	0	9	0.00	0	11	0.00	0	12	0.16
31250	0	5	0.00	0	5	2.40	—	—	—	0	7	0.00
38400	0	4	–2.34	0	4	0.00	0	5	0.00	—	—	—

	Operating Frequency φ (MHz)											
	φ = 9.8304 MHz			φ = 10 MHz			φ = 12 MHz			φ = 12.288 MHz		
Bit Rate (bits/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	174	–0.26	2	177	–0.25	2	212	0.03	2	217	0.08
150	2	127	0.00	2	129	0.16	2	155	0.16	2	159	0.00
300	1	255	0.00	2	64	0.16	2	77	0.16	2	79	0.00
600	1	127	0.00	1	129	0.16	1	155	0.16	1	159	0.00
1200	0	255	0.00	1	64	0.16	1	77	0.16	1	79	0.00
2400	0	127	0.00	0	129	0.16	0	155	0.16	0	159	0.00
4800	0	63	0.00	0	64	0.16	0	77	0.16	0	79	0.00
9600	0	31	0.00	0	32	–1.36	0	38	0.16	0	39	0.00
19200	0	15	0.00	0	15	1.73	0	19	–2.34	0	19	0.00
31250	0	9	–1.70	0	9	0.00	0	11	0.00	0	11	2.40
38400	0	7	0.00	0	7	1.73	0	9	–2.34	0	9	0.00



[1] SCI initialization:
The TxD pin is automatically designated as the transmit data output pin.
After the TE bit is set to 1, one frame of 1s is output and transmission is enabled.

[2] SCI status check and transmit data write:
Read SSR and check that the TDRE flag is set to 1, then write transmit data to TDR. Set the MPBT bit in SSR to 0 or 1. Finally, clear the TDRE flag to 0.

[3] Serial transmission continuation procedure:
To continue serial transmission, be sure to read 1 from the TDRE flag to confirm that writing is possible, then write data to TDR, and then clear the TDRE flag to 0. Checking and clearing of the TDRE flag is automatic when the DTC is activated by a transmit-data-empty interrupt (TXI) request, and data is written to TDR.

[4] Break output at the end of serial transmission:
To output a break in serial transmission, set the port DDR to 1, clear DR to 0, then clear the TE bit in SCR to 0.

Figure 15.10 Sample Multiprocessor Serial Transmission Flowchart

Bit 4

AASX	Description	
0	Second slave address not recognized	(Initial value)
	[Clearing conditions]	
	1. When 0 is written in AASX after reading AASX = 1	
	2. When a start condition is detected	
	3. In master mode	
1	Second slave address recognized	
	[Setting condition]	
	When the second slave address is detected in slave receive mode while FSX = 0	

Bit 3—Arbitration Lost (AL): This flag indicates that arbitration was lost in master mode. The I²C bus interface monitors the bus. When two or more master devices attempt to seize the bus at nearly the same time, if the I²C bus interface detects data differing from the data it sent, it sets AL to 1 to indicate that the bus has been taken by another master.

AL is cleared by reading AL after it has been set to 1, then writing 0 in AL. In addition, AL is reset automatically by write access to ICDR in transmit mode, or read access to ICDR in receive mode.

Bit 3

AL	Description	
0	Bus arbitration won	(Initial value)
	[Clearing conditions]	
	1. When ICDR data is written (transmit mode) or read (receive mode)	
	2. When 0 is written in AL after reading AL = 1	
1	Arbitration lost	
	[Setting conditions]	
	1. If the internal SDA and SDA pin disagree at the rise of SCL in master transmit mode	
	2. If the internal SCL line is high at the fall of SCL in master transmit mode	

Bit 2—Slave Address Recognition Flag (AAS): In I²C bus format slave receive mode, this flag is set to 1 if the first frame following a start condition matches bits SVA6 to SVA0 in SAR, or if the general call address (H'00) is detected.

16.3.7 Automatic Switching from Formatless Mode to I²C Bus Format

Setting the SW bit to 1 in DDCSWR enables formatless mode to be selected as the IIC0 operating mode. Switching from formatless mode to the I²C bus format (slave mode) is performed automatically when a falling edge is detected on the SCL pin.

The following four preconditions are necessary for this operation:

- A common data pin (SDA) for formatless and I²C bus format operation
- Separate clock pins for formatless operation (VSYNCI) and I²C bus format operation (SCL)
- A fixed 1 level for the SCL pin during formatless operation (the SCL pin does not output a low level)
- Settings of bits other than TRS in ICCR that allow I²C bus format operation

Automatic switching is performed from formatless mode to the I²C bus format when the SW bit in DDCSWR is automatically cleared to 0 on detection of a falling edge on the SCL pin. Switching from the I²C bus format to formatless mode is achieved by having software set the SW bit in DDCSWR to 1.

In formatless mode, bits (such as MSL and TRS) that control the I²C bus interface operating mode must not be modified. When switching from the I²C bus format to formatless mode, set the TRS bit to 1 or clear it to 0 according to the transmit data (transmission or reception) in formatless mode, then set the SW bit to 1. After automatic switching from formatless mode to the I²C bus format (slave mode), in order to wait for slave address reception, the TRS bit is automatically cleared to 0.

If a falling edge is detected on the SCL pin during formatless operation, I²C bus interface operating mode is switched to the I²C bus format without waiting for a stop condition to be detected.

The value of the BBSY bit cannot be modified directly by this module clear function, but since the stop condition pin waveform is generated according to the state and release timing of the SCL and SDA pins, the BBSY bit may be cleared as a result. Similarly, state switching of other bits and flags may also have an effect.

To prevent problems caused by these factors, the following procedure should be used when initializing the IIC state.

1. Execute initialization of the internal state according to the setting of bits CLR3 to CLR0 or ICE bit clearing.
2. Execute a stop condition issuance instruction (write 0 to BBSY and SCP) to clear the BBSY bit to 0, and wait for two transfer rate clock cycles.
3. Re-execute initialization of the internal state according to the setting of bits CLR3 to CLR0 or ICE bit clearing.
4. Initialize (re-set) the IIC registers.

16.4 Usage Notes

- In master mode, if an instruction to generate a start condition is immediately followed by an instruction to generate a stop condition, neither condition will be output correctly. To output consecutive start and stop conditions, after issuing the instruction that generates the start condition, read the relevant ports, check that SCL and SDA are both low, then issue the instruction that generates the stop condition. Note that SCL may not yet have gone low when BBSY is cleared to 0.

- Either of the following two conditions will start the next transfer. Pay attention to these conditions when reading or writing to ICDR.
  - Write access to ICDR when ICE = 1 and TRS = 1 (including automatic transfer from ICDRT to ICDRS)
  - Read access to ICDR when ICE = 1 and TRS = 0 (including automatic transfer from ICDRS to ICDRR)

- Table 16.6 shows the timing of SCL and SDA output in synchronization with the internal clock. Timings on the bus are determined by the rise and fall times of signals affected by the bus load capacitance, series resistance, and parallel resistance.

Section 18 D/A Converter

18.1 Overview

The H8S/2138 Group and H8S/2134 Group have an on-chip D/A converter module with two channels.

18.1.1 Features

Features of the D/A converter module are listed below.

- Eight-bit resolution
- Two-channel output
- Maximum conversion time: 10 µs (with 20-pF load capacitance)
- Output voltage: 0 V to AV_{CC}
- D/A output retention in software standby mode

21.5.3 Erase Block Registers 1 and 2 (EBR1, EBR2)

Bit	7	6	5	4	3	2	1	0
EBR1	—	—	—	—	—	—	EB9/—*2	EB8/—*2
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	—	—	R/W*1 *2	R/W*1 *2

Bit	7	6	5	4	3	2	1	0
EBR2	EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W*1	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Notes: 1. In normal mode, these bits cannot be modified and are always read as 0.
2. Bits EB8 and EB9 are not present in the 64-kbyte versions; These bits must not be set to 1.

EBR1 and EBR2 are registers that specify the flash memory erase area block by block; bits 1 and 2 in EBR1 (128 kB versions only) and bits 7 to 0 in EBR2 are readable/writable bits. EBR1 and EBR2 are each initialized to H'00 by a reset, in hardware standby mode, software standby mode, subactive mode, subsleep mode, and watch mode, and the SWE bit in FLMCR1 is not set. When a bit in EBR1 or EBR2 is set, the corresponding block can be erased. Other blocks are erase-protected. Set only one bit in EBR1 or EBR2 (more than one bit cannot be set). When on-chip flash memory is disabled, a read will return H'00, and writes are invalid.

The flash memory block configuration is shown in table 21.5.

22.10.8 Status Polling

- The FO7 status polling flag indicates the operating status in auto-program or auto-erase mode.
- The FO6 status polling flag indicates a normal or abnormal end in auto-program or auto-erase mode.

Table 22.20 Status Polling Output Truth Table

Pin Names	Internal Operation in Progress	Abnormal End	—	Normal End
FO7	0	1	0	1
FO6	0	0	1	1
FO0 to FO5	0	0	0	0

22.10.9 Programmer Mode Transition Time

Commands cannot be accepted during the oscillation stabilization period or the programmer mode setup period. After the programmer mode setup time, a transition is made to memory read mode.

Table 22.21 Command Wait State Transition Time Specifications

Item	Symbol	Min	Max	Unit
Standby release (oscillation stabilization time)	t_{osc1}	20	—	ms
Programmer mode setup time	t_{bmv}	10	—	ms
V_{CC} hold time	t_{dwn}	0	—	ms

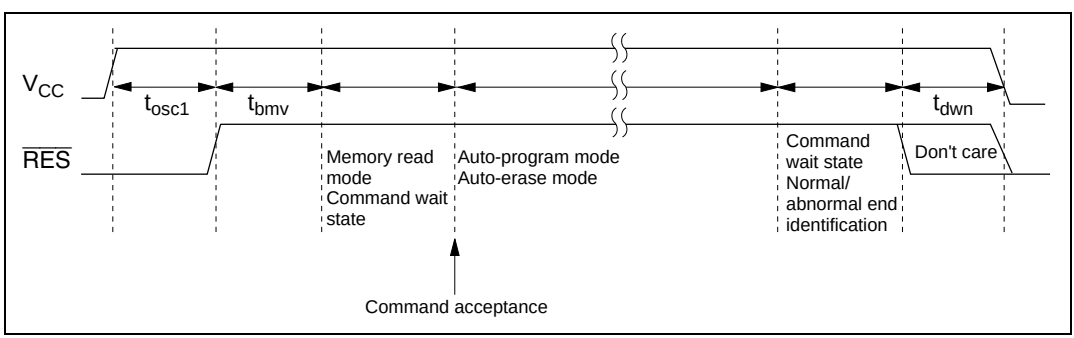


Figure 22.23 Oscillation Stabilization Time, Programmer Mode Setup Time, and Power Supply Fall Sequence

In order to retain on-chip RAM data, the RAME bit in SYSCR should be cleared to 0 before driving the $\overline{\text{STBY}}$ pin low.

Do not change the state of the mode pins (MD1 and MD0) while the chip is in hardware standby mode.

Hardware standby mode is cleared by means of the $\overline{\text{STBY}}$ pin and the $\overline{\text{RES}}$ pin. When the $\overline{\text{STBY}}$ pin is driven high while the $\overline{\text{RES}}$ pin is low, the reset state is set and clock oscillation is started. Ensure that the $\overline{\text{RES}}$ pin is held low until the clock oscillation settles (at least 8 ms—the oscillation settling time—when using a crystal oscillator). When the $\overline{\text{RES}}$ pin is subsequently driven high, a transition is made to the program execution state via the reset exception handling state.

24.7.2 Hardware Standby Mode Timing

Figure 24.4 shows an example of hardware standby mode timing.

When the $\overline{\text{STBY}}$ pin is driven low after the $\overline{\text{RES}}$ pin has been driven low, a transition is made to hardware standby mode. Hardware standby mode is cleared by driving the $\overline{\text{STBY}}$ pin high, waiting for the oscillation settling time, then changing the $\overline{\text{RES}}$ pin from low to high.

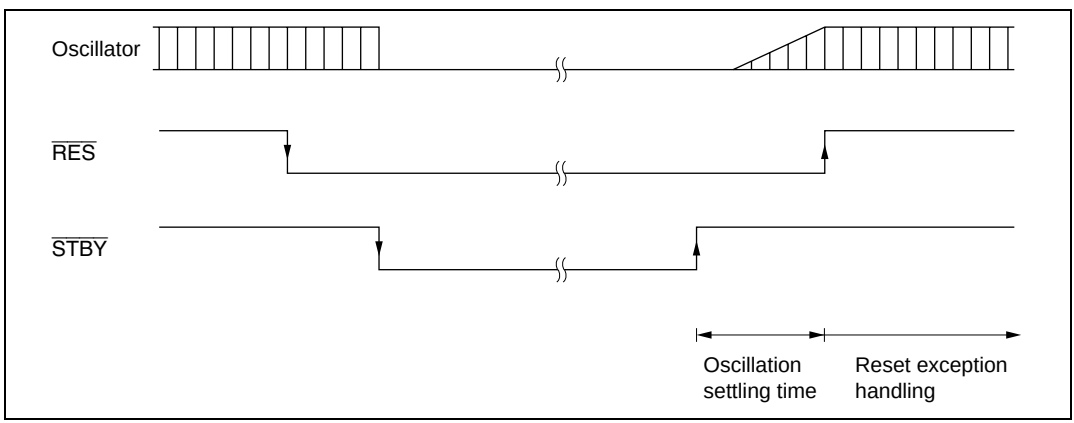


Figure 24.4 Hardware Standby Mode Timing

25.3 Electrical Characteristics of H8S/2138 F-ZTAT (A-Mask Version), and Mask ROM Versions of H8S/2138 and H8S/2137

25.3.1 Absolute Maximum Ratings

Table 25.15 lists the absolute maximum ratings.

Table 25.15 Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power supply voltage*1	V_{CC}	–0.3 to +7.0	V
Power supply voltage*1 (3-V version)	V_{CC}	–0.3 to +4.3	V
Power supply voltage*2 (VCL pin)	V_{CL}	–0.3 to +4.3	V
Input voltage (except ports 6 and 7)	V_{in}	–0.3 to V_{CC} +0.3	V
Input voltage (CIN input not selected for port 6)	V_{in}	–0.3 to V_{CC} +0.3	V
Input voltage (CIN input selected for port 6)	V_{in}	Lower voltage of –0.3 to V_{CC} +0.3 and AV_{CC} +0.3	V
Input voltage (port 7)	V_{in}	–0.3 to AV_{CC} +0.3	V
Analog power supply voltage	AV_{CC}	–0.3 to +7.0	V
Analog power supply voltage (3-V version)	AV_{CC}	–0.3 to +4.3	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} +0.3	V
Operating temperature	T_{opr}	Regular specifications: –20 to +75	°C
		Wide-range specifications: –40 to +85	°C
Operating temperature (flash memory programming/erasing)	T_{opr}	Regular specifications: –20 to +75	°C
		Wide-range specifications: –40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution: 1. Permanent damage to the chip may result if absolute maximum ratings are exceeded.
2. Never apply more than 7.0 V to any of the pins of the 5- or 4-V version or 4.3 V to any of the pins of the 3-V version.

Notes: 1. Voltage applied to the VCC1 pin.
Never exceed the maximum rating of V_{CL} in the low-power version (3-V version) because both the VCC1 and V_{CL} pins are connected to the V_{CC} power supply.
2. It is an operating power supply voltage pin on the chip.
Never apply power supply voltage to the V_{CL} pin in the 5- or 4-V version.
Always connect an external capacitor between the V_{CL} pin and ground for internal voltage stabilization.

Notes: 1. Set the times according to the program/erase algorithms.

2. Programming time per 128 bytes (Shows the total period for which the P-bit in the flash memory control register (FLMCR1) is set. It does not include the programming verification time.)
3. Block erase time (shows the total period for which the E-bit in FLMCR1 is set. It does not include the erase verification time.)
4. Maximum programming time (tP (max))

   tP (max) = (wait time after P-bit setting (z1) + (z3)) × 6 + wait time after P-bit setting (z2) × ((N) – 6)
5. Maximum programming count (N) should be set according to the actual set value of (z1, z2, z3) to allow programming within the maximum programming time (tP (max)). The wait time after P-bit setting (z1, z2, z3) must be changed with the value of the number of writing times (n) as follows.

   The number of times for writing n

   $1 \leq n \leq 6$ z1 = 30 µs, z3 = 10 µs

   $7 \leq n \leq 1000$ z2 = 200 µs
6. Maximum erase time (tE (max))

   tE (max) = waiting time after E-bit setting (z) × Maximum erase count (N)
7. Maximum erase count (N) should be set according to the actual setting (z) to allow erase within the maximum erase time (tE (max)).
8. Minimum number of times for which all characteristics are guaranteed after rewriting (Guarantee range is 1 to minimum value).
9. Reference value for 25°C (as a guideline, rewriting should normally function up to this value).
10. Data retention characteristic when rewriting is performed within the specification range, including the minimum value.

Instruction	1	2	3	4	5	6	7	8	9
BMI d:8	R:W NEXT	R:W EA							
BGE d:8	R:W NEXT	R:W EA							
BLT d:8	R:W NEXT	R:W EA							
BGT d:8	R:W NEXT	R:W EA							
BLE d:8	R:W NEXT	R:W EA							
BRA d:16 (BT d:16)	R:W 2nd	Internal operation, 1 state	R:W EA						
BRN d:16 (BF d:16)	R:W 2nd	Internal operation, 1 state	R:W EA						
BHI d:16	R:W 2nd	Internal operation, 1 state	R:W EA						
BLS d:16	R:W 2nd	Internal operation, 1 state	R:W EA						
BCC d:16 (BHS d:16)	R:W 2nd	Internal operation, 1 state	R:W EA						
BCS d:16 (BLO d:16)	R:W 2nd	Internal operation, 1 state	R:W EA						
BNE d:16	R:W 2nd	Internal operation, 1 state	R:W EA						
BEQ d:16	R:W 2nd	Internal operation, 1 state	R:W EA						
BVC d:16	R:W 2nd	Internal operation, 1 state	R:W EA						
BVS d:16	R:W 2nd	Internal operation, 1 state	R:W EA						
BPL d:16	R:W 2nd	Internal operation, 1 state	R:W EA						
BMI d:16	R:W 2nd	Internal operation, 1 state	R:W EA						
BGE d:16	R:W 2nd	Internal operation, 1 state	R:W EA						

Instruction		1	2	3	4	5	6	7	8	9
CMP.B #xx:8,Rd		R:W NEXT								
CMP.B Rs,Rd		R:W NEXT								
CMP.W #xx:16,Rd		R:W 2nd	R:W NEXT							
CMP.W Rs,Rd		R:W NEXT								
CMP.L #xx:32,ERd		R:W 2nd	R:W 3rd	R:W NEXT						
CMP.L ERs,ERd		R:W NEXT								
DAA Rd		R:W NEXT								
DAS Rd		R:W NEXT								
DEC.B Rd		R:W NEXT								
DEC.W #1/2,Rd		R:W NEXT								
DEC.L #1/2,ERd		R:W NEXT								
DIVXS.B Rs,Rd		R:W 2nd	R:W NEXT	Internal operation, 11 states						
DIVXS.W Rs,ERd		R:W 2nd	R:W NEXT	Internal operation, 19 states						
DIVXU.B Rs,Rd		R:W NEXT	Internal operation, 11 states							
DIVXU.W Rs,ERd		R:W NEXT	Internal operation, 19 states							
EEPMOV.B		R:W 2nd	R:B EAs*1	R:B EAd*1	R:B EAs*2	W:B EAd*2	R:W NEXT			
EEPMOV.W		R:W 2nd	R:B EAs*1	R:B EAd*1	R:B EAs*2	W:B EAd*2	R:W NEXT			
EXTS.W Rd		R:W NEXT			← Repeated n times*2 →					
EXTS.L ERd		R:W NEXT								
EXTU.W Rd		R:W NEXT								
EXTU.L ERd		R:W NEXT								
INC.B Rd		R:W NEXT								
INC.W #1/2,Rd		R:W NEXT								
INC.L #1/2,ERd		R:W NEXT								
JMP @ERn		R:W NEXT	R:W EA							
JMP @aa:24		R:W 2nd	Internal operation, 1 state	R:W EA						
JMP @@aa:8	Advanced	R:W NEXT	R:W:M aa:8	R:W aa:8	Internal operation, 1 state	R:W EA				
JSR @ERn	Advanced	R:W NEXT	R:W EA	W:W:M Stack (H)	W:W Stack (L)					
JSR @aa:24	Advanced	R:W 2nd	Internal operation, 1 state	R:W EA	W:W:M Stack (H)	W:W Stack (L)				
JSR @@aa:8	Advanced	R:W NEXT	R:W:M aa:8	R:W aa:8	W:W:M Stack (H)	W:W Stack (L)	R:W EA			

P9DDR—Port 9 Data Direction Register **H'FFC0** **Port 9**

Bit	7	6	5	4	3	2	1	0
	P97DDR	P96DDR	P95DDR	P94DDR	P93DDR	P92DDR	P91DDR	P90DDR
Mode 1								
Initial value	0	1	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W
Modes 2 and 3								
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Specification of input or output for port 9 pins

P9DR—Port 9 Data Register **H'FFC1** **Port 9**

Bit	7	6	5	4	3	2	1	0
	P97DR	P96DR	P95DR	P94DR	P93DR	P92DR	P91DR	P90DR
Initial value	0	—*	0	0	0	0	0	0
Read/Write	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

Output data for port 9 pins

Note: * Determined by state of pin P96.

IER—IRQ Enable Register **H'FFC2** **Interrupt Controller**

Bit	7	6	5	4	3	2	1	0
	IRQ7E	IRQ6E	IRQ5E	IRQ4E	IRQ3E	IRQ2E	IRQ1E	IRQ0E
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IRQ7 to IRQ0 enable

0	IRQn interrupt disabled
1	IRQn interrupt enabled

(n = 7 to 0)

ADCSR—A/D Control/Status Register H'FFE8 A/D Converter

Bit	7	6	5	4	3	2	1	0
	ADF	ADIE	ADST	SCAN	CKS	CH2	CH1	CH0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Channel select

Group selection	Channel selection		Description	
CH2	CH1	CH0	Single mode	Scan mode
0	0	0	AN0	AN0
		1	AN1	AN0, AN1
	1	0	AN2	AN0, AN1, AN2
		1	AN3	AN0, AN1, AN2, AN3
1	0	0	AN4	AN4
		1	AN5	AN4, AN5
	1	0	AN6 or CIN0–CIN7	AN4, AN5, AN6 or CIN0–CIN7
		1	AN7	AN4, AN5, AN6 or CIN0–CIN7, AN7

Clock select

0	Conversion time = 266 states (max.)
1	Conversion time = 134 states (max.)

Scan mode

0	Single mode
1	Scan mode

A/D start

0	A/D conversion stopped
1	• Single mode: A/D conversion is started. Cleared to 0 automatically when conversion on the specified channel ends • Scan mode: A/D conversion is started. Conversion continues sequentially on the selected channels until ADST is cleared to 0 by software, a reset, or a transition to standby mode or module stop mode

A/D interrupt enable

0	A/D conversion end interrupt (ADI) request disabled
1	A/D conversion end interrupt (ADI) request enabled

A/D end flag

0	[Clearing conditions] • When 0 is written in the to ADF flag after reading ADF = 1 • When the DTC is activated by an ADI interrupt, and ADDR is read
1	[Setting conditions] • Single mode: When A/D conversion ends • Scan mode: When A/D conversion ends on all specified channels

Note: * Only 0 can be written, to clear the flag.