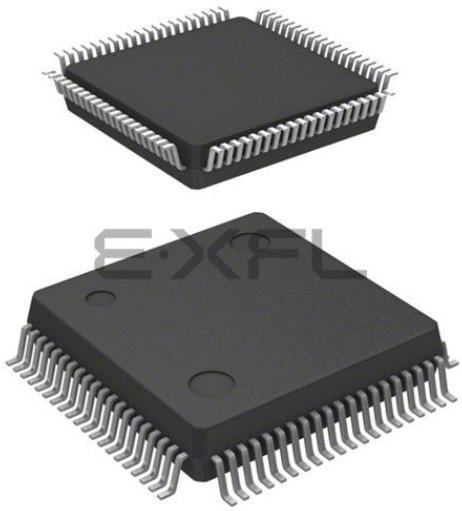

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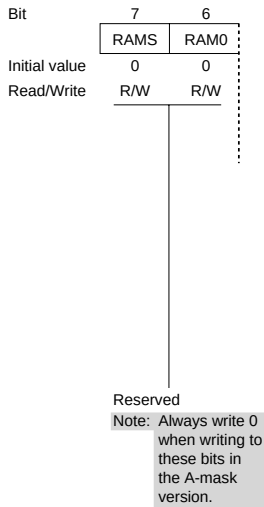
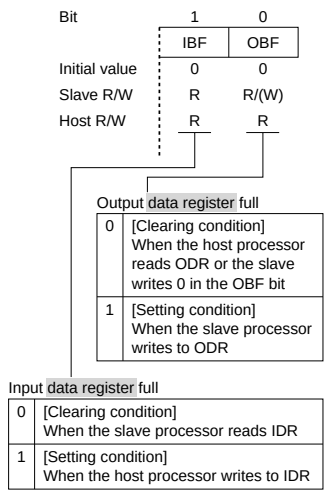
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	IrDA, SCI
Peripherals	POR, PWM, WDT
Number of I/O	58
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2134fa20v

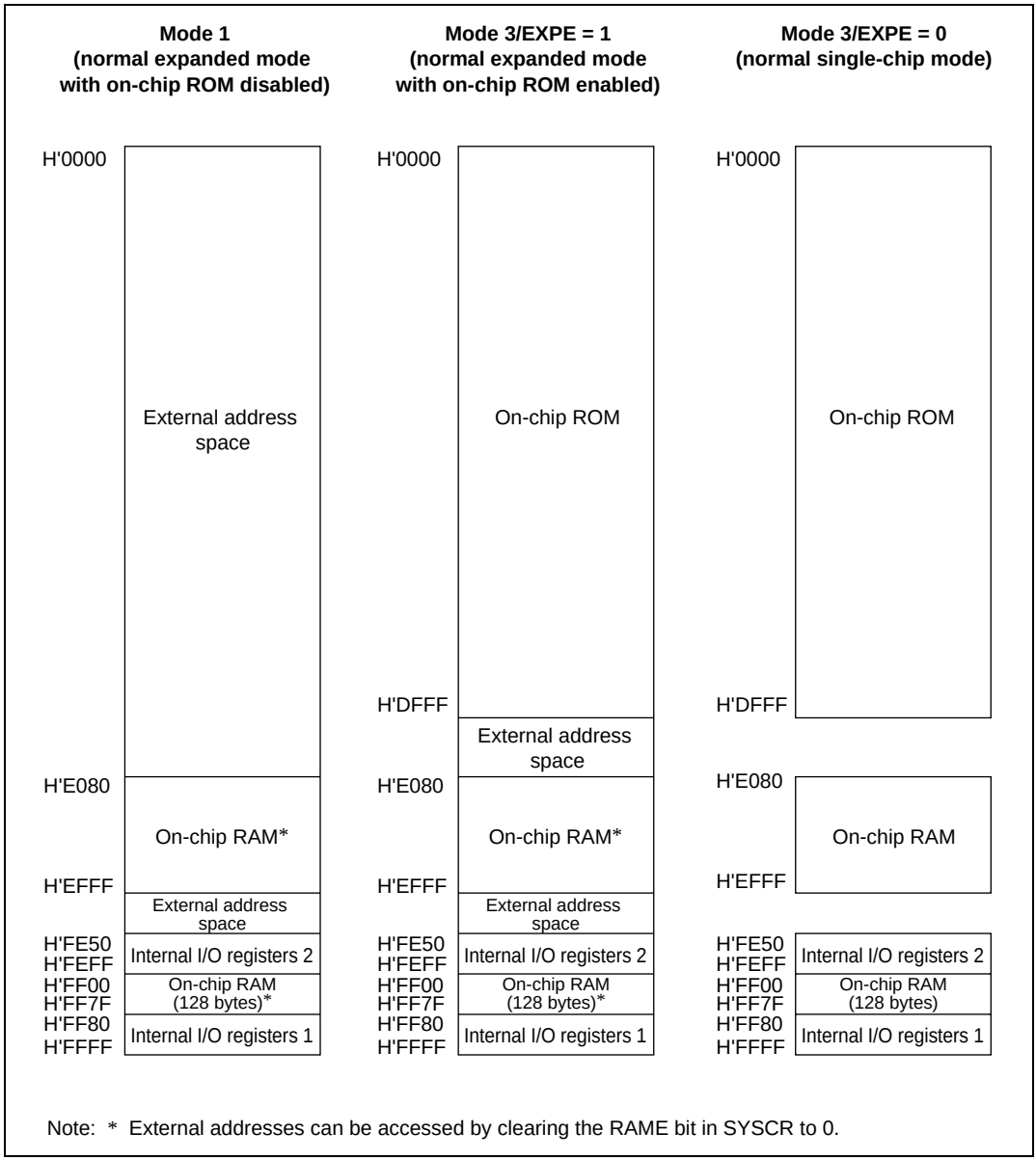
Item	Page	Revision (See Manual for Details)
B.3 Function	942	WSCR H'FFC7 Bus Controller Figure amended



	959	STR1, 2 H'FFF6, H'FFFE HIF Figure amended



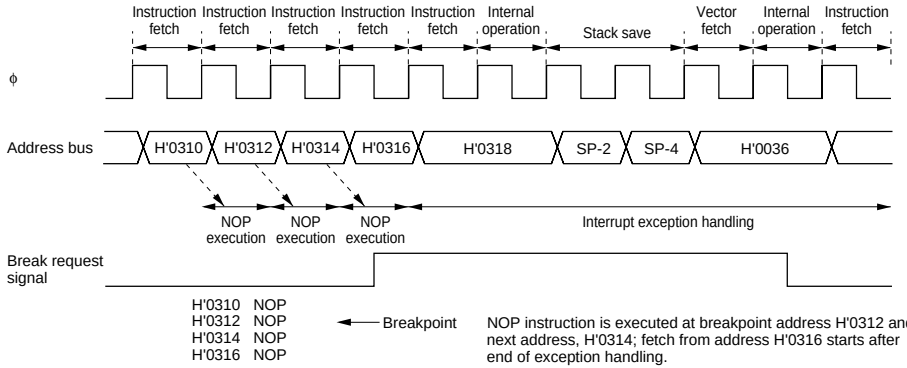
Pin No.	Pin Name			
	Expanded Modes		Single-Chip Modes	Flash Memory Programmer Mode
FP-80A TFP-80C	Mode 1	Mode 2 (EXPE = 1) Mode 3 (EXPE = 1)	Mode 2 (EXPE = 0) Mode 3 (EXPE = 0)	
45	P46/PWX0	P46/PWX0	P46/PWX0	NC
46	P47/PWX1	P47/PWX1	P47/PWX1	NC
47	VCC1	VCC1	VCC1	VCC
48	A15	A15/P27/PW15/ CBLANK	P27/PW15/ CBLANK	$\overline{CE}$
49	A14	A14/P26/PW14	P26/PW14	FA14
50	A13	A13/P25/PW13	P25/PW13	FA13
51	A12	A12/P24/PW12	P24/PW12	FA12
52	A11	A11/P23/PW11	P23/PW11	FA11
53	A10	A10/P22/PW10	P22/PW10	FA10
54	A9	A9/P21/PW9	P21/PW9	$\overline{OE}$
55	A8	A8/P20/PW8	P20/PW8	FA8
56	VSS	VSS	VSS	VSS
57	A7	A7/P17/PW7	P17/PW7	FA7
58	A6	A6/P16/PW6	P16/PW6	FA6
59	A5	A5/P15/PW5	P15/PW5	FA5
60	A4	A4/P14/PW4	P14/PW4	FA4
61	A3	A3/P13/PW3	P13/PW3	FA3
62	A2	A2/P12/PW2	P12/PW2	FA2
63	A1	A1/P11/PW1	P11/PW1	FA1
64	A0	A0/P10/PW0	P10/PW0	FA0
65	D0	D0	P30/HDB0	FO0
66	D1	D1	P31/HDB1	FO1
67	D2	D2	P32/HDB2	FO2
68	D3	D3	P33/HDB3	FO3
69	D4	D4	P34/HDB4	FO4
70	D5	D5	P35/HDB5	FO5
71	D6	D6	P36/HDB6	FO6
72	D7	D7	P37/HDB7	FO7
73	VSS	VSS	VSS	VSS
74	P80	P80	P80/HA0	NC



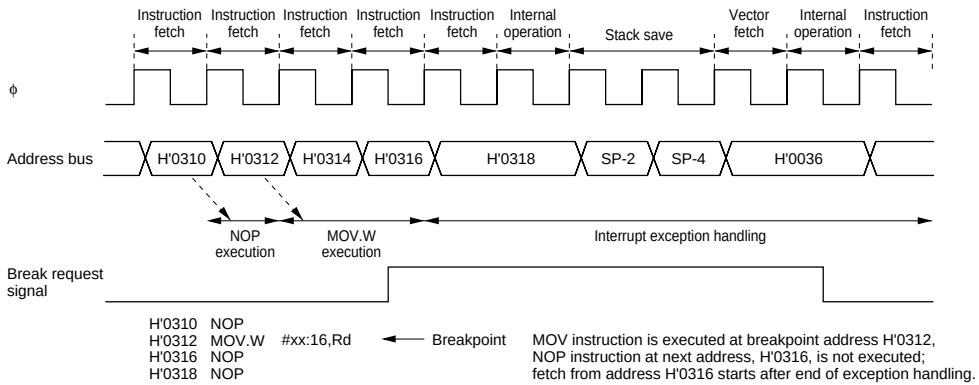
Note: * External addresses can be accessed by clearing the RAME bit in SYSCR to 0.

Figure 3.3 H8S/2133 Memory Map in Each Operating Mode

- Program area in on-chip memory, 1-state execution instruction at specified break address



- Program area in on-chip memory, 2-state execution instruction at specified break address



- Program area in external memory (2-state access, 16-bit-bus access), 1-state execution instruction at specified break address

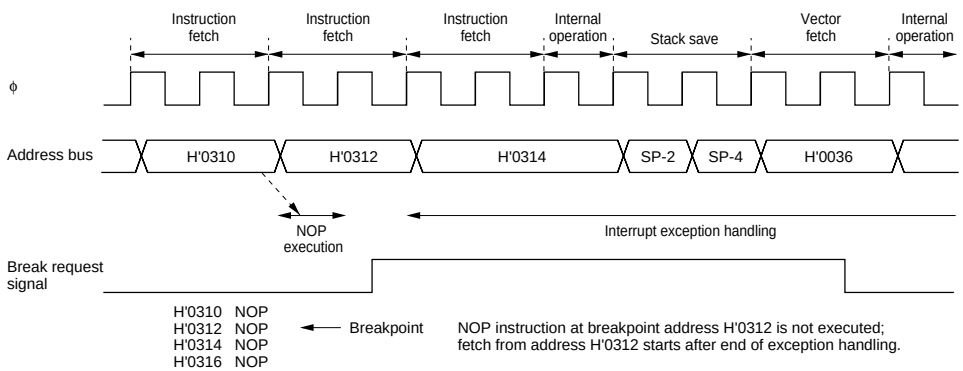


Figure 5.6 Examples of Address Break Timing

6.1.3 Pin Configuration

Table 6.1 summarizes the pins of the bus controller.

Table 6.1 Bus Controller Pins

Name	Symbol	I/O	Function
Address strobe	$\overline{AS}$	Output	Strobe signal indicating that address output on address bus is enabled (when IOSE bit is 0)
I/O select	$\overline{IOS}$	Output	I/O select signal (when IOSE bit is 1)
Read	$\overline{RD}$	Output	Strobe signal indicating that external space is being read
Write	$\overline{WR}$	Output	Strobe signal indicating that external space is being written to, and that data bus is enabled
Wait	$\overline{WAIT}$	Input	Wait request signal when external 3-state access space is accessed

6.1.4 Register Configuration

Table 6.2 summarizes the registers of the bus controller.

Table 6.2 Bus Controller Registers

Name	Abbreviation	R/W	Initial Value	Address*
Bus control register	BCR	R/W	H'D7	H'FFC6
Wait state control register	WSCR	R/W	H'33	H'FFC7

Note: * Lower 16 bits of the address.

6.3.4 I/O Select Signal

In the H8S/2138 Group and H8S/2134 Group, an I/O select signal ($\overline{IOS}$) can be output, with the signal output going low when the designated external space is accessed.

Figure 6.2 shows an example of $\overline{IOS}$ signal output timing.

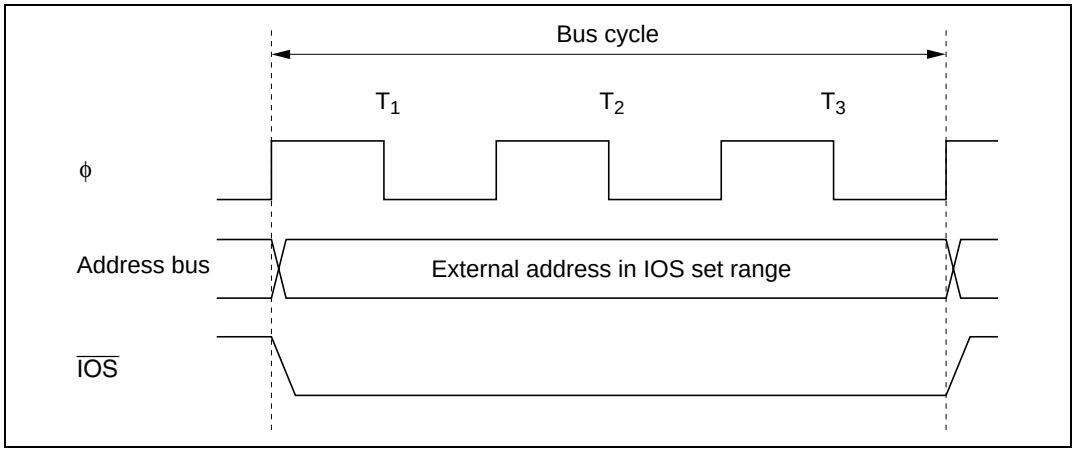


Figure 6.2 $\overline{IOS}$ Signal Output Timing

Enabling or disabling of $\overline{IOS}$ signal output is controlled by the setting of the IOSE bit in SYSCR. In expanded mode, this pin operates as the $\overline{AS}$ output pin after a reset, and therefore the IOSE bit in SYSCR must be set to 1 in order to use this pin as the $\overline{IOS}$ signal output. See section 8, I/O Ports, for details.

The range of addresses for which the $\overline{IOS}$ signal is output can be set with bits IOS1 and IOS0 in BCR. The $\overline{IOS}$ signal address ranges are shown in table 6.4.

Table 6.4 $\overline{IOS}$ Signal Output Range Settings

IOS1	IOS0	$\overline{IOS}$ Signal Output Range	
0	0	H'(FF)F000 to H'(FF)F03F	
	1	H'(FF)F000 to H'(FF)F0FF	
1	0	H'(FF)F000 to H'(FF)F3FF	
	1	H'(FF)F000 to H'(FF)FE4F*	(Initial value)

Note: * In the H8S/2138 F-ZTAT A-mask version, the address range is from H'(FF)F000 to H'(FF)F7FF.

9.1.2 Block Diagram

Figure 9.1 shows a block diagram of the PWM timer module.

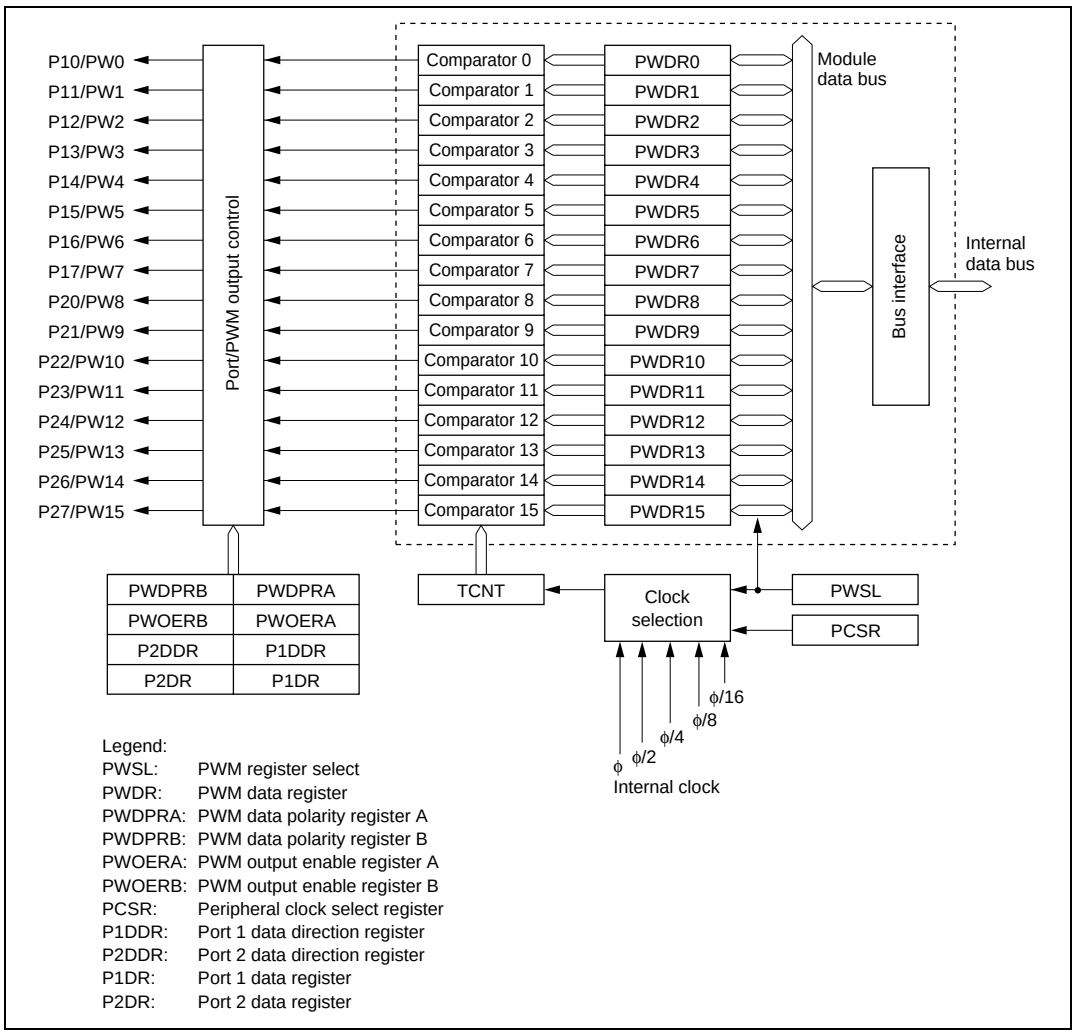


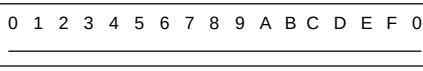
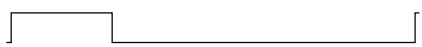
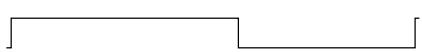
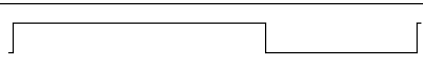
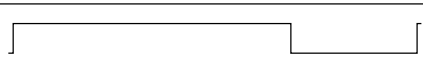
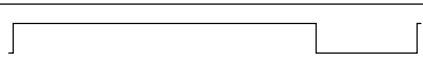
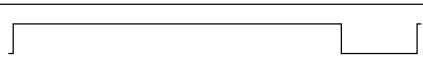
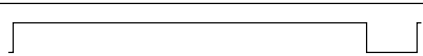
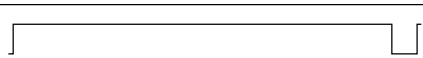
Figure 9.1 Block Diagram of PWM Timer Module

9.3 Operation

9.3.1 Correspondence between PWM Data Register Contents and Output Waveform

The upper 4 bits of PWDR specify the duty cycle of the basic pulse as 0/16 to 15/16 with a resolution of 1/16, as shown in table 9.4.

Table 9.4 Duty Cycle of Basic Pulse

Upper 4 Bits	Basic Pulse Waveform (Internal)
0000	
0001	
0010	
0011	
0100	
0101	
0110	
0111	
⋮	
1000	
1001	
1010	
1011	
1100	
1101	
1110	
1111	

12.4 Interrupt Sources

The TMR0, TMR1, and TMRY 8-bit timers can generate three types of interrupt: compare-match A and B (CMIA and CMIB), and overflow (OVI). TMRX can generate only an ICIX interrupt. An interrupt is requested when the corresponding interrupt enable bit is set in TCR or TCSR. Independent signals are sent to the interrupt controller for each interrupt. It is also possible to activate the DTC by means of CMIA and CMIB interrupts from TMR0, TMR1, and TMRY.

An overview of 8-bit timer interrupt sources is given in tables 12.4 to 12.6.

Table 12.4 TMR0 and TMR1 8-Bit Timer Interrupt Sources

Interrupt source	Description	DTC Activation	Interrupt Priority
CMIA	Requested by CMFA	Possible	High
CMIB	Requested by CMFB	Possible	↑
OVI	Requested by OVF	Not possible	Low

Table 12.5 TMRX 8-Bit Timer Interrupt Source

Interrupt source	Description	DTC Activation
ICIX	Requested by ICF	Not possible

Table 12.6 TMRY 8-Bit Timer Interrupt Sources

Interrupt source	Description	DTC Activation	Interrupt Priority
CMIA	Requested by CMFA	Possible	High
CMIB	Requested by CMFB	Possible	↑
OVI	Requested by OVF	Not possible	Low

Section 14 Watchdog Timer (WDT)

14.1 Overview

The H8S/2138 Group and H8S/2134 Group have an on-chip watchdog timer with two channels (WDT0, WDT1) for monitoring system operation. The WDT outputs an overflow signal if a system crash prevents the CPU from writing to the timer counter, allowing it to overflow. At the same time, the WDT can also generate an internal reset signal or internal NMI interrupt signal.

When this watchdog function is not needed, the WDT can be used as an interval timer. In interval timer mode, an interval timer interrupt is generated each time the counter overflows.

14.1.1 Features

WDT features are listed below.

- Switchable between watchdog timer mode and interval timer mode
  - WOVI interrupt generation in interval timer mode
- Internal reset or internal interrupt generated when the timer counter overflows
  - Choice of internal reset or NMI interrupt generation in watchdog timer mode
- Choice of 8 (WDT0) or 16 (WDT1) counter input clocks
  - Maximum WDT interval: system clock period × 131072 × 256
  - Subclock can be selected for the WDT1 input counter
  - Maximum interval when the subclock is selected: subclock period × 256 × 256

ICDR is an 8-bit readable/writable register that is used as a transmit data register when transmitting and a receive data register when receiving. ICDR is divided internally into a shift register (ICDRS), receive buffer (ICDRR), and transmit buffer (ICDRT). ICDRS cannot be read or written by the CPU, ICDRR is read-only, and ICDRT is write-only. Data transfers among the three registers are performed automatically in coordination with changes in the bus state, and affect the status of internal flags such as TDRE and RDRF.

If IIC is in transmit mode and the next data is in ICDRT (the TDRE flag is 0) following transmission/reception of one frame of data using ICDRS, data is transferred automatically from ICDRT to ICDRS. If IIC is in receive mode and no previous data remains in ICDRR (the RDRF flag is 0) following transmission/reception of one frame of data using ICDRS, data is transferred automatically from ICDRS to ICDRR.

If the number of bits in a frame, excluding the acknowledge bit, is less than 8, transmit data and receive data are stored differently. Transmit data should be written justified toward the MSB side when MLS = 0, and toward the LSB side when MLS = 1. Receive data bits read from the LSB side should be treated as valid when MLS = 0, and bits read from the MSB side when MLS = 1.

ICDR is assigned to the same address as SARX, and can be written and read only when the ICE bit is set to 1 in ICCR.

The value of ICDR is undefined after a reset.

The TDRE and RDRF flags are set and cleared under the conditions shown below. Setting the TDRE and RDRF flags affects the status of the interrupt flags.

Bit 5—I²C Bus Interface Continuous Transmission/Reception Interrupt Request Flag (IRTR): Indicates that the I²C bus interface has issued an interrupt request to the CPU, and the source is completion of reception/transmission of one frame in continuous transmission/reception for which DTC activation is possible. When the IRTR flag is set to 1, the IRIC flag is also set to 1 at the same time.

IRTR flag setting is performed when the TDRE or RDRF flag is set to 1. IRTR is cleared by reading IRTR after it has been set to 1, then writing 0 in IRTR. IRTR is also cleared automatically when the IRIC flag is cleared to 0.

Bit 5

IRTR	Description	
0	Waiting for transfer, or transfer in progress	(Initial value)
	[Clearing conditions]	
	1. When 0 is written in IRTR after reading IRTR = 1	
	2. When the IRIC flag is cleared to 0	
1	Continuous transfer state	
	[Setting conditions]	
	• In I²C bus interface slave mode When the TDRE or RDRF flag is set to 1 when AASX = 1	
	• In other modes When the TDRE or RDRF flag is set to 1	

Bit 4—Second Slave Address Recognition Flag (AASX): In I²C bus format slave receive mode, this flag is set to 1 if the first frame following a start condition matches bits SVAX6 to SVAX0 in SARX.

AASX is cleared by reading AASX after it has been set to 1, then writing 0 in AASX. AASX is also cleared automatically when a start condition is detected.

18.2 Register Descriptions

18.2.1 D/A Data Registers 0 and 1 (DADR0, DADR1)

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D/A data registers 0 and 1 (DADR0 and DADR1) are 8-bit readable/writable registers that store data to be converted. When analog output is enabled, the value in the D/A data register is converted and output continuously at the analog output pin.

The D/A data registers are initialized to H'00 by a reset and in hardware standby mode.

18.2.2 D/A Control Register (DACR)

Bit	7	6	5	4	3	2	1	0
	DAOE1	DAOE0	DAE	—	—	—	—	—
Initial value	0	0	0	1	1	1	1	1
Read/Write	R/W	R/W	R/W	—	—	—	—	—

DACR is an 8-bit readable/writable register that controls the operation of the D/A converter module.

DACR is initialized to H'1F by a reset and in hardware standby mode.

Bit 7—D/A Output Enable 1 (DAOE1): Controls D/A conversion and analog output.

Bit 7 DAOE1	Description	
0	Analog output DA1 is disabled	(Initial value)
1	D/A conversion is enabled on channel 1. Analog output DA1 is enabled	

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Analog power supply voltage*1	AV_{CC}	4.5	—	5.5	V	Operating
		2.0	—	5.5	V	Idle/not used
RAM standby voltage	V_{RAM}	2.0	—	—	V	

Notes: 1. Do not leave the AVCC, and AVSS pins open even if the A/D converter and D/A converter are not used.

Even if the A/D converter and D/A converter are not used, apply a value in the range 2.0 V to 5.5 V to AVCC by connection to the power supply (V_{CC}), or some other method.

2. P67 to P60 include supporting module inputs multiplexed on those pins.
3. $\overline{IRQ2}$ includes the $\overline{ADTRG}$ signal multiplexed on that pin.
4. P52/SCK0/SCL0 and P97/SDA0 are NMOS push-pull outputs in H8S/2138.

An external pull-up resistor is necessary to provide high-level output from SCL0 and SDA0 (ICE = 1).

P52/SCK0 and P97 (ICE = 0) high levels are driven by NMOS in H8S/2138.

5. When ICE = 0. Low-level output when the bus drive function is selected is determined separately.
6. The upper limit of the port 6 applied voltage is V_{CC} +0.3 V when CIN input is not selected, and the lower of V_{CC} +0.3 V and AV_{CC} +0.3 V when CIN input is selected. When a pin is in output mode, the output voltage is equivalent to the applied voltage.
7. Current dissipation values are for V_{IH} min = V_{CC} –0.5 V and V_{IL} max = 0.5 V with all output pins unloaded and the on-chip pull-up MOSs in the off state.
8. The values are for $V_{RAM} \leq V_{CC} < 4.5V$, V_{IH} min = $V_{CC} \times 0.9$, and V_{IL} max = 0.3 V.
9. For flash memory program/erase operations, the applicable range is T_a = 0 to +75°C (regular specifications) or T_a = 0 to +85°C (wide-range specifications).

Table 25.12 A/D Conversion Characteristics
(CIN7 to CIN0 Input: 134/266-State Conversion)

Condition A: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0 V, φ = 2 MHz to maximum operating frequency, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Condition B: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, φ = 2 MHz to maximum operating frequency, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Condition C: V_{CC} = 3.0 V to 5.5 V, AV_{CC} = 3.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, φ = 2 MHz to maximum operating frequency, T_a = –20 to +75°C

	Condition A			Condition B			Condition C			
	20 MHz			16 MHz			10 MHz			
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Resolution	10	10	10	10	10	10	10	10	10	Bits
Conversion time*5	—	—	6.7	—	—	8.4	—	—	13.4	µs
Analog input capacitance	—	—	20	—	—	20	—	—	20	pF
Permissible signal-source impedance	—	—	10*3 5*4	—	—	10*3 5*4	—	—	10*1 5*2	kΩ
Nonlinearity error	—	—	±5.0	—	—	±5.0	—	—	±11.0	LSB
Offset error	—	—	±5.5	—	—	±5.5	—	—	±11.5	LSB
Full-scale error	—	—	±5.5	—	—	±5.5	—	—	±11.5	LSB
Quantization error	—	—	±0.5	—	—	±0.5	—	—	±0.5	LSB
Absolute accuracy	—	—	±6.0	—	—	±6.0	—	—	±12.0	LSB

Notes: 1. When 4.0 V ≤ AV_{CC} ≤ 5.5 V
2. When 3.0 V ≤ AV_{CC} < 4.0 V
3. When conversion time ≥ 11. 17 µs (CKS = 1 and φ ≤ 12 MHz, or CKS = 0)
4. When conversion time < 11. 17 µs (CKS = 1 and φ > 12 MHz)
5. In single mode and φ = maximum operating frequency.

25.3.4 A/D Conversion Characteristics

Tables 25.24 and 25.25 list the A/D conversion characteristics.

Table 25.24 A/D Conversion Characteristics (AN7 to AN0 Input: 134/266-State Conversion)

Condition A: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0 V, φ = 2 MHz to maximum operating frequency, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Condition B: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, φ = 2 MHz to maximum operating frequency, T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Condition C: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, φ = 2 MHz to maximum operating frequency, T_a = –20 to +75°C

	Condition A			Condition B			Condition C			
	20 MHz			16 MHz			10 MHz			
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Resolution	10	10	10	10	10	10	10	10	10	Bits
Conversion time[*3]	—	—	6.7	—	—	8.4	—	—	13.4	µs
Analog input capacitance	—	—	20	—	—	20	—	—	20	pF
Permissible signal-source impedance	—	—	10[*1] 5[*2]	—	—	10[*1] 5[*2]	—	—	5	kΩ
Nonlinearity error	—	—	±3.0	—	—	±3.0	—	—	±7.0	LSB
Offset error	—	—	±3.5	—	—	±3.5	—	—	±7.5	LSB
Full-scale error	—	—	±3.5	—	—	±3.5	—	—	±7.5	LSB
Quantization error	—	—	±0.5	—	—	±0.5	—	—	±0.5	LSB
Absolute accuracy	—	—	±4.0	—	—	±4.0	—	—	±8.0	LSB

Notes: 1. When conversion time ≥ 11. 17 µs (CKS = 1 and φ ≤ 12 MHz, or CKS = 0)
2. When conversion time < 11. 17 µs (CKS = 1 and φ > 12 MHz)
3. In single mode and φ = maximum operating frequency.

RDR1—Receive Data Register 1 **H'FF8D** **SCI1**
RDR2—Receive Data Register 2 **H'FFA5** **SCI2**
RDR0—Receive Data Register 0 **H'FFDD** **SCI0**

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Stores serial receive data

TDR1—Transmit Data Register 1 **H'FF8B** **SCI1**
TDR2—Transmit Data Register 2 **H'FFA3** **SCI2**
TDR0—Transmit Data Register 0 **H'FFDB** **SCI0**

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores serial transmit data

C.3 Port 3 Block Diagram

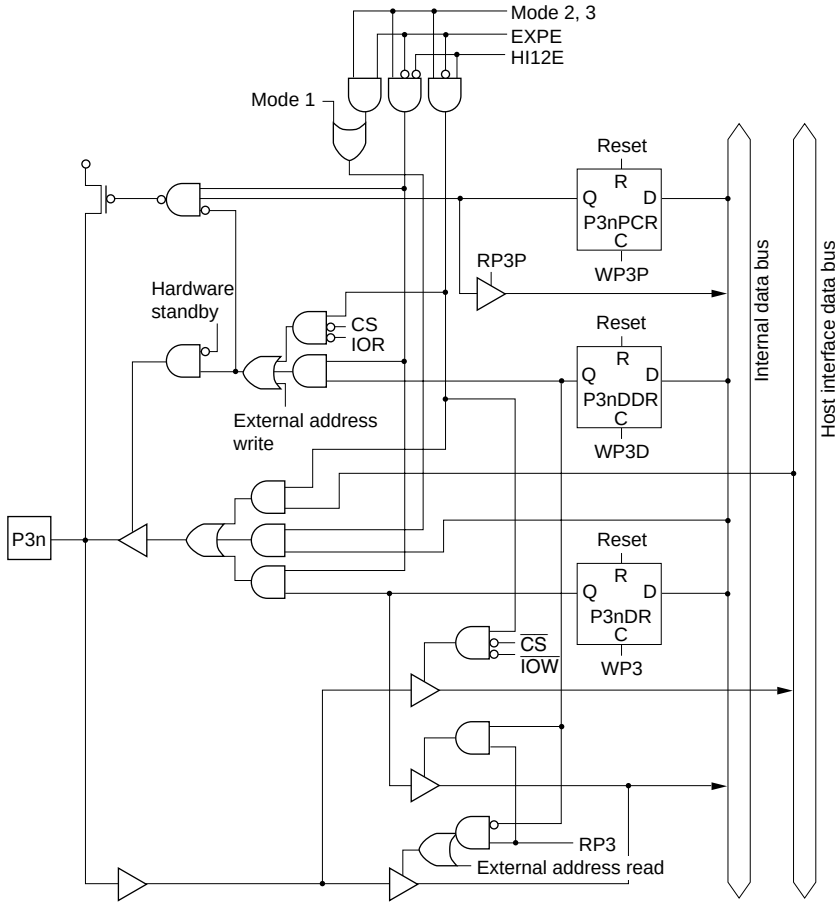


Figure C.5 Port 3 Block Diagram