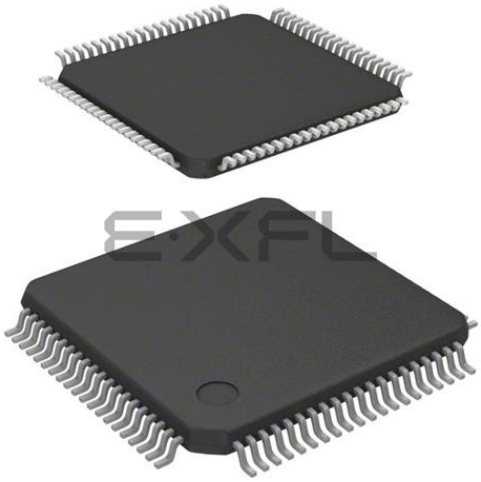

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	Host Interface, I²C, IrDA, SCI
Peripherals	POR, PWM, WDT
Number of I/O	58
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2138atf20v

Section 1 Overview

1.1 Overview

The H8S/2138 Group and H8S/2134 Group comprise microcomputers (MCUs) built around the H8S/2000 CPU, employing Renesas Technology proprietary architecture, and equipped with supporting modules on-chip.

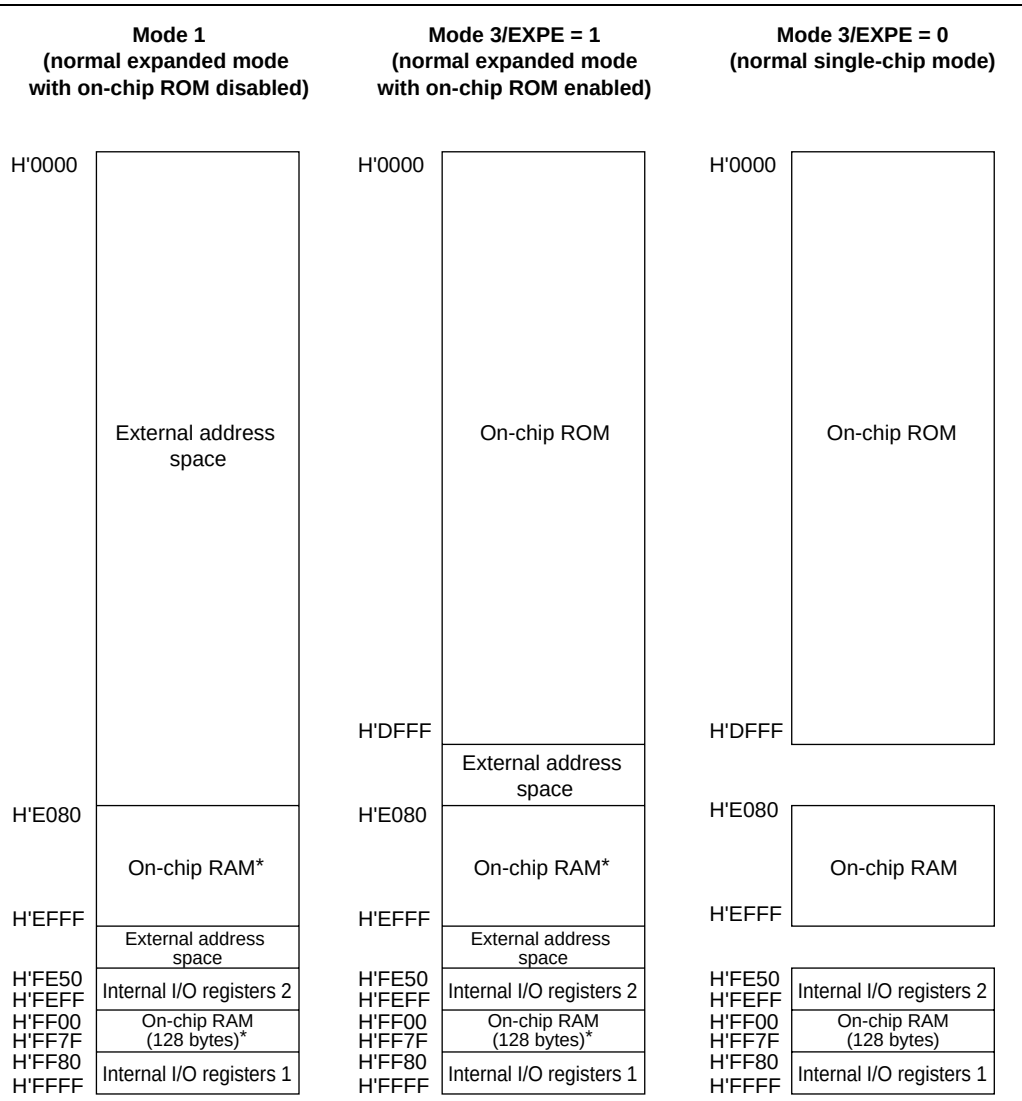
The H8S/2000 CPU has an internal 32-bit architecture, is provided with sixteen 16-bit general registers and a concise, optimized instruction set designed for high-speed operation, and can address a 16-Mbyte linear address space. The instruction set is upward-compatible with H8/300 and H8/300H CPU instructions at the object-code level, facilitating migration from the H8/300, H8/300L, or H8/300H Series.

On-chip supporting modules required for system configuration include a data transfer controller (DTC) bus master, ROM and RAM, a 16-bit free-running timer module (FRT), 8-bit timer module (TMR), watchdog timer module (WDT), two PWM timers (PWM and PWMX), serial communication interface (SCI), host interface (HIF), D/A converter (DAC), A/D converter (ADC), and I/O ports. An I^2C bus interface (IIC) can also be incorporated as an option.

The on-chip ROM is either flash memory (F-ZTAT™) or mask ROM, with a capacity of 128, 96, 64, or 32 kbytes. ROM is connected to the CPU via a 16-bit data bus, enabling both byte and wo data to be accessed in one state. Instruction fetching has been speeded up, and processing spe

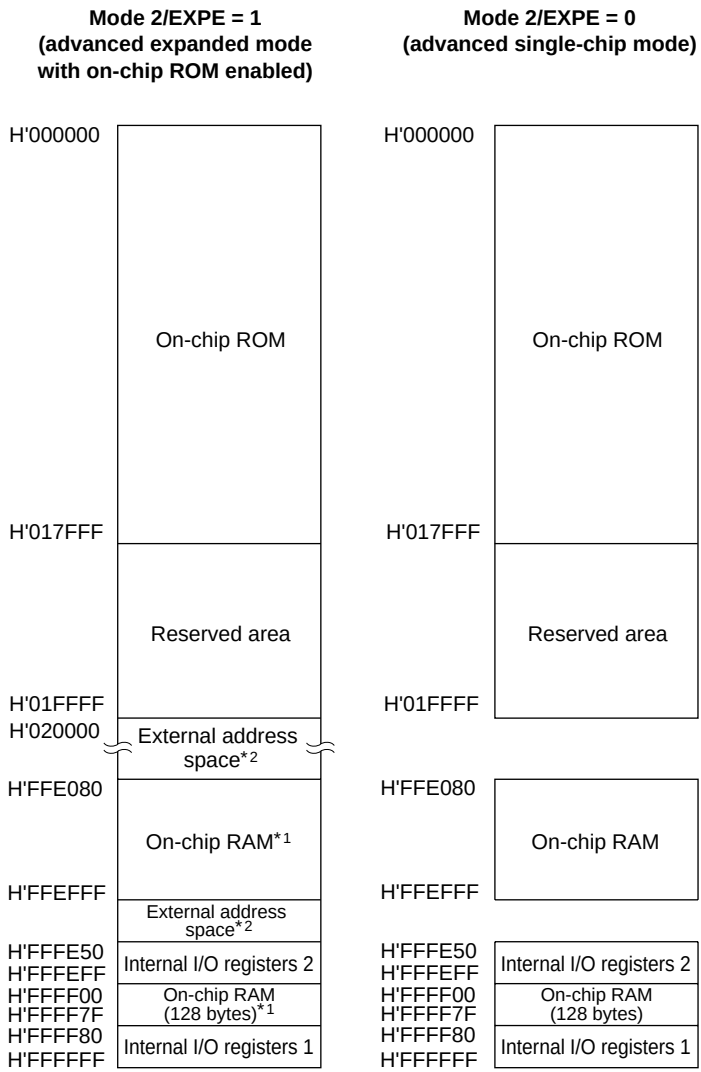
This manual describes the hardware of the H8S/2138 Group and H8S/2134 Group. Refer to the

Type	Instruction	Size*1	Function
Bit-manipulation instructions	BXOR	B	C ⊕ (<bit-No.> of <EAd>) → C Exclusive-ORs the carry flag with a specified bit in a general register or memory operand and stores the result in the carry flag.
	BIXOR	B	C ⊕ [¬ (<bit-No.> of <EAd>)] → C Exclusive-ORs the carry flag with the inverse of a specified bit in a general register or memory operand and stores the result in the carry flag. The bit number is specified by 3-bit immediate data.
	BLD	B	(<bit-No.> of <EAd>) → C Transfers a specified bit in a general register or memory operand to the carry flag.
	BILD	B	¬ (<bit-No.> of <EAd>) → C Transfers the inverse of a specified bit in a general register or memory operand to the carry flag. The bit number is specified by 3-bit immediate data.
	BST	B	C → (<bit-No.> of <EAd>) Transfers the carry flag value to a specified bit in a general register or memory operand.
	BIST	B	¬ C → (<bit-No.> of <EAd>) Transfers the inverse of the carry flag value to a specified bit in a general register or memory operand. The bit number is specified by 3-bit immediate data.



Note: * External addresses can be accessed by clearing the RAME bit in SYSCR to 0.

Figure 3.3 H8S/2133 Memory Map in Each Operating Mode



Notes: 1. External addresses can be accessed by clearing the RAME bit in SYSCR to 0.
2. For these models, the maximum number of external address pins is 16. An external address can only be specified correctly for an area that uses the I/O strobe function.

Figure 3.3 H8S/2133 Memory Map in Each Operating Mode (cont)

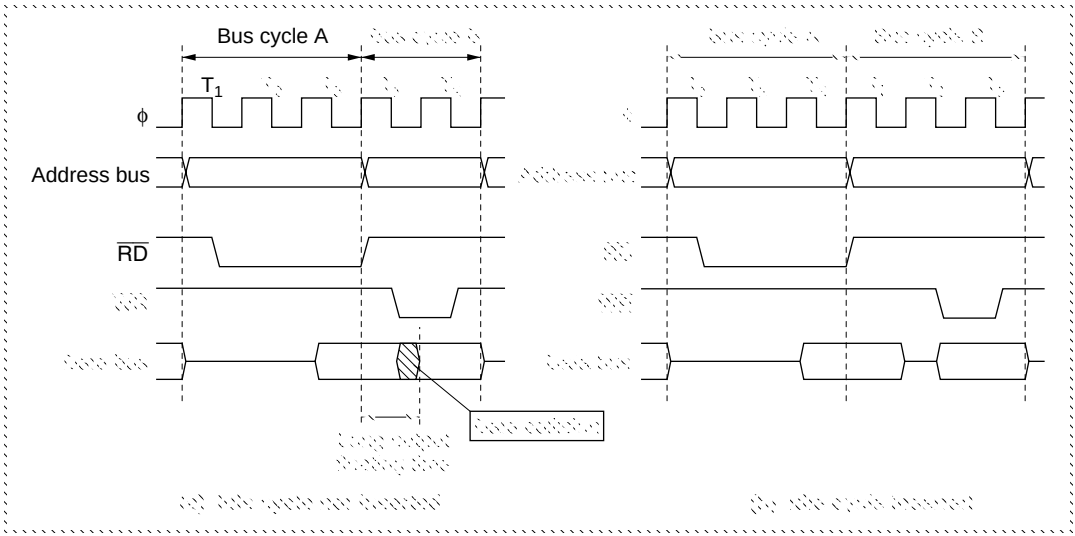


Figure 6.3 Example of Idle Cycle Operation

6.5.3 Pin States in Idle Cycle

Table 6.5 shows pin states in an idle cycle.

Table 6.5 Pin States in Idle Cycle

Pins	Pin State
A23 to A0, D15 to D0	Contents of next bus cycle
CS7 to CS0	High impedance
RD	High
HWR	High
LWR	High

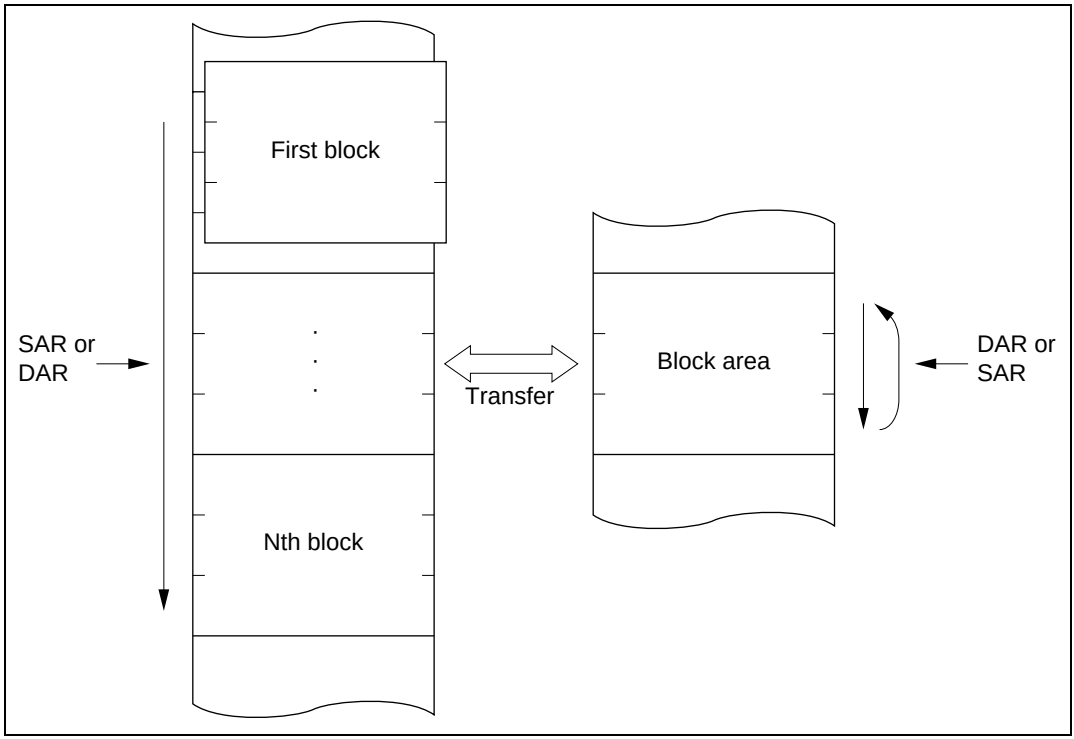


Figure 7.8 Memory Mapping in Block Transfer Mode

Pin	Selection Method and Pin Functions

P83

The pin function is switched as shown below according to bit P83DDR.

P83DDR	0	1
Pin function	P83 input pin	P83 output pin

P82/HIFSD

The pin function is switched as shown below according to the combination of operating mode, bit SDE in SYSCR2 of the HIF, and bit P82DDR.

Operating mode	Not slave mode		Slave mode		
SDE	—		0		1
P82DDR	0	1	0	1	—
Pin function	P82 input pin	P82 output pin	P82 input pin	P82 output pin	HIFSD input pin

P81/GA20/$\overline{\text{CS2}}$

The pin function is switched as shown below according to the combination of operating mode, bit CS2E, bit FGA20E in HICR of the HIF, and bit P81DDR.

Operating mode	Not slave mode		Slave mode				
FGA20E	—		0			1	
CS2E	—		0		1	—	
P81DDR	0	1	0	1	—	0	1
Pin function	P81 input pin	P81 output pin	P81 input pin	P81 output pin	$\overline{\text{CS2}}$ input pin	P81 input pin	GA20 output pin

This pin should be used as the GA20 or $\overline{\text{CS2}}$ output pin only in mode 2 or 3 (EXPE = 0).

P80/HA0

The pin function is switched as shown below according to the combination of operating mode and bit P80DDR.

Operating mode	Not slave mode		Slave mode
P80DDR	0	1	—
Pin function	P80 input pin	P80 output pin	HA0 input pin

9.2.10 Module Stop Control Register (MSTPCR)

	MSTPCRH								MSTPCRL							
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	MSTP15	MSTP14	MSTP13	MSTP12	MSTP11	MSTP10	MSTP9	MSTP8	MSTP7	MSTP6	MSTP5	MSTP4	MSTP3	MSTP2	MSTP1	MSTP0
Initial value	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MSTPCR comprises two 8-bit readable/writable registers, and is used to perform module stop mode control.

When the MSTP11 bit is set to 1, 8-bit PWM timer operation is halted and a transition is made to module stop mode. For details, see section 24.5, Module Stop Mode.

MSTPCR is initialized to H'3FFF by a reset and in hardware standby mode. It is not initialized in software standby mode.

MSTPCRH Bit 3—Module Stop (MSTP11): Specifies PWM module stop mode.

MSTPCRH Bit 3	
MSTP11	**Description**
0	PWM module stop mode is cleared
1	PWM module stop mode is set (Initial value)

11.2.9 Timer Output Compare Control Register (TOCR)

Bit	7	6	5	4	3	2	1	0
	ICRDMS	OCRAMS	ICRS	OCRS	OEA	OEB	OLVLA	OLVLB
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TOCR is an 8-bit readable/writable register that enables output from the output compare pins, selects the output levels, switches access between output compare registers A and B, controls th ICRD and OCRA operating mode, and switches access to input capture registers A, B, and C.

TOCR is initialized to H'00 by a reset and in hardware standby mode.

Bit 7—Input Capture D Mode Select (ICRDMS): Specifies whether ICRD is used in the normal operating mode or in the operating mode using OCRDM.

Bit 7

ICRDMS	**Description**	
0	The normal operating mode is specified for ICRD	(Initial value)
1	The operating mode using OCRDM is specified for ICRD	

Bit 6—Output Compare A Mode Select (OCRAMS):Specifies whether OCRA is used in the normal operating mode or in the operating mode using OCRAR and OCRAF.

Bit 6

OCRAMS	**Description**	
0	The normal operating mode is specified for OCRA	(Initial value)
1	The operating mode using OCRAR and OCRAF is specified for OCRA	

Bit 5—Input Capture Register Select (ICRS):The same addresses are shared by ICRA and OCRAR, by ICRB and OCRAF, and by ICRC and OCRDM. The ICRS bit determines which registers are selected when the shared addresses are read or written to. The operation of ICRA, ICRB, and ICRC is not affected.

Bit 4—Framing Error (FER): Indicates that a framing error occurred during reception in asynchronous mode, causing abnormal termination.

Bit 4

FER	Description
0	[Clearing condition] (Initial value)*1 When 0 is written in FER after reading FER = 1
1	[Setting condition] When the SCI checks the stop bit at the end of the receive data when reception ends, and the stop bit is 0 *2

Notes: 1. The FER flag is not affected and retains its previous state when the RE bit in SCR is cleared to 0.

2. In 2-stop-bit mode, only the first stop bit is checked for a value of 0; the second stop bit is not checked. If a framing error occurs, the receive data is transferred to RDR but the RDRF flag is not set. Also, subsequent serial reception cannot be continued while the FER flag is set to 1. In synchronous mode, serial transmission cannot be continued, either.

Bit 3—Parity Error (PER): Indicates that a parity error occurred during reception using parity addition in asynchronous mode, causing abnormal termination.

Bit 3

PER	Description
0	[Clearing condition] (Initial value)*1 When 0 is written in PER after reading PER = 1
1	[Setting condition] When, in reception, the number of 1 bits in the receive data plus the parity bit does not match the parity setting (even or odd) specified by the O/$\overline{E}$ bit in SMR*2

Notes: 1. The PER flag is not affected and retains its previous state when the RE bit in SCR is cleared to 0.

2. If a parity error occurs, the receive data is transferred to RDR but the RDRF flag is not set. Also, subsequent serial reception cannot be continued while the PER flag is set to 1. In synchronous mode, serial transmission cannot be continued, either.

Bit 5—A/D Start (ADST): Selects starting or stopping of A/D conversion. Holds a value of 1 during A/D conversion.

The ADST bit can be set to 1 by software, a timer conversion start trigger, or the A/D external trigger input pin ($\overline{\text{ADTRG}}$).

Bit 5

ADST	Description	
0	A/D conversion stopped	(Initial value)
1	Single mode: A/D conversion is started. Cleared to 0 automatically when conversion on the specified channel ends Scan mode: A/D conversion is started. Conversion continues sequentially on the selected channels until ADST is cleared to 0 by software, a reset, or a transition to standby mode or module stop mode	

Bit 4—Scan Mode (SCAN):Selects single mode or scan mode as the A/D conversion operating mode. See section 19.4, Operation, for single mode and scan mode operation. Only set the SCA bit while conversion is stopped.

Bit 4

SCAN	Description	
0	Single mode	(Initial value)
1	Scan mode	

Bit 3—Clock Select (CKS):Sets the A/D conversion time. Only change the conversion time while ADST = 0.

Bit 3

CKS	Description	
0	Conversion time = 266 states (max.)	(Initial value)
1	Conversion time = 134 states (max.)	

On-Board Programming Modes

- Boot mode

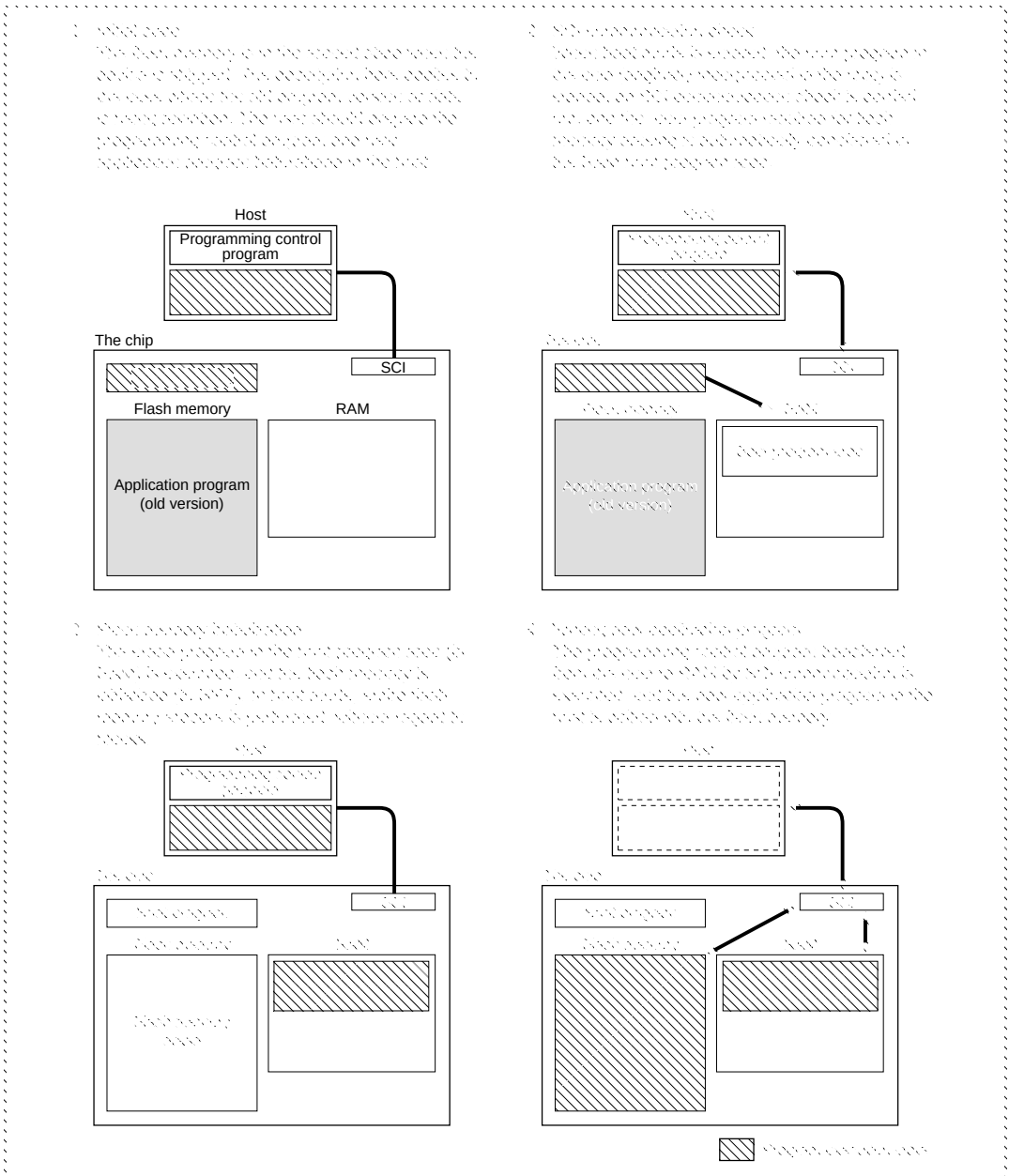


Figure 21.21 Boot Mode

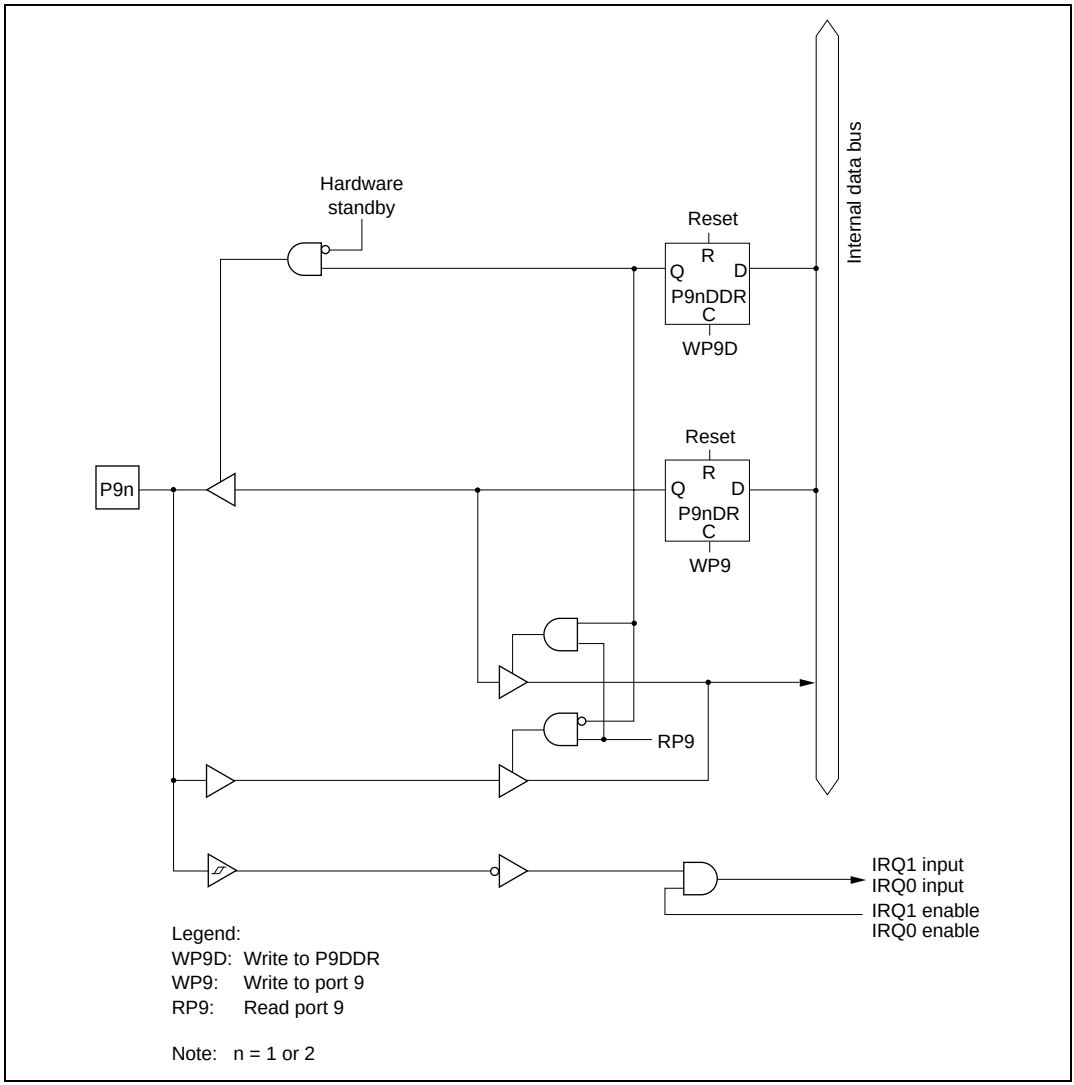


Figure C.30 Port 9 Block Diagram (Pins P91, P92)