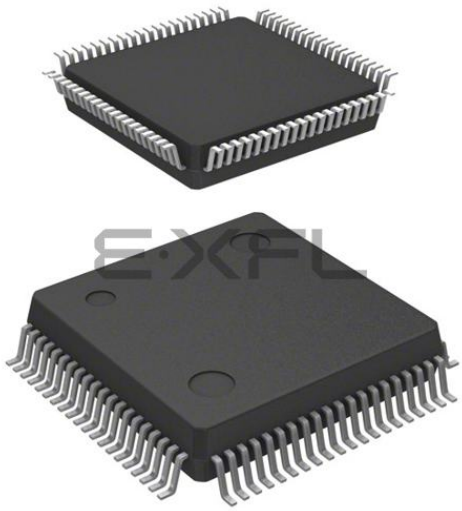
Renesas Electronics America Inc - DF2138AVFA10V Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2000
Core Size	16-Bit
Speed	10MHz
Connectivity	Host Interface, I²C, IrDA, SCI
Peripherals	POR, PWM, WDT
Number of I/O	58
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2138avfa10v

(3) Condition-Code Register (CCR)

This 8-bit register contains internal CPU status information, including an interrupt mask bit (I) and half-carry (H), negative (N), zero (Z), overflow (V), and carry (C) flags.

Bit 7—Interrupt Mask Bit (I): Masks interrupts other than NMI when set to 1. (NMI is accepted regardless of the I bit setting.) The I bit is set to 1 by hardware at the start of an exception-handling sequence. For details, refer to section 5, Interrupt Controller.

Bit 6—User Bit or Interrupt Mask Bit (UI): Can be written and read by software using the LDC, STC, ANDC, ORC, and XORC instructions. This bit can also be used as an interrupt mask bit. For details, refer to section 5, Interrupt Controller.

Bit 5—Half-Carry Flag (H): When the ADD.B, ADDX.B, SUB.B, SUBX.B, CMP.B, or NEG.B instruction is executed, this flag is set to 1 if there is a carry or borrow at bit 3, and cleared to 0 otherwise. When the ADD.W, SUB.W, CMP.W, or NEG.W instruction is executed, the H flag is set to 1 if there is a carry or borrow at bit 11, and cleared to 0 otherwise. When the ADD.L, SUB.L, CMP.L, or NEG.L instruction is executed, the H flag is set to 1 if there is a carry or borrow at bit 27, and cleared to 0 otherwise.

Bit 4—User Bit (U): Can be written and read by software using the LDC, STC, ANDC, ORC, and XORC instructions.

Bit 3—Negative Flag (N): Stores the value of the most significant bit (sign bit) of data.

Bit 2—Zero Flag (Z): Set to 1 to indicate zero data, and cleared to 0 to indicate non-zero data.

Bit 1—Overflow Flag (V): Set to 1 when an arithmetic overflow occurs, and cleared to 0 otherwise.

Bit 0—Carry Flag (C): Set to 1 when a carry occurs, and cleared to 0 otherwise. Used by:

- Add instructions, to indicate a carry
- Subtract instructions, to indicate a borrow
- Shift and rotate instructions, to store the carry

The carry flag is also used as a bit accumulator by bit-manipulation instructions.

Some instructions leave some or all of the flag bits unchanged. For the action of each instruction on the flag bits, refer to appendix A.1, Instruction.

2.7 Addressing Modes and Effective Address Calculation

2.7.1 Addressing Mode

The CPU supports the eight addressing modes listed in table 2.4. Each instruction uses a subset of these addressing modes. Arithmetic and logic instructions can use the register direct and immediate modes. Data transfer instructions can use all addressing modes except program-counter relative and memory indirect. Bit-manipulation instructions use register direct, register indirect, or absolute addressing mode to specify an operand, and register direct (BSET, BCLR, BNOT, and BTST instructions) or immediate (3-bit) addressing mode to specify a bit number in the operand.

Table 2.4 Addressing Modes

No.	Addressing Mode	Symbol
1	Register direct	Rn
2	Register indirect	@ERn
3	Register indirect with displacement	@(d:16,ERn)/@(d:32,ERn)
4	Register indirect with post-increment Register indirect with pre-decrement	@ERn+ @-ERn
5	Absolute address	@aa:8/@aa:16/@aa:24/@aa:32
6	Immediate	#xx:8/#xx:16/#xx:32
7	Program-counter relative	@(d:8,PC)/@(d:16,PC)
8	Memory indirect	@@aa:8

Register Direct—Rn: The register field of the instruction code specifies an 8-, 16-, or 32-bit general register containing the operand. R0H to R7H and R0L to R7L can be specified as 8-bit registers. R0 to R7 and E0 to E7 can be specified as 16-bit registers. ER0 to ER7 can be specified as 32-bit registers.

Register Indirect—@ERn: The register field of the instruction code specifies an address register (ERn) which contains the address of the operand in memory. If the address is a program instruction address, the lower 24 bits are valid and the upper 8 bits are all assumed to be 0 (H'00).

Register Indirect with Displacement—@(d:16, ERn) or @(d:32, ERn): A 16-bit or 32-bit displacement contained in the instruction is added to an address register (ERn) specified by the register field of the instruction, and the sum gives the address of a memory operand. A 16-bit displacement is sign-extended when added.

3.1.2 Register Configuration

The H8S/2138 Group and H8S/2134 Group have a mode control register (MDCR) that indicates the inputs at the mode pins (MD1 and MD0), a system control register (SYSCR) and bus control register (BCR) that control the operation of the MCU, and a serial timer control register (STCR) that controls the operation of the supporting modules. Table 3.2 summarizes these registers.

Table 3.2 MCU Registers

Name	Abbreviation	R/W	Initial Value	Address*
Mode control register	MDCR	R/W	Undetermined	H'FFC5
System control register	SYSCR	R/W	H'09	H'FFC4
Bus control register	BCR	R/W	H'D7	H'FFC6
Serial timer control register	STCR	R/W	H'00	H'FFC3

Note: * Lower 16 bits of the address.

3.2 Register Descriptions

3.2.1 Mode Control Register (MDCR)

Bit	7	6	5	4	3	2	1	0
	EXPE	—	—	—	—	—	MDS1	MDS0
Initial value	—*	0	0	0	0	0	—*	—*
Read/Write	R/W*	—	—	—	—	—	R	R

Note: * Determined by pins MD1 and MD0.

MDCR is an 8-bit read-only register that indicates the operating mode setting and the current operating mode of the MCU.

The EXPE bit is initialized in coordination with the mode pin states by a reset and in hardware standby mode.

6.5 Burst ROM Interface

6.5.1 Overview

With the H8S/2138 Group and H8S/2134 Group, external space area 0 can be designated as burst ROM space, and burst ROM interfacing can be performed.

External space can be designated as burst ROM space by means of the BRSTRM bit in BCR. Consecutive burst accesses of a maximum of 4 words or 8 words can be performed for CPU instruction fetches only. One or two states can be selected for burst access.

6.5.2 Basic Timing

The number of states in the initial cycle (full access) of the burst ROM interface is in accordance with the setting of the AST bit. Also, when the AST bit is set to 1, wait state insertion is possible. One or two states can be selected for the burst cycle, according to the setting of the BRSTS1 bit in BCR. Wait states cannot be inserted.

When the BRSTS0 bit in BCR is cleared to 0, burst access of up to 4 words is performed; when the BRSTS0 bit is set to 1, burst access of up to 8 words is performed.

The basic access timing for burst ROM space is shown in figures 6.8 (a) and (b). The timing shown in figure 6.8 (a) is for the case where the AST and BRSTS1 bits are both set to 1, and that in figure 6.8 (b) is for the case where both these bits are cleared to 0.

7.2.2 DTC Mode Register B (MRB)

Bit	7	6	5	4	3	2	1	0
	CHNE	DISEL	—	—	—	—	—	—
Initial value	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
Read/Write	—	—	—	—	—	—	—	—

MRB is an 8-bit register that controls the DTC operating mode.

Bit 7—DTC Chain Transfer Enable (CHNE): Specifies chain transfer. In chain transfer, multiple data transfers can be performed consecutively in response to a single transfer request. With data transfer for which CHNE is set to 1, there is no determination of the end of the specified number of transfers, clearing of the interrupt source flag, or clearing of DTCER.

Bit 7

CHNE	Description
0	End of DTC data transfer (activation waiting state is entered)
1	DTC chain transfer (new register information is read, then data is transferred)

Bit 6—DTC Interrupt Select (DISEL): Specifies whether interrupt requests to the CPU are disabled or enabled after a data transfer.

Bit 6

DISEL	Description
0	After a data transfer ends, the CPU interrupt is disabled unless the transfer counter is 0 (the DTC clears the interrupt source flag of the activating interrupt to 0)
1	After a data transfer ends, the CPU interrupt is enabled (the DTC does not clear the interrupt source flag of the activating interrupt to 0)

Bits 5 to 0—Reserved: In the H8S/2138 Group these bits have no effect on DTC operation, and should always be written with 0.

9.2 Register Descriptions

9.2.1 PWM Register Select (PWSL)

Bit	7	6	5	4	3	2	1	0
	PWCKE	PWCKS	—	—	RS3	RS2	RS1	RS0
Initial value	0	0	1	0	0	0	0	0
Read/Write	R/W	R/W	—	—	R/W	R/W	R/W	R/W

PWSL is an 8-bit readable/writable register used to select the PWM timer input clock and the PWM data register.

PWSL is initialized to H'20 by a reset, and in the standby modes, watch mode, subactive mode, subsleep mode, and module stop mode.

Bits 7 and 6—PWM Clock Enable, PWM Clock Select (PWCKE, PWCKS): These bits, together with bits PWCKA and PWCKB in PCSR, select the internal clock input to TCNT in the PWM timer.

PWSL		PCSR			
Bit 7	**Bit 6**	**Bit 2**	**Bit 1**		
PWCKE	**PWCKS**	**PWCKB**	**PWCKA**	**Description**	
0	—	—	—	Clock input is disabled	(Initial value)
1	0	—	—	ϕ (system clock) is selected	
	1	0	0	$\phi/2$ is selected	
			1	$\phi/4$ is selected	
		1	0	$\phi/8$ is selected	
			1	$\phi/16$ is selected	

The PWM resolution, PWM conversion period, and carrier frequency depend on the selected internal clock, and can be found from the following equations.

Resolution (minimum pulse width) = 1/internal clock frequency
PWM conversion period = resolution × 256
Carrier frequency = 16/PWM conversion period

Thus, with a 20-MHz system clock (ϕ), the resolution, PWM conversion period, and carrier frequency are as shown below.

10.1.3 Pin Configuration

Table 10.1 lists the pins used by the PWM D/A module.

Table 10.1 Input and Output Pins

Name	Abbr.	I/O	Function
PWM output pin 0	PWX0	Output	PWM output, channel A
PWM output pin 1	PWX1	Output	PWM output, channel B

10.1.4 Register Configuration

Table 10.2 lists the registers of the PWM D/A module.

Table 10.2 Register Configuration

Name	Abbreviation	R/W	Initial value	Address*1
PWM D/A control register	DACR	R/W	H'30	H'FFA0*2
PWM D/A data register A high	DADRAH	R/W	H'FF	H'FFA0*2
PWM D/A data register A low	DADRAL	R/W	H'FF	H'FFA1*2
PWM D/A data register B high	DADRBH	R/W	H'FF	H'FFA6*2
PWM D/A data register B low	DADRBL	R/W	H'FF	H'FFA7*2
PWM D/A counter high	DACNTH	R/W	H'00	H'FFA6*2
PWM D/A counter low	DACNTL	R/W	H'03	H'FFA7*2
Module stop control register	MSTPCRH	R/W	H'3F	H'FF86
	MSTPCRL	R/W	H'FF	H'FF87

Notes: 1. Lower 16 bits of the address.

2. Registers in the 14-bit PWM timer are assigned to the same addresses as the other registers. In this case, register selection is performed by the IICE bit in the serial timer control register (STCR), and also the same addresses are shared by DADRAH and DACR, and by DADRB and DACNT. Switching is performed by the REGS bit in DACNT or DADRB.

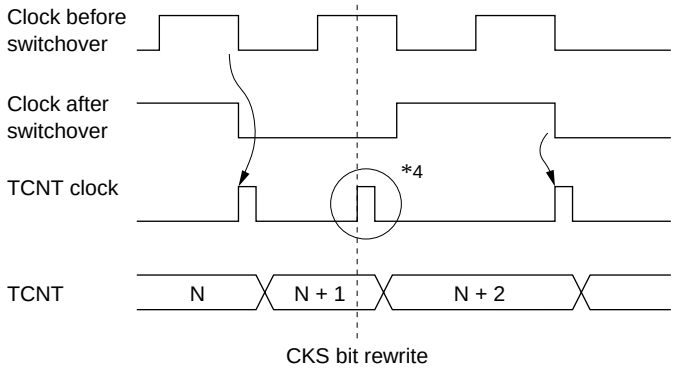
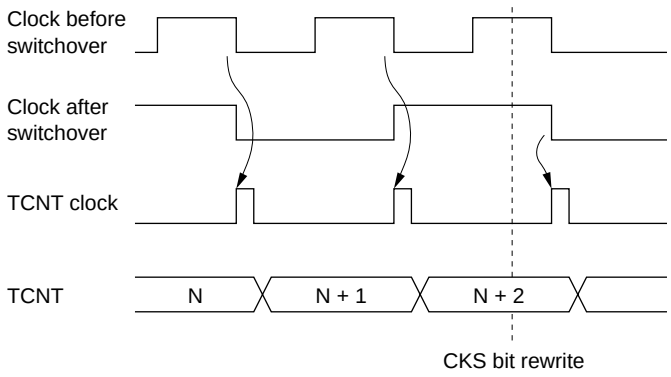
10.2.2 D/A Data Registers A and B (DADRA and DADRB)

	DADRH								DADRL							
Bit (CPU)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit (Data)	13	12	11	10	9	8	7	6	5	4	3	2	1	0	—	—
DADRA	DA13	DA12	DA11	DA10	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	CFS	—
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—
DADRB	DA13	DA12	DA11	DA10	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	CFS	REGS
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

There are two 16-bit readable/writable D/A data registers: DADRA and DADRB. DADRA corresponds to PWM D/A channel A, and DADRB to PWM D/A channel B. The CPU can read and write the PWM D/A data register values, but since DADRA and DADRB are 16-bit registers, data transfers between them and the CPU are performed using a temporary register (TEMP). See section 10.3, Bus Master Interface, for details.

The least significant (CPU) bit of DADRA is not used and is always read as 1.

DADR is initialized to H'FFFF by a reset, and in the standby modes, watch mode, subactive mode, subsleep mode, and module stop mode.

No.	Timing of Switchover by Means of CKS1 and CKS0 Bits	TCNT Clock Operation
3	Switching from high to low*3	
4	Switching from high to high	

Notes: 1. Includes switching from low to stop, and from stop to low.
2. Includes switching from stop to high.
3. Includes switching from high to stop.
4. Generated on the assumption that the switchover is a falling edge; TCNT is incremented.

Table 13.8 Examples of OCRAR, OCRAF, TOCR, TCORA, TCORB, TCR, and TCSR Settings

Register	Bit(s)	Abbreviation	Contents	Description	
TCR in TMRY	7	CMIEB	0	Interrupts due to compare-match and overflow are disabled	
	6	CMIEA	0		
	5	OVIE	0		
	4 and 3	CCLR1, CCLR0	01	TCNT is cleared by compare-match A	
	2 to 0	CKS2 to CKS0	001	TCNT is incremented on internal clock: $\phi/4$	
TCSR in TMRY	3 to 0	OS3 to OS0	0110	0 output on compare-match B 1 output on compare-match A	
TOCRA in TMRY			H'3F (example)	IHG signal period = $\phi \times 256$	
TOCRB in TMRY			H'03 (example)	IHG signal 1 interval = $\phi \times 16$	
TCR in FRT	1 and 0	CKS1, CKS0	01	FRC is incremented on internal clock: $\phi/8$	
OCRAR in FRT			H'7FEF (example)	IVG signal 0 interval = $\phi \times 262016$	IVG signal period = $\phi \times 262144$ (1024 times IHG signal)
OCRAF in FRT			H'000F (example)	IVG signal 1 interval = $\phi \times 128$	
TOCR in FRT	6	OCRAMS	1	OCRA is set to the operating mode in which OCRAR and OCRAF are used	

only when register IDR1 is accessed using $\overline{CS1}$. Slave logic decodes the commands input from the host processor. When an H'D1 host command is detected, bit 1 of the data following the host command is output from the GA20 output pin. This operation does not depend on firmware or interrupts, and is faster than the regular processing using interrupts. Table 17.7 lists the conditions that set and clear GA20 (P81). Figure 17.2 shows the GA20 output in flowchart form. Table 17.8 indicates the GA20 output signal values.

Table 17.7 GA20 (P81) Set/Clear Timing

Pin Name	Setting Condition	Clearing Condition
GA20 (P81)	Rising edge of the host's write signal ($\overline{IOW}$) when bit 1 of the written data is 1 and the data follows an H'D1 host command	Rising edge of the host's write signal ($\overline{IOW}$) when bit 1 of the written data is 0 and the data follows an H'D1 host command Also, when bit FGA20E in HICR is cleared to 0

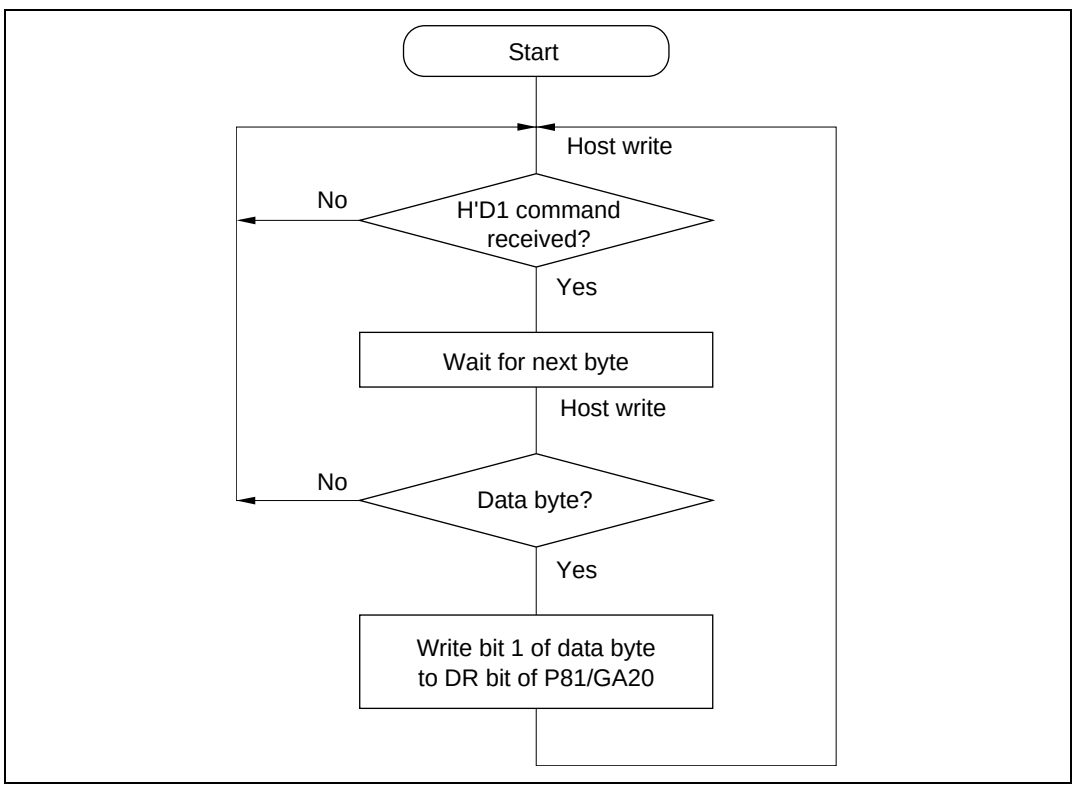


Figure 17.2 GA20 Output

- Interrupts cannot be used while the flash memory is being programmed or erased.
- The RxD1 and TxD1 pins should be pulled up on the board.
- Before branching to the programming control program (RAM area H'(FF)E080 (128-kbyte versions including H8S/2132, except for H8S/2132R or H'(FF)E880 (64-kbyte versions, including H8S/2132R, except for H8S/2132)), the chip terminates transmit and receive operations by the on-chip SCI (channel 1) (by clearing the RE and TE bits in SCR to 0), but the adjusted bit rate value remains set in BRR. The transmit data output pin, TxD1, goes to the high-level output state (P84DDR = 1, P84DR = 1).

  The contents of the CPU's internal general registers are undefined at this time, so these registers must be initialized immediately after branching to the programming control program. In particular, since the stack pointer (SP) is used implicitly in subroutine calls, etc., a stack area must be specified for use by the programming control program.

  The initial values of other on-chip registers are not changed.
- Boot mode can be entered by making the pin settings shown in table 21.6 and executing a reset-start.

  When the chip detects the boot mode setting at reset release*1, P92, P91, and P90 can be used as I/O ports.

  Boot mode can be cleared by driving the reset pin low, waiting at least 20 states, then setting the mode pins, and executing reset release*1. Boot mode can also be cleared by a WDT overflow reset.

  The mode pin input levels must not be changed in boot mode.
- If the mode pin input levels are changed (for example, from low to high) during a reset, the state of ports with multiplexed address functions and bus control output pins ($\overline{AS}$, $\overline{RD}$, $\overline{WR}$) will change according to the change in the microcomputer's operating mode*2.

  Therefore, care must be taken to make pin settings to prevent these pins from becoming output signal pins during a reset, or to prevent collision with signals outside the microcomputer.

Notes: 1. Mode pin input must satisfy the mode programming setup time (t_{MDS} = 4 states) with respect to the reset release timing.

2. Ports with multiplexed address functions will output a low level as the address signal if mode pin setting is for mode 1 is entered during a reset. In other modes, the port pins go to the high-impedance state. The bus control output signals will output a high level if mode pin setting is for mode 1 is entered during a reset. In other modes, the port pins go to the high-impedance state.

21.10.2 Socket Adapters and Memory Map

In programmer mode, a socket adapter is mounted on the writer programmer to match the package concerned. Socket adapters are available for each writer manufacturer supporting Renesas Technology microcomputer device types with 128-kbyte or 64-kbyte on-chip flash memory.

Figure 21.15 shows the memory map in programmer mode. For pin names in programmer mode, see section 1.3.2, Pin Functions in Each Operating Mode.

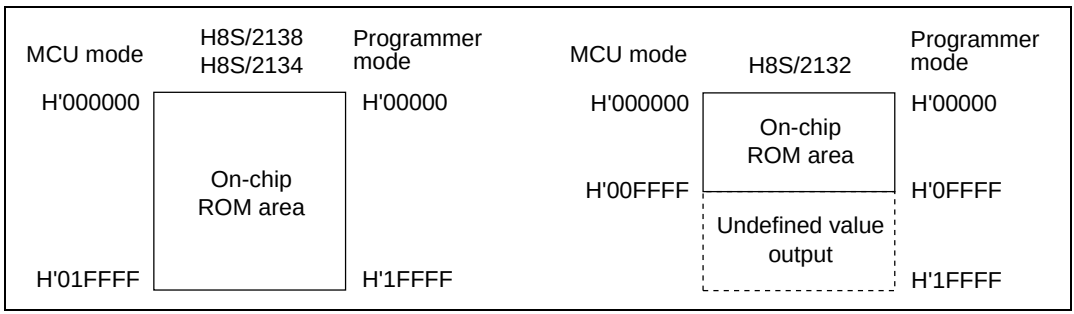


Figure 21.15 Memory Map in Programmer Mode

21.10.3 Programmer Mode Operation

Table 21.11 shows how the different operating modes are set when using programmer mode, and table 21.12 lists the commands used in programmer mode. Details of each mode are given below.

- Memory Read Mode

  Memory read mode supports byte reads.
- Auto-Program Mode

  Auto-program mode supports programming of 128 bytes at a time. Status polling is used to confirm the end of auto-programming.
- Auto-Erase Mode

  Auto-erase mode supports automatic erasing of the entire flash memory. Status polling is used to confirm the end of auto-erasing.
- Status Read Mode

  Status polling is used for auto-programming and auto-erasing, and normal termination can be confirmed by reading the FO6 signal. In status read mode, error information is output if an error occurs.

22.5.3 Erase Block Registers 1 and 2 (EBR1, EBR2)

Bit	7	6	5	4	3	2	1	0
EBR1	—	—	—	—	—	—	EB9	EB8
Initial value	0	0	0	0	0	0	0	0
Read/Write	—*2	—*2	—*2	—*2	—*2	—*2	R/W*1	R/W*1

Bit	7	6	5	4	3	2	1	0
EBR2	EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W*1	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Notes: 1. In normal mode, these bits cannot be modified and are always read as 0.
2. This bit must not be set to 1.

EBR1 and EBR2 are registers that specify the flash memory erase area block by block; bits 1 and 0 in EBR1 and bits 7 to 0 in EBR2 are readable/writable bits. EBR1 and EBR2 are each initialized to H'00 by a reset, in hardware standby mode, software standby mode, subactive mode, subsleep mode, and watch mode, and when the SWE bit in FLMCR1 is not set. When a bit in EBR1 and EBR2 is set, the corresponding block can be erased. Other blocks are erase-protected. Set only one bit in EBR1 and EBR2 (more than one bit cannot be set). When on-chip flash memory is disabled, a read will return H'00, and writes are invalid.

The flash memory block configuration is shown in table 22.5.

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Output high voltage	All output pins (except P97, and P52*4)*5	V_{OH}	V_{CC} –0.5	—	—	V	I_{OH} = –200 µA
			3.5	—	—	V	I_{OH} = –1 mA
	P97, P52*4		2.0	—	—	V	I_{OH} = –200 µA, V_{CC} = 4.5 to 5.5 V
Output low voltage	All output pins*5	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
	Ports 1 to 3		—	—	1.0	V	I_{OL} = 10 mA
Input leakage current	$\overline{RES}$	$\lvert I_{in} \rvert$	—	—	10.0	µA	V_{in} = 0.5 to V_{CC} –0.5 V
	$\overline{STBY}$, NMI, MD1, MD0		—	—	1.0	µA	
	Port 7		—	—	1.0	µA	V_{in} = 0.5 to AV_{CC} –0.5 V
Three-state leakage current (off state)	Ports 1 to 6, 8, 9	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0.5 to V_{CC} –0.5 V
Input pull-up MOS current	Ports 1 to 3	$-I_P$	30	—	300	µA	V_{in} = 0 V
	Port 6 (P6PUE = 0)		60	—	600	µA	
	Port 6 (P6PUE = 1)		15	—	200	µA	
Input capacitance	$\overline{RES}$ (4)	C_{in}	—	—	80	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25°C
	NMI		—	—	50	pF	
	P52, P97, P42, P86		—	—	20	pF	
	Input pins except (4) above		—	—	15	pF	
Current dissipation*7	Normal operation	I_{CC}	—	55	70	mA	f = 20 MHz
	Sleep mode		—	36	55	mA	f = 20 MHz
	Standby mode*8		—	1.0	5.0	µA	$T_a \leq 50°C$
			—	—	20.0	µA	50°C < T_a
Analog power supply current	During A/D, D/A conversion	AI_{CC}	—	3.2	7.0	mA	
	Idle		—	0.01	5.0	µA	AV_{CC}= 2.0 V to 5.5 V

Table 25.17 Permissible Output Currents

Conditions: V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0 V, Ta = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin)	SCL1, SCL0, SDA1, SDA0	I_{OL}	—	—	20	mA
	Ports 1 to 3		—	—	10	mA
	Other output pins		—	—	2	mA
Permissible output low current (total)	Total of ports 1 to 3	$\sum I_{OL}$	—	—	80	mA
	Total of all output pins, including the above		—	—	120	mA
Permissible output high current (per pin)	All output pins	$-I_{OH}$	—	—	2	mA
Permissible output high current (total)	Total of all output pins	$\sum -I_{OH}$	—	—	40	mA

Conditions: V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0 V, T_a = –20 to +75°C

Item		Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin)	SCL1, SCL0, SDA1, SDA0	I_{OL}	—	—	10	mA
	Ports 1 to 3		—	—	2	mA
	Other output pins		—	—	1	mA
Permissible output low current (total)	Total of ports 1 to 3	$\sum I_{OL}$	—	—	40	mA
	Total of all output pins, including the above		—	—	60	mA
Permissible output high current (per pin)	All output pins	$-I_{OH}$	—	—	2	mA
Permissible output high current (total)	Total of all output pins	$\sum -I_{OH}$	—	—	30	mA

Notes: 1. To protect chip reliability, do not exceed the output current values in table 25.17.

2. When driving a Darlington pair or LED, always insert a current-limiting resistor in the output line, as show in figures 25.1 and 25.2.

Item			Symbol	Condition A 20 MHz Min	Condition A 20 MHz Max	Condition B 16 MHz Min	Condition B 16 MHz Max	Condition C 10 MHz Min	Condition C 10 MHz Max	Unit	Test Conditions
TMR	Timer output delay time		t_{TMOD}	—	50	—	50	—	100	ns	Figure 25.18
	Timer reset input setup time		t_{TMRS}	30	—	30	—	50	—		Figure 25.20
	Timer clock input setup time		t_{TMCS}	30	—	30	—	50	—		Figure 25.19
	Timer clock pulse width	Single edge	t_{TMCWH}	1.5	—	1.5	—	1.5	—	t_{cyc}	
		Both edges	t_{TMCWL}	2.5	—	2.5	—	2.5	—		
PWM, PWMX	Pulse output delay time		t_{PWOD}	—	50	—	50	—	100	ns	Figure 25.21
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	4	—	4	—	t_{cyc}	Figure 25.22
		Synchronous		6	—	6	—	6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	0.4	0.6	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	1.5	—	1.5	—	1.5	t_{cyc}	
	Input clock fall time		t_{SCKf}	—	1.5	—	1.5	—	1.5		
	Transmit data delay time (synchronous)		t_{TXD}	—	50	—	50	—	100	ns	Figure 25.23
	Receive data setup time (synchronous)		t_{RXS}	50	—	50	—	100	—	ns	
	Receive data hold time (synchronous)		t_{RXH}	50	—	50	—	100	—	ns	
A/D converter	Trigger input setup time		t_{TRGS}	30	—	30	—	50	—	ns	Figure 25.24

Note: * Only supporting modules that can be used in subclock operation.

Table A.3 Operation Code Map (3)

Instruction code:

1st byte		2nd byte		3rd byte		4th byte	
AH	AL	BH	BL	CH	CL	DH	DL

Instruction when most significant bit of DH is 0.
Instruction when most significant bit of DH is 1.

CL / AH AL BH BL CH	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
01C05	MULXS		MULXS													
01D05		DIVXS		DIVXS												
01F06					OR	XOR	AND									
7Cr06*1				BTST												
7Cr07*1				BTST	BOR / BIOR	BXOR / BIXOR	BAND / BIAND	BLD / BILD								
7Dr06*1	BSET	BNOT	BCLR					BST / BIST								
7Dr07*1	BSET	BNOT	BCLR													
7Eaa6*2				BTST												
7Eaa7*2				BTST	BOR / BIOR	BXOR / BIXOR	BAND / BIAND	BLD / BILD								
7Faa6*2	BSET	BNOT	BCLR					BST / BIST								
7Faa7*2	BSET	BNOT	BCLR													

Notes: 1. r is the register specification field.
2. aa is the absolute address specification.

DACR—PWM (D/A) Control Register **H'FFA0** **PWMX**

Bit	7	6	5	4	3	2	1	0
	TEST	PWME	—	—	OEB	OEA	OS	CKS
Initial value	0	0	1	1	0	0	0	0
Read/Write	R/W	R/W	—	—	R/W	R/W	R/W	R/W

Clock select

0	Resolution (T) = system clock cycle time (t_{cyc})
1	Resolution (T) = system clock cycle time (t_{cyc}) × 2

Output select

0	Direct PWM output
1	Inverted PWM output

Output enable A

0	PWM channel A output (PWX0 output pin) disabled
1	PWM channel A output (PWX0 output pin) enabled

Output enable B

0	PWM channel B output (PWX1 output pin) disabled
1	PWM channel B output (PWX1 output pin) enabled

PWM enable

0	DACNT operates as a 14-bit up-counter
1	DACNT halts at H'0003

Test mode

0	User mode: the PWM D/A module operates normally
1	Test mode: correct conversion results will not be obtained