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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	10MHz
Connectivity	Host Interface, I²C, IrDA, SCI
Peripherals	POR, PWM, WDT
Number of I/O	58
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2138avtf10v

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Configuration of This Manual

This manual comprises the following items:

1. General Precautions on Handling of Product
2. Configuration of This Manual
3. Preface
4. Main Revisions for This Edition

   The list of revisions is a summary of points that have been revised or added to earlier versions. This does not include all of the revised contents. For details, see the actual locations in this manual.
5. Contents
6 Overview
7. Description of Functional Modules
   - CPU and System-Control Modules
   - On-Chip Peripheral Modules

   The configuration of the functional description of each module differs according to the module. However, the generic style includes the following items:

   i) Feature
   ii) Input/Output Pin
   iii) Register Description
   iv) Operation
   v) Usage Note

When designing an application system that includes this LSI, take notes into account. Each section includes notes in relation to the descriptions given, and usage notes are given, as required, as the final part of each section.

8. List of Registers
9. Electrical Characteristics
10. Appendix

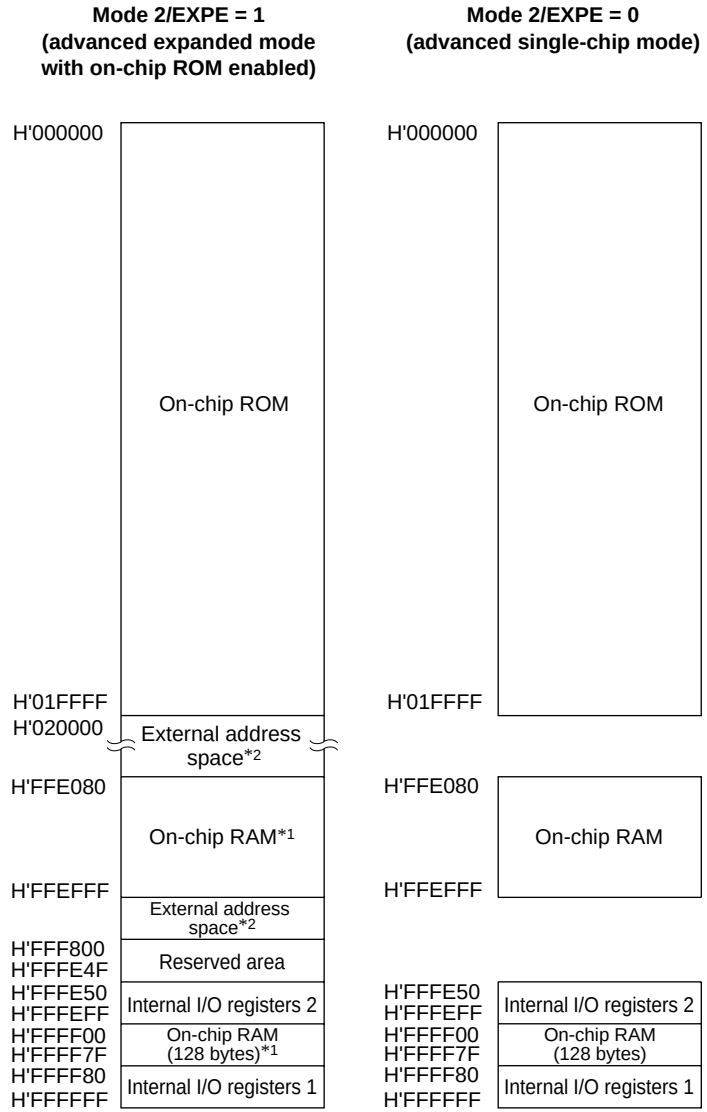
2.6.3 Table of Instructions Classified by Function

Table 2.3 summarizes the instructions in each functional category. The notation used in table 2.3 is defined below.

Operation Notation

Rd	General register (destination)*
Rs	General register (source)*
Rn	General register*
ERn	General register (32-bit register)
(EAd)	Destination operand
(EAs)	Source operand
EXR	Extended control register
CCR	Condition-code register
N	N (negative) flag in CCR
Z	Z (zero) flag in CCR
V	V (overflow) flag in CCR
C	C (carry) flag in CCR
PC	Program counter
SP	Stack pointer
#IMM	Immediate data
disp	Displacement
+	Addition
–	Subtraction
×	Multiplication
÷	Division
∧	Logical AND
∨	Logical OR
⊕	Logical exclusive OR
→	Move
¬	NOT (logical complement)
:8/:16/:24/:32	8-, 16-, 24-, or 32-bit length

Note: * General registers include 8-bit registers (R0H to R7H, R0L to R7L), 16-bit registers (R0 to R7, E0 to E7), and 32-bit registers (ER0 to ER7).



Notes: 1. External addresses can be accessed by clearing the RAME bit in SYSCR to 0.
2. For these models, the maximum number of external address pins is 16. An external address can only be specified correctly for an area that uses the I/O strobe function.

Figure 3.2 H8S/2138 F-ZTAT A-Mask Version Memory Map in Each Operating Mode (cont)

8-Bit 3-State Access Space: Figure 6.6 shows the bus timing for an 8-bit 3-state access space. When an 8-bit access space is accessed, the upper half (D15 to D8) of the data bus is used.

Wait states can be inserted.

These group have no lower data bus (D7 to D0) pins or $\overline{\text{LWR}}$ pin. In these group, the upper data bus (D15 to D8) pins are designated D7 to D0, and the $\overline{\text{HWR}}$ signal pin is designated $\overline{\text{WR}}$.

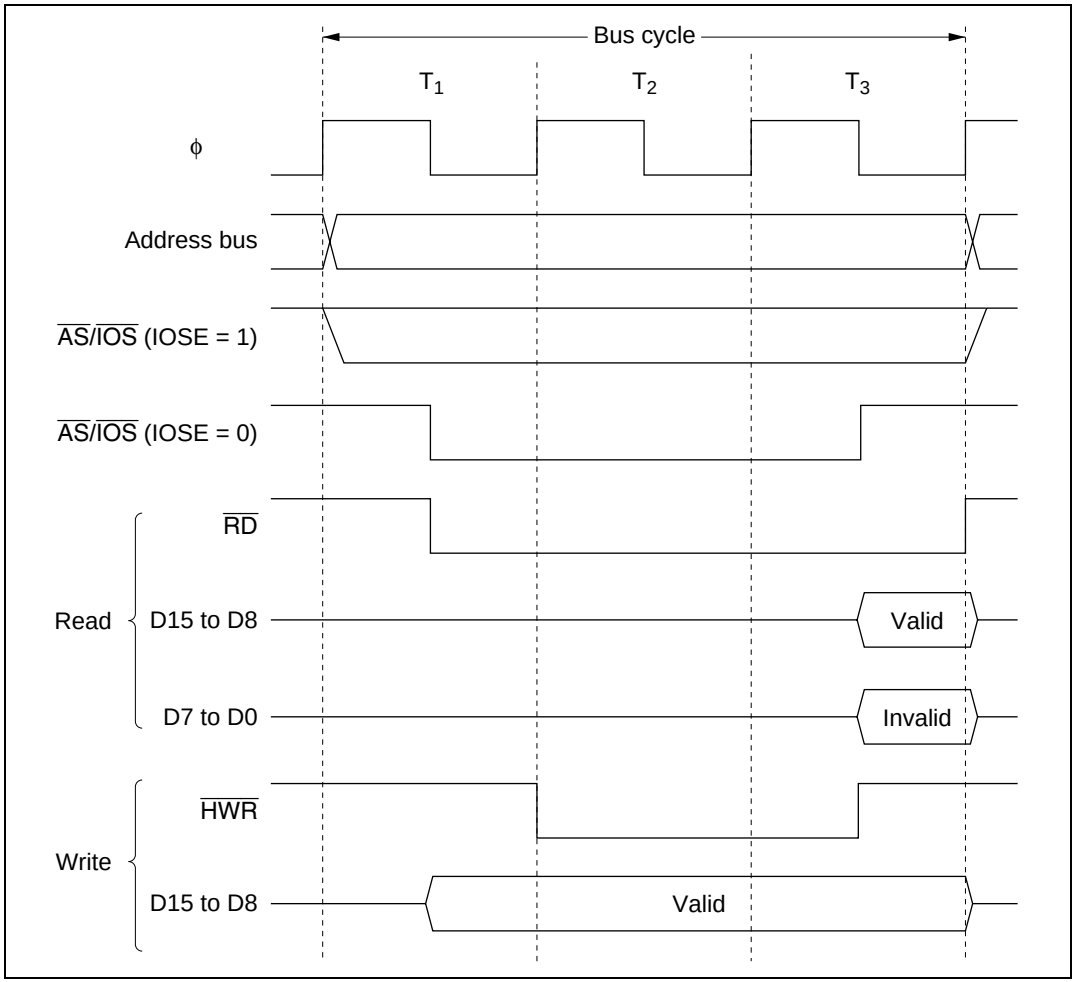


Figure 6.6 Bus Timing for 8-Bit 3-State Access Space

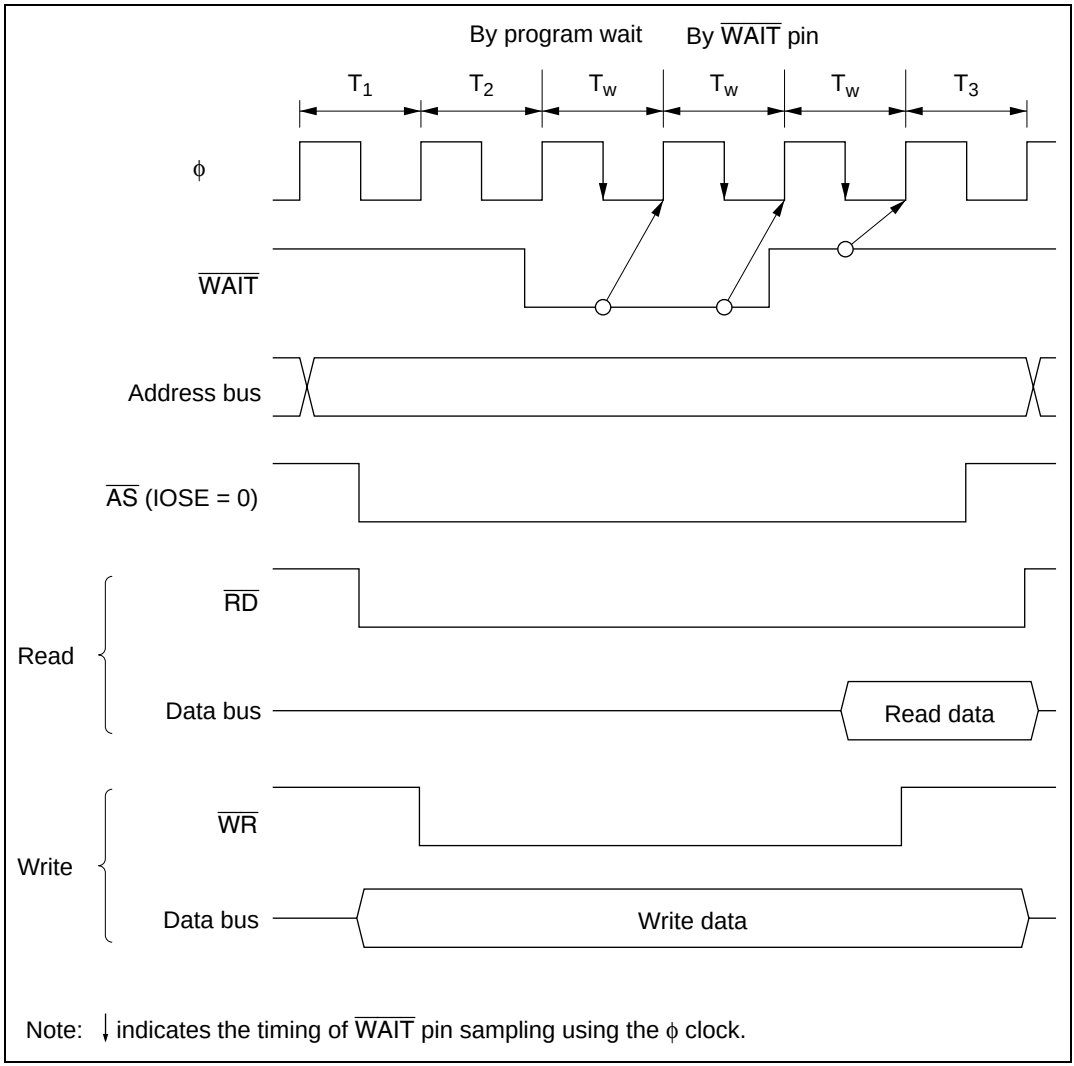


Figure 6.7 Example of Wait State Insertion Timing

The settings after a reset are: 3-state access, insertion of 3 program wait states, and WAIT input disabled.

7.2.6 DTC Transfer Count Register B (CRB)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
Read/Write	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

CRB is a 16-bit register that designates the number of times data is to be transferred by the DTC in block transfer mode. It functions as a 16-bit transfer counter (1 to 65,536) that is decremented by 1 every time data is transferred, and transfer ends when the count reaches H'0000.

7.2.7 DTC Enable Registers (DTCER)

Bit	7	6	5	4	3	2	1	0
	DTCE7	DTCE6	DTCE5	DTCE4	DTCE3	DTCE2	DTCE1	DTCE0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The DTC enable registers comprise five 8-bit readable/writable registers, DTCERA to DTCERE, with bits corresponding to the interrupt sources that can activate the DTC. These bits enable or disable DTC service for the corresponding interrupt sources.

The DTC enable registers are initialized to H'00 by a reset and in hardware standby mode.

Bit n—DTC Activation Enable (DTCEn)

Bit n DTCEn	Description	
0	DTC activation by interrupt is disabled [Clearing conditions] • When data transfer ends with the DISEL bit set to 1 • When the specified number of transfers end	(Initial value)
1	DTC activation by interrupt is enabled [Holding condition] When the DISEL bit is 0 and the specified number of transfers have not ended	

(n = 7 to 0)

8.3.4 MOS Input Pull-Up Function

Port 2 has an on-chip MOS input pull-up function that can be controlled by software. This MOS input pull-up function can be used in modes 2 and 3, and can be specified as on or off on a bit-by-bit basis.

When a P2DDR bit is cleared to 0 in mode 2 or 3, setting the corresponding P2PCR bit to 1 turns on the MOS input pull-up for that pin.

The MOS input pull-up function is in the off state after a reset and in hardware standby mode. The prior state is retained in software standby mode.

Table 8.6 summarizes the MOS input pull-up states.

Table 8.6 MOS Input Pull-Up States (Port 2)

Mode	Reset	Hardware Standby Mode	Software Standby Mode	In Other Operations
1	Off	Off	Off	Off
2, 3	Off	Off	On/Off	On/Off

Legend:

Off: MOS input pull-up is always off.

On/Off: On when P2DDR = 0 and P2PCR = 1; otherwise off.

8.5 Port 4

8.5.1 Overview

Port 4 is an 8-bit I/O port. Port 4 pins also function as 14-bit PWM output pins (PWX1, PWX0), 8-bit timer 0 and 1 (TMR0, TMR1) I/O pins (TMCI0, TMRI0, TMO0, TMCI1, TMRI1, TMO1), timer connection I/O pins (CSYNCI, HSYNCI, HSYNCO) (H8S/2138 Group only), SCI2 I/O pins (TxD2, RxD2, SCK2), IrDA interface I/O pins (IrTxD, IrRxD), host interface output pins (HIRQ12, HIRQ1, HIRQ11) (H8S/2138 Group only), and the IIC1 I/O pin (SDA1) (option in H8S/2138 Group only). Port 4 pin functions are the same in all operating modes.

Figure 8.12 shows the port 4 pin configuration.

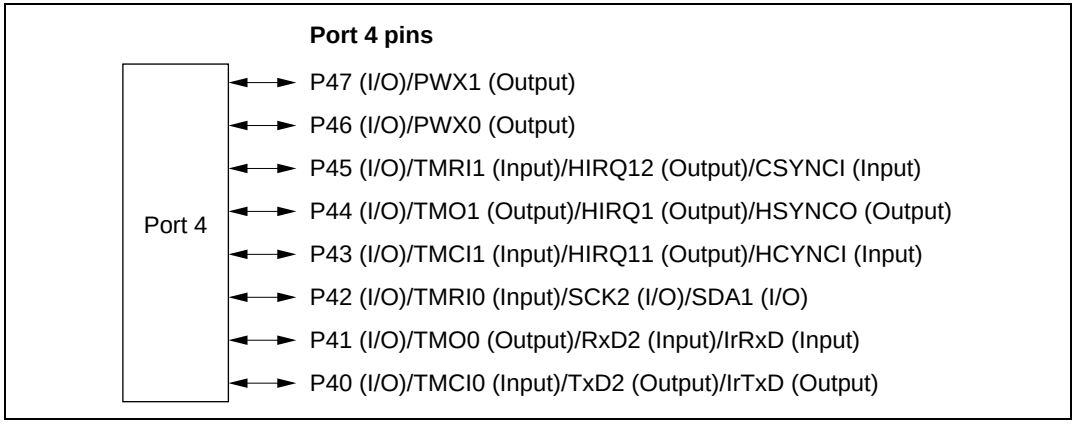


Figure 8.12 Port 4 Pin Functions

8.5.2 Register Configuration

Table 8.9 shows the port 4 register configuration.

Table 8.9 Port 4 Registers

Name	Abbreviation	R/W	Initial Value	Address*
Port 4 data direction register	P4DDR	W	H'00	H'FFB5
Port 4 data register	P4DR	R/W	H'00	H'FFB7

Note: * Lower 16 bits of the address.

Section 9 8-Bit PWM Timers [H8S/2138 Group]

9.1 Overview

The H8/2138 Group has an on-chip pulse width modulation (PWM) timer module with sixteen outputs. Sixteen output waveforms are generated from a common time base, enabling PWM output with a high carrier frequency to be produced using pulse division. The PWM timer module has sixteen 8-bit PWM data registers (PWDRs), and an output pulse with a duty cycle of 0 to 100% can be obtained as specified by PWDR and the port data register (P1DR or P2DR).

9.1.1 Features

The PWM timer module has the following features.

- Operable at a maximum carrier frequency of 1.25 MHz using pulse division (at 20-MHz operation)
- Duty cycles from 0 to 100% with 1/256 resolution (100% duty realized by port output)
- Direct or inverted PWM output, and PWM output enable/disable control

11.3.9 ICRD and OCRDM Mask Signal Generation

When the ICRDMS bit in TOCR is set to 1 and the contents of OCRDM are other than H'0000, a signal that masks the ICRD input capture function is generated.

The mask signal is set by the input capture signal. The mask signal setting timing is shown in figure 11.15.

The mask signal is cleared by the sum of the ICRD contents and twice the OCRDM contents, and an FRC compare-match. The mask signal clearing timing is shown in figure 11.16.

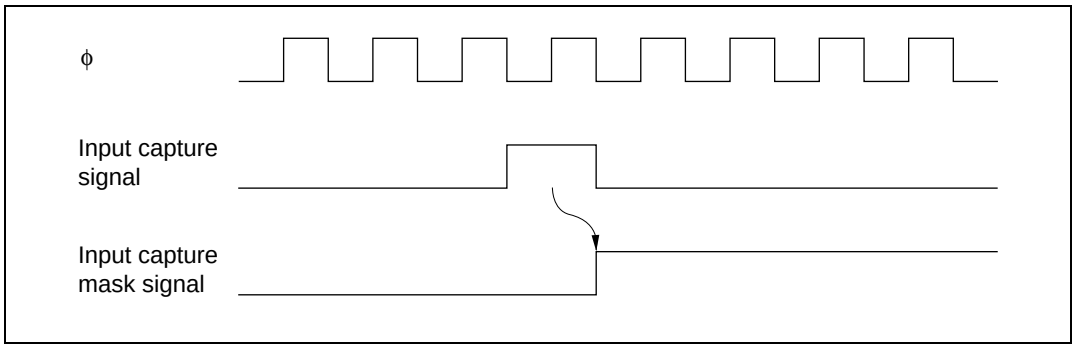


Figure 11.15 Input Capture Mask Signal Setting Timing

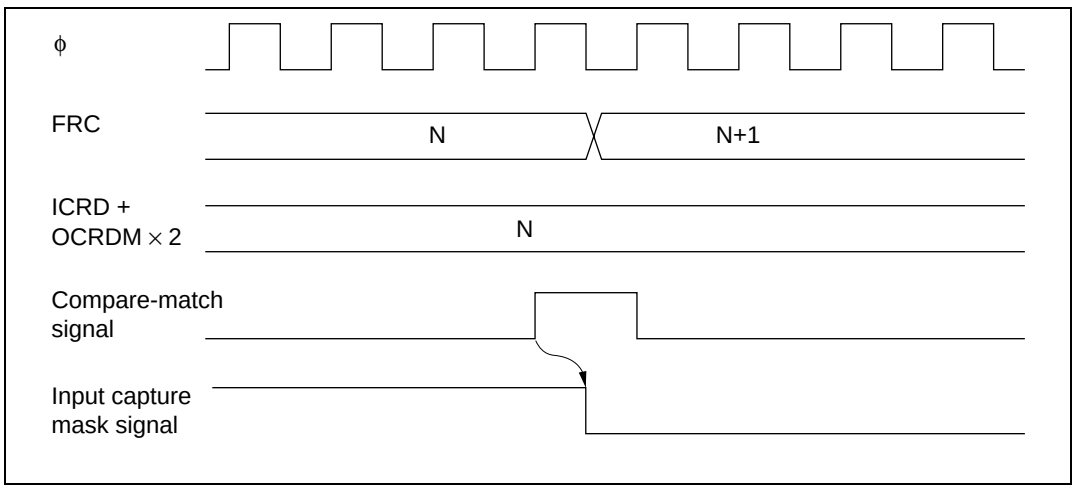


Figure 11.16 Input Capture Mask Signal Clearing Timing

16.3.5 Slave Transmit Operation

In slave transmit mode, the slave device outputs the transmit data, while the master device outputs the receive clock and returns an acknowledge signal. The transmission procedure and operations in slave transmit mode are described below.

[1] Set the ICE bit in ICCR to 1. Set the MLS bit in ICMR and the MST and TRS bits in ICCR according to the operating mode.

[2] When the slave address matches in the first frame following detection of the start condition, the slave device drives SDA low at the 9th clock pulse and returns an acknowledge signal. At the same time, the IRIC flag in ICCR is set to 1. If the IEIC bit in ICCR has been set to 1, an interrupt request is sent to the CPU. .If the 8th data bit (R/$\overline{W}$) is 1, the TRS bit in ICCR is set to 1, and the mode changes to slave transmit mode automatically. The TDRE internal flag is set to 1. The slave device drives SCL low from the fall of the transmit clock until ICDR data is written.

[3] After clearing the IRIC flag to 0, write data to ICDR. The TDRE internal flag is cleared to 0. The written data is transferred to ICDRS, and the TDRE internal flag and the IRIC and IRTR flags are set to 1 again. After clearing the IRIC flag to 0, write the next data to ICDR. The slave device sequentially sends the data written into ICDR in accordance with the clock output by the master device at the timing shown in figure 16.11.

[4] When one frame of data has been transmitted, the IRIC flag in ICCR is set to 1 at the rise of the 9th transmit clock pulse. If the TDRE internal flag has been set to 1, this slave device drives SCL low from the fall of the transmit clock until data is written to ICDR. The master device drives SDA low at the 9th clock pulse, and returns an acknowledge signal. As this acknowledge signal is stored in the ACKB bit in ICSR, this bit can be used to determine whether the transfer operation was performed normally. When the TDRE internal flag is 0, the data written into ICDR is transferred to ICDRS, transmission is started, and the TDRE internal flag and the IRIC and IRTR flags are set to 1 again.

[5] To continue transmission, clear the IRIC flag to 0, then write the next data to be transmitted into ICDR. The TDRE internal flag is cleared to 0.

Transmit operations can be performed continuously by repeating steps [4] and [5]. To end transmission, write H'FF to ICDR to release SDA on the slave side. When SDA is changed from low to high when SCL is high, and the stop condition is detected, the BBSY flag in ICCR is cleared to 0.

Bit 3	Bit 2	Bit 1	Bit 0	A/D Converter	A/D Converter
KBADE	KBCH2	KBCH1	KBCH0	Channel 6 Input	Channel 7 Input
0	—	—	—	AN6	AN7
1	0	0	0	CIN0	Undefined
			1	CIN1	Undefined
		1	0	CIN2	Undefined
			1	CIN3	Undefined
	1	0	0	CIN4	Undefined
			1	CIN5	Undefined
		1	0	CIN6	Undefined
			1	CIN7	Undefined

19.2.5 Module Stop Control Register (MSTPCR)

	MSTPCRH								MSTPCRL							
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	MSTP15	MSTP14	MSTP13	MSTP12	MSTP11	MSTP10	MSTP9	MSTP8	MSTP7	MSTP6	MSTP5	MSTP4	MSTP3	MSTP2	MSTP1	MSTP0
Initial value	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MSTPCR, comprising two 8-bit readable/writable registers, performs module stop mode control.

When the MSTP9 bit in MSTPCR is set to 1, A/D converter operation stops at the end of the bus cycle and a transition is made to module stop mode. Registers cannot be read or written to in module stop mode. For details, see section 24.5, Module Stop Mode.

MSTPCR is initialized to H'3FFF by a reset and in hardware standby mode. It is not initialized in software standby mode.

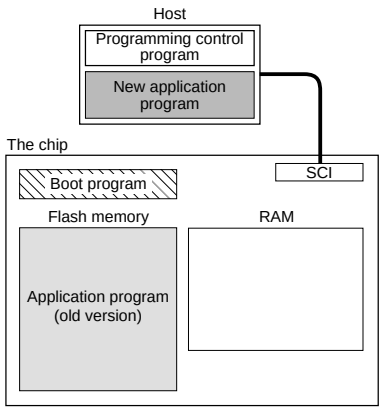
MSTPCRH Bit 1—Module Stop (MSTP9): Specifies the A/D converter module stop mode.

MSTPCRH Bit 1		
MSTP9	Description	
0	A/D converter module stop mode is cleared	
1	A/D converter module stop mode is set	(Initial value)

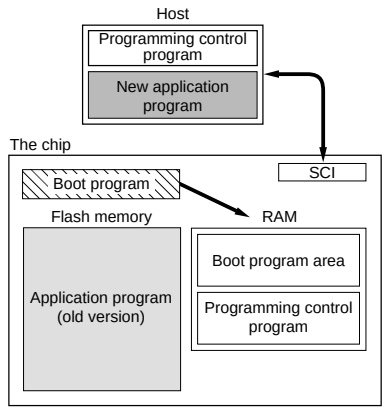
On-Board Programming Modes

- Boot mode

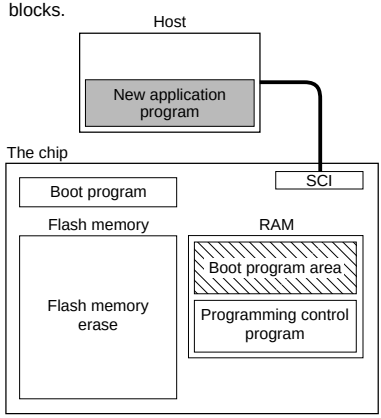
1. Initial state
   The flash memory is in the erased state when the device is shipped. The description here applies to the case where the old program version or data is being rewritten. The user should prepare the programming control program and new application program beforehand in the host.



2. Programming control program transfer
   When boot mode is entered, the boot program in the chip (originally incorporated in the chip) is started, an SCI communication check is carried out, and the boot program required for flash memory erasing is automatically transferred to the RAM boot program area.



3. Flash memory initialization
   The erase program in the boot program area (in RAM) is executed, and the flash memory is initialized (to H'FF). In boot mode, entire flash memory erasure is performed, without regard to blocks.



4. Writing new application program
   The programming control program transferred from the host to RAM by SCI communication is executed, and the new application program in the host is written into the flash memory.

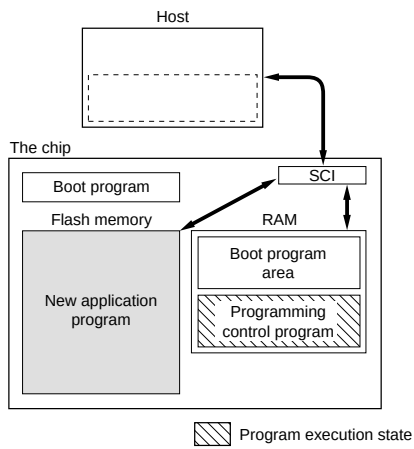


Figure 22.4 Boot Mode

MSTRCRH and MSTPCRL Bits 7 to 0—Module Stop (MSTP 15 to MSTP 0): These bits specify module stop mode. See table 24.4 for the method of selecting on-chip supporting modules.

MSTPCRH, MSTPCRL Bits 7 to 0

MSTP15 to MSTP0	Description	
0	Module stop mode is cleared	(Initial value of MSTP15, MSTP14)
1	Module stop mode is set	(Initial value of MSTP13 to MSTP0)

24.3 Medium-Speed Mode

When the SCK2 to SCK0 bits in SBYCR are set to 1 in high-speed mode, the operating mode changes to medium-speed mode at the end of the bus cycle. In medium-speed mode, the CPU operates on the operating clock (ϕ/2, ϕ/4, ϕ/8, ϕ/16, or ϕ/32) specified by the SCK2 to SCK0 bits. The bus master other than the CPU (the DTC) also operates in medium-speed mode. On-chip supporting modules other than the bus masters always operate on the high-speed clock (ϕ).

In medium-speed mode, a bus access is executed in the specified number of states with respect to the bus master operating clock. For example, if ϕ/4 is selected as the operating clock, on-chip memory is accessed in 4 states, and internal I/O registers in 8 states.

Medium-speed mode is cleared by clearing all of bits SCK2 to SCK0 to 0. A transition is made to high-speed mode and medium-speed mode is cleared at the end of the current bus cycle.

If a SLEEP instruction is executed when the SSBY bit in SBYCR and the LSON bit in LPWRCR are cleared to 0, a transition is made to sleep mode. When sleep mode is cleared by an interrupt, medium-speed mode is restored.

If a SLEEP instruction is executed when the SSBY bit in SBYCR is set to 1, and the LSON bit in LPWRCR and the PSS bit in TCSR (WDT1) are both cleared to 0, a transition is made to software standby mode. When software standby mode is cleared by an external interrupt, medium-speed mode is restored.

When the $\overline{\text{RES}}$ pin is driven low, a transition is made to the reset state, and medium-speed mode is cleared. The same applies in the case of a reset caused by overflow of the watchdog timer.

When the $\overline{\text{STBY}}$ pin is driven low, a transition is made to hardware standby mode.

Figure 24.2 shows the timing for transition to and clearance of medium-speed mode.

24.8 Watch Mode

24.8.1 Watch Mode

If a SLEEP instruction is executed in high-speed mode or subactive mode when the SSBY in SBYCR is set to 1, the DTON bit in LPWRCR is cleared to 0, and the PSS bit in TCSR (WDT1) is set to 1, the CPU makes a transition to watch mode.

In this mode, the CPU and all on-chip supporting modules except WDT1 stop. As long as the prescribed voltage is supplied, the contents of some of the CPU's internal registers and on-chip RAM are retained, and I/O ports retain their states prior to the transition.

24.8.2 Clearing Watch Mode

Watch mode is cleared by an interrupt (WOVI1 interrupt, NMI pin, or pin $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, $\overline{\text{IRQ2}}$, $\overline{\text{IRQ6}}$, or $\overline{\text{IRQ7}}$), or by means of the $\overline{\text{RES}}$ pin or $\overline{\text{STBY}}$ pin.

Clearing with an Interrupt: When an interrupt request signal is input, watch mode is cleared and a transition is made to high-speed mode or medium-speed mode if the LSON bit in LPWRCR is cleared to 0, or to subactive mode if the LSON bit is set to 1. When making a transition to high-speed mode, after the elapse of the time set in bits STS2 to STS0 in SBYCR, stable clocks are supplied to the entire chip, and interrupt exception handling is started.

Watch mode cannot be cleared with an IRQ0, IRQ1, IRQ2, IRQ6, or IRQ7 interrupt if the corresponding enable bit has been cleared to 0, or with an on-chip supporting module interrupt if acceptance of the relevant interrupt has been disabled by the interrupt enable register or masked by the CPU.

See section 24.6.3, Setting Oscillation Settling Time after Clearing Software Standby Mode, for the oscillation settling time setting when making a transition from watch mode to high-speed mode.

Clearing with the $\overline{\text{RES}}$ Pin: See "Clearing with the $\overline{\text{RES}}$ Pin" in section 24.6.2, Clearing Software Standby Mode.

Clearing with the $\overline{\text{STBY}}$ Pin: When the $\overline{\text{STBY}}$ pin is driven low, a transition is made to hardware standby mode.

Table 25.10 I²C Bus Timing

Conditions: V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0 V, ϕ = 5 MHz to maximum operating frequency, T_a = –20 to +75°C

		Ratings					
Item	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	**Notes**
SCL clock cycle time	t_{SCL}	12	—	—	t_{cyc}		Figure 25.26
SCL clock high pulse width	t_{SCLH}	3	—	—	t_{cyc}		
SCL clock low pulse width	t_{SCLL}	5	—	—	t_{cyc}		
SCL, SDA input rise time	t_{Sr}	—	—	7.5*	t_{cyc}		
SCL, SDA input fall time	t_{Sf}	—	—	300	ns		
SCL, SDA input spike pulse elimination time	t_{SP}	—	—	1	t_{cyc}		
SDA input bus free time	t_{BUF}	5	—	—	t_{cyc}		
Start condition input hold time	t_{STAH}	3	—	—	t_{cyc}		
Retransmission start condition input setup time	t_{STAS}	3	—	—	t_{cyc}		
Stop condition input setup time	t_{STOS}	3	—	—	t_{cyc}		
Data input setup time	t_{SDAS}	0.5	—	—	t_{cyc}		
Data input hold time	t_{SDAH}	0	—	—	ns		
SCL, SDA capacitive load	C_b	—	—	400	pF		

Note: * $17.5t_{cyc}$ can be set according to the clock selected for use by the I²C module. For details, see section 16.4, Usage Notes.

Instruction	Mnemonic		Instruction Fetch I	Branch Address Read J	Stack Operation K	Byte Data Access L	Word Data Access M	Internal Operation N
ROTR	ROTR.B Rd		1					
	ROTR.B #2,Rd		1					
	ROTR.W Rd		1					
	ROTR.W #2,Rd		1					
	ROTR.L ERd		1					
	ROTR.L #2,ERd		1					
ROTXL	ROTXL.B Rd		1					
	ROTXL.B #2,Rd		1					
	ROTXL.W Rd		1					
	ROTXL.W #2,Rd		1					
	ROTXL.L ERd		1					
	ROTXL.L #2,ERd		1					
ROTXR	ROTXR.B Rd		1					
	ROTXR.B #2,Rd		1					
	ROTXR.W Rd		1					
	ROTXR.W #2,Rd		1					
	ROTXR.L ERd		1					
	ROTXR.L #2,ERd		1					
RTE	RTE		2		2/3*1			1
RTS	RTS	Normal	2		1			1
		Advanced	2		2			1
SHAL	SHAL.B Rd		1					
	SHAL.B #2,Rd		1					
	SHAL.W Rd		1					
	SHAL.W #2,Rd		1					
	SHAL.L ERd		1					
	SHAL.L #2,ERd		1					
SHAR	SHAR.B Rd		1					
	SHAR.B #2,Rd		1					
	SHAR.W Rd		1					
	SHAR.W #2,Rd		1					
	SHAR.L ERd		1					
	SHAR.L #2,ERd		1					

TCSR1—Timer Control/Status Register 1 H'FFEA WDT1

TCSR1

Bit	7	6	5	4	3	2	1	0
	OVF	WT/$\overline{IT}$	TME	PSS	RST/$\overline{NMI}$	CKS2	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*1	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock select 2 to 0

PSS	CKS2	CKS1	CKS0	Clock
0	0	0	0	φ/2
			1	φ/64
		1	0	φ/128
			1	φ/512
	1	0	0	φ/2048
			1	φ/8192
		1	0	φ/32768
			1	φ/131072
1	0	0	0	φSUB/2
			1	φSUB/4
		1	0	φSUB/8
			1	φSUB/16
	1	0	0	φSUB/32
			1	φSUB/64
		1	0	φSUB/128
			1	φSUB/256

Reset or NMI

0	NMI interrupt requested
1	Internal reset requested

Prescaler select*2

0	TCNT counts on a φ-based prescaler (PSM) scaled clock
1	TCNT counts on a φSUB-based prescaler (PSS) scaled clock

Timer enable

0	TCNT is initialized to H'00 and halted
1	TCNT counts

Timer mode select

0	Interval timer mode: Interval timer interrupt request (WOVI) sent to CPU when TCNT overflows
1	Watchdog timer mode: Reset or NMI interrupt request sent to CPU when TCNT overflows

Overflow flag

0	[Clearing conditions] • When 0 is written in the TME bit • When 0 is written in OVF after reading TCSR when OVF = 1
1	[Setting condition] When TCNT overflows from H'FF to H'00 When internal reset request is selected in watchdog timer mode, OVF is cleared automatically by an internal reset after being set

Notes: 1. Only 0 can be written, to clear the flag.
2. For operation control when a transition is made to power-down mode, see section 24.2.3, Timer Control/Status Register (TCSR).