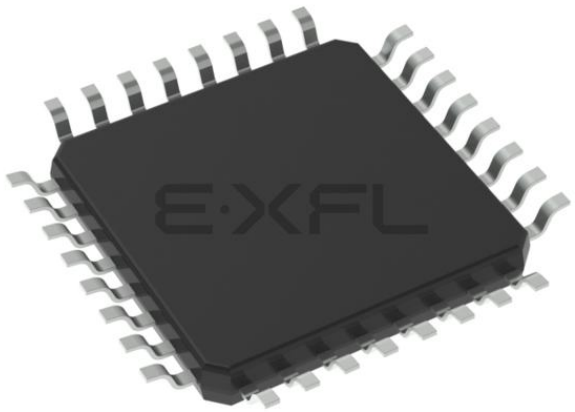

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, WDT
Number of I/O	26
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-TQFP
Supplier Device Package	32-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamc20e18a-aut

1. Description

The Atmel SAM C20 devices provide the following features: In-system programmable Flash, six-channel direct memory access (DMA) controller, six-channel Event System, programmable interrupt controller, up to 52 programmable I/O pins, 32-bit real-time clock and calendar, up to five 16-bit Timer/Counters (TC) and three Timer/Counters for Control (TCC), where each TC can be configured to perform frequency and waveform generation, accurate program execution timing or input capture with time and frequency measurement of digital signals. The TCs can operate in 8- or 16-bit mode, selected TCs can be cascaded to form a 32-bit TC, and three timer/counters have extended functions optimized for motor, lighting and other control applications. Two TCC can operate in 24-bit mode, and the third TCC can operate in 16- bit mode. The series provide up to four Serial Communication Modules (SERCOM) that each can be configured to act as an USART, UART, SPI, I^2C up to 3.4MHz, SMBus, RS-485 and LIN master/slave; one 12-bit, 1Msps ADC with up to 12-channels , two analog comparators with window mode, Peripheral Touch Controller supporting up to 256 buttons, sliders, wheels and proximity sensing; programmable Watchdog Timer, brown-out detector and power-on reset and two-pin Serial Wire Debug (SWD) program and debug interface.

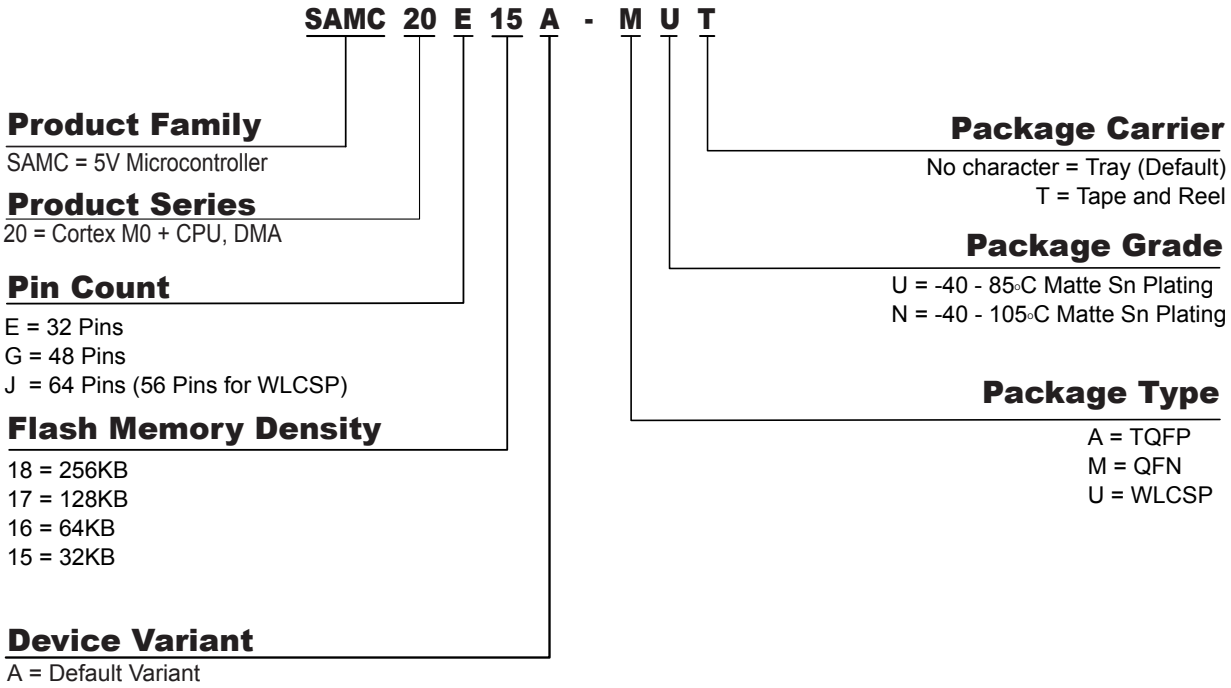
All devices have accurate and low-power external and internal oscillators. All oscillators can be used as a source for the system clock. Different clock domains can be independently configured to run at different frequencies, enabling power saving by running each peripheral at its optimal clock frequency, and thus maintaining a high CPU frequency while reducing power consumption.

The SAM C20 devices have three software-selectable sleep modes, idle, standby and off. In idle mode the CPU is stopped while all other functions can be kept running. In standby all clocks and functions are stopped expect those selected to continue running. In this mode all RAMs and logic contents are retained. The device supports SleepWalking. This feature allows the peripheral to wake up from sleep based on predefined conditions, and thus allows some internal operation like DMA transfer and/or the CPU to wake up only when needed, e.g. when a threshold is crossed or a result is ready. The Event System supports synchronous and asynchronous events, allowing peripherals to receive, react to and send events even in standby mode.

The Flash program memory can be reprogrammed in-system through the SWD interface. The same interface can be used for non-intrusive on-chip debug of application code. A boot loader running in the device can use any communication interface to download and upgrade the application program in the Flash memory.

The Atmel SAM C20 devices are supported with a full suite of program and system development tools, including C compilers, macro assemblers, program debugger/simulators, programmers and evaluation kits.

3. Ordering Information



3.1. SAM C20E

Table 3-1. SAM C20E15A Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type	Temp
ATSAM C20E15A-AUT	32K	4K	TQFP32	Tape & Reel	85°C
ATSAM C20E15A-ANT	32K	4K	TQFP32	Tape & Reel	105°C
ATSAM C20E15A-MUT	32K	4K	QFN32	Tape & Reel	85°C
ATSAM C20E15A-MNT	32K	4K	QFN32	Tape & Reel	105°C

Table 3-2. SAM C20E16A Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type	Temp
ATSAM C20E16A-AUT	64K	8K	TQFP32	Tape & Reel	85°C
ATSAM C20E16A-ANT	64K	8K	TQFP32	Tape & Reel	105°C
ATSAM C20E16A-MUT	64K	8K	QFN32	Tape & Reel	85°C
ATSAM C20E16A-MNT	64K	8K	QFN32	Tape & Reel	105°C

Table 3-3. SAM C20E17A Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type	Temp
ATSAM C20E17A-AUT	128K	16K	TQFP32	Tape & Reel	85°C
ATSAM C20E17A-ANT	128K	16K	TQFP32	Tape & Reel	105°C
ATSAM C20E17A-MUT	128K	16K	QFN32	Tape & Reel	85°C
ATSAM C20E17A-MNT	128K	16K	QFN32	Tape & Reel	105°C

Table 3-4. SAM C20E18A Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type	Temp
ATSAM C20E18A-AUT	256K	32K	TQFP32	Tape & Reel	85°C
ATSAM C20E18A-ANT	256K	32K	TQFP32	Tape & Reel	105°C
ATSAM C20E18A-MUT	256K	32K	QFN32	Tape & Reel	85°C
ATSAM C20E18A-MNT	256K	32K	QFN32	Tape & Reel	105°C

3.2. SAM C20G

Table 3-5. SAM C20G15A Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type	Temp
ATSAM C20G15A-AUT	32K	4K	TQFP48	Tape & Reel	85°C
ATSAM C20G15A-ANT	32K	4K	TQFP48	Tape & Reel	105°C
ATSAM C20G15A-MUT	32K	4K	QFN48	Tape & Reel	85°C
ATSAM C20G15A-MNT	32K	4K	QFN48	Tape & Reel	105°C

Table 3-6. SAM C20G16A Ordering Codes

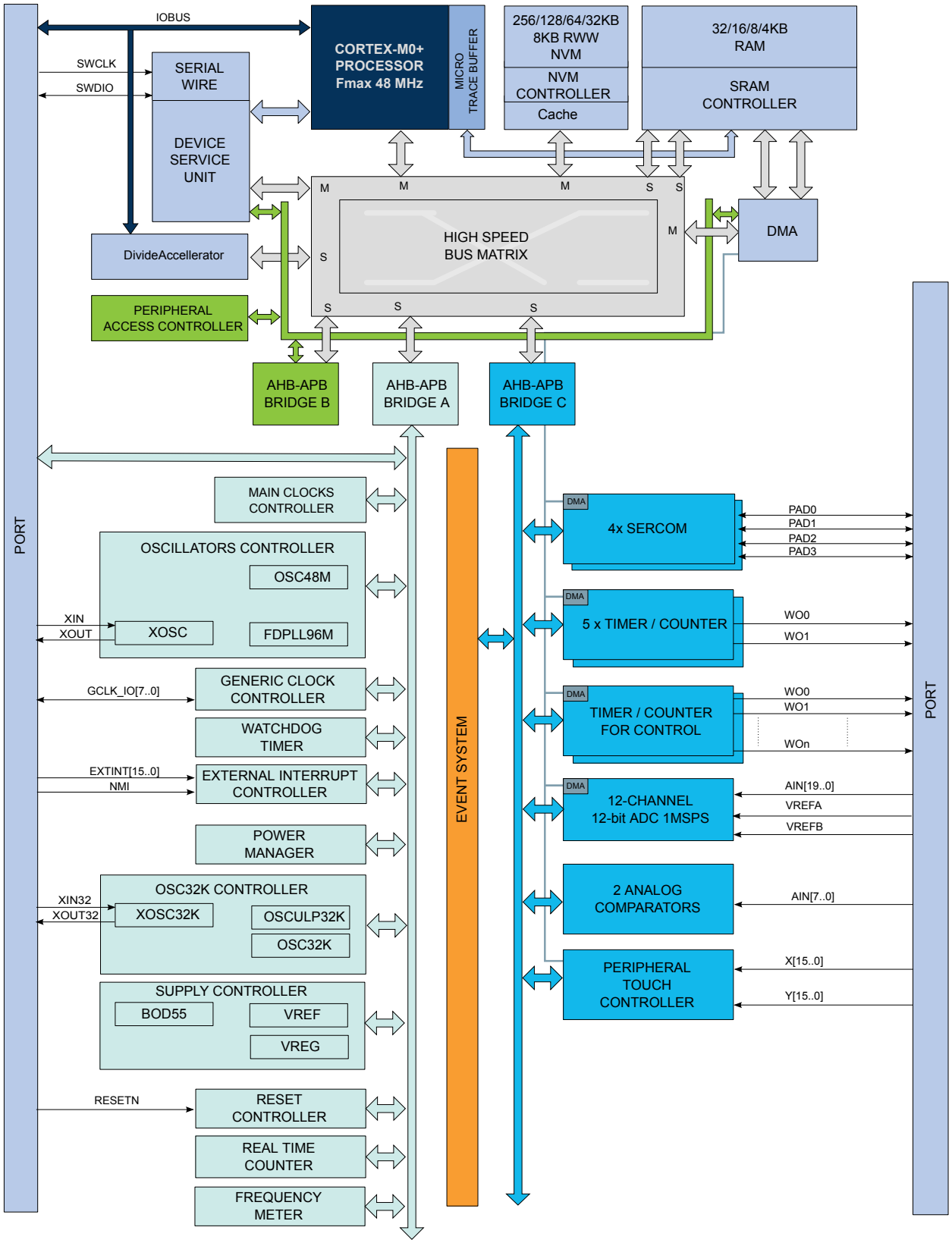
Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type	Temp
ATSAM C20G16A-AUT	64K	8K	TQFP48	Tape & Reel	85°C
ATSAM C20G16A-ANT	64K	8K	TQFP48	Tape & Reel	105°C
ATSAM C20G16A-MUT	64K	8K	QFN48	Tape & Reel	85°C
ATSAM C20G16A-MNT	64K	8K	QFN48	Tape & Reel	105°C

DEVSEL (DID[7:0])	Device
0x09	Reserved
0x0A	SAM C20E18A
0x0B	SAM C20E17A
0x0C	SAM C20E16A
0x0D	SAM C20E15A
0x0E-0xFF	Reserved

Note: The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die.

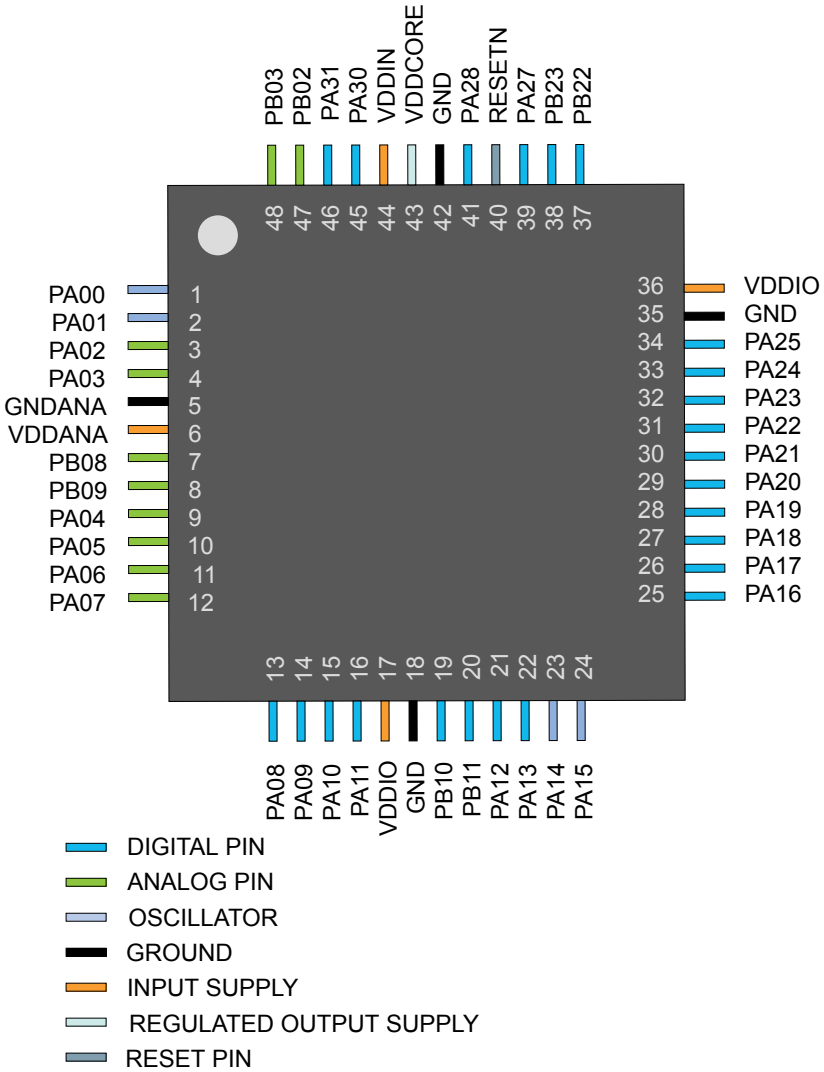
4. Block Diagram

Figure 4-1. System Block Diagram for SAM C20E/G/J



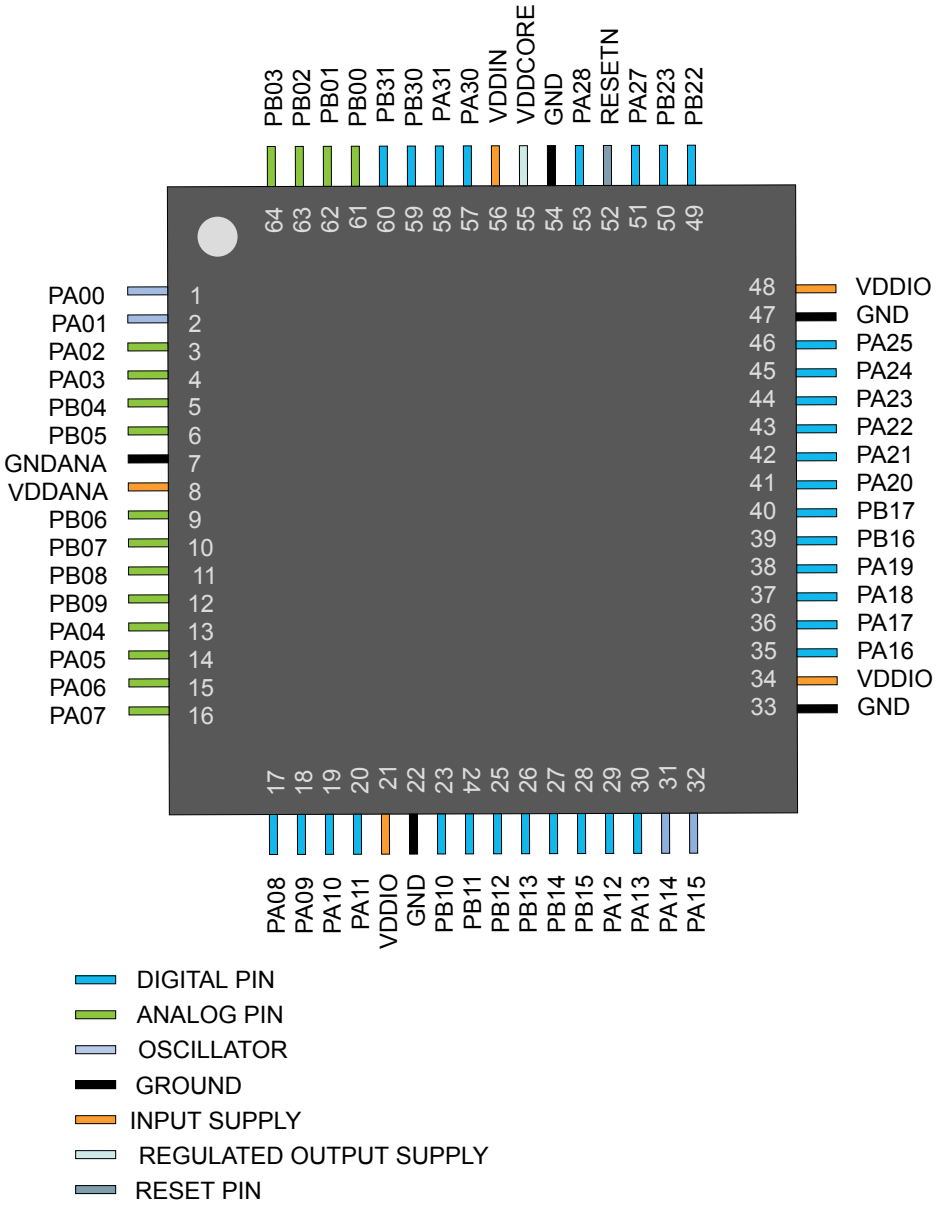
5.2. SAM C20G

5.2.1. QFN48 / TQFP48

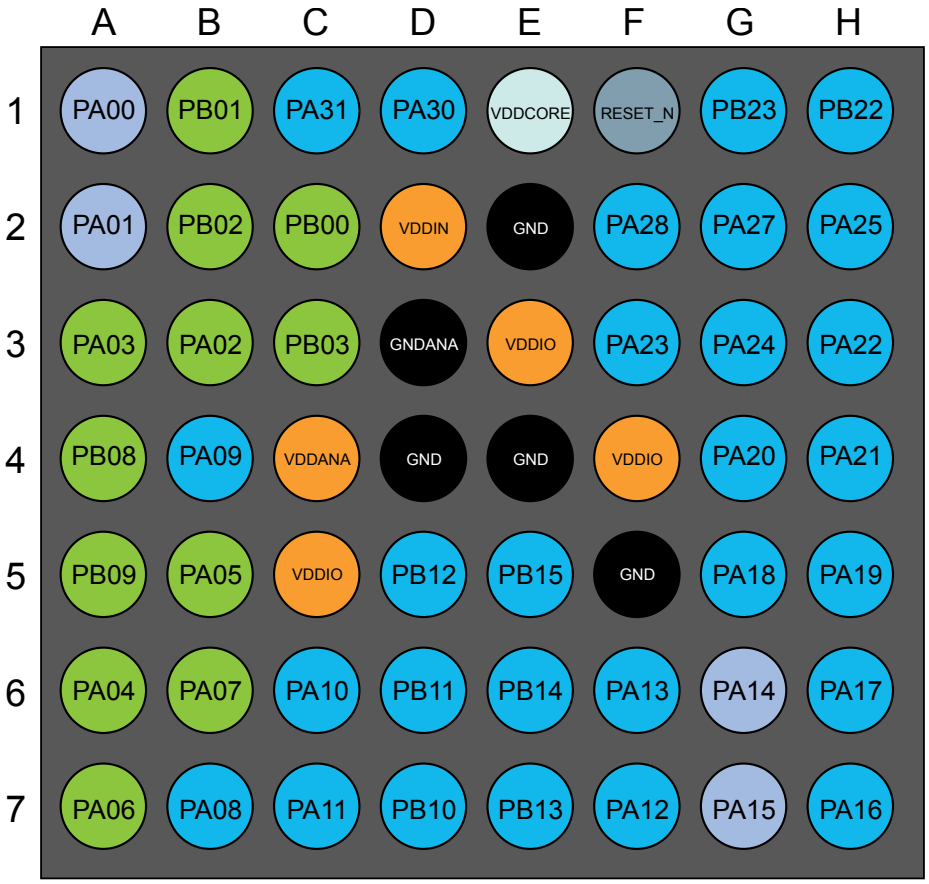


5.3. SAM C20J

5.3.1. QFN64 / TQFP64



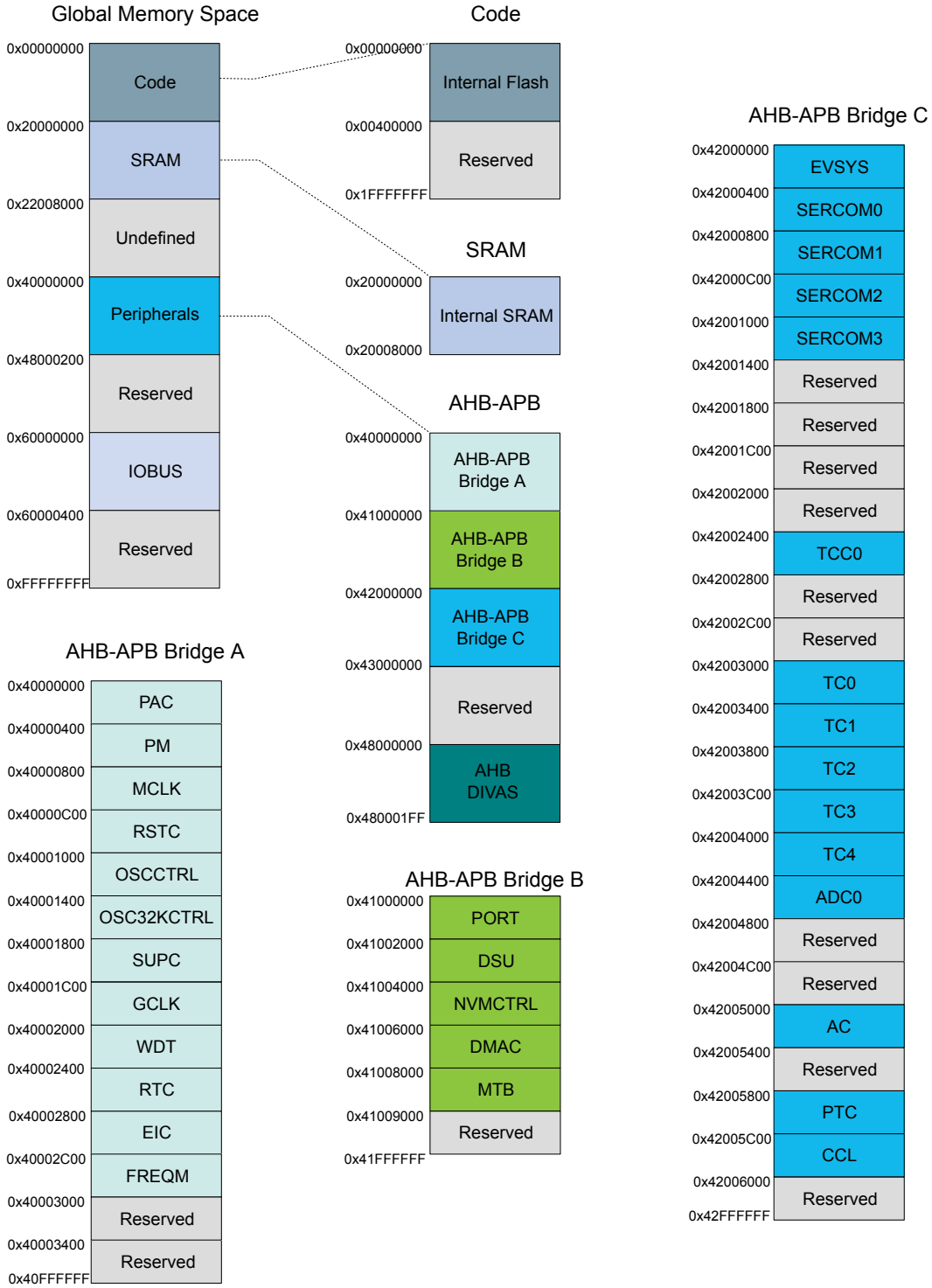
5.3.2. WLCSP56


A B C D E F G H
1 PA00 PB01 PA31 PA30 VDDCORE RESET_N PB23 PB22
2 PA01 PB02 PB00 VDDIN GND PA28 PA27 PA25
3 PA03 PA02 PB03 GNDANA VDDIO PA23 PA24 PA22
4 PB08 PA09 VDDANA GND GND VDDIO PA20 PA21
5 PB09 PA05 VDDIO PB12 PB15 GND PA18 PA19
6 PA04 PA07 PA10 PB11 PB14 PA13 PA14 PA17
7 PA06 PA08 PA11 PB10 PB13 PA12 PA15 PA16
DIGITAL PIN
ANALOG PIN
OSCILLATOR
GROUND
INPUT SUPPLY
REGULATED OUTPUT SUPPLY
RESET PIN

Signal Name	Function	Type	Active Level
PA28 - PA27	Parallel I/O Controller I/O Port A	Digital	
PA31 - PA30	Parallel I/O Controller I/O Port A	Digital	
PB17 - PB00	Parallel I/O Controller I/O Port B	Digital	
PB23 - PB22	Parallel I/O Controller I/O Port B	Digital	
PB31 - PB30	Parallel I/O Controller I/O Port B	Digital	

8. Product Mapping

Figure 8-1. SAM C20 Product Mapping



9.2.2. Interrupt Line Mapping

Each of the interrupt lines is connected to one peripheral instance, as shown in the table below. Each peripheral can have one or more interrupt flags, located in the peripheral's Interrupt Flag Status and Clear (INTFLAG) register.

The interrupt flag is set when the interrupt condition occurs. Each interrupt in the peripheral can be individually enabled by writing a one to the corresponding bit in the peripheral's Interrupt Enable Set (INTENSET) register, and disabled by writing a one to the corresponding bit in the peripheral's Interrupt Enable Clear (INTENCLR) register.

An interrupt request is generated from the peripheral when the interrupt flag is set and the corresponding interrupt is enabled.

The interrupt requests for one peripheral are ORed together on system level, generating one interrupt request for each peripheral. An interrupt request will set the corresponding interrupt pending bit in the NVIC interrupt pending registers (SETPEND/CLRPEND bits in ISPR/ICPR).

For the NVIC to activate the interrupt, it must be enabled in the NVIC interrupt enable register (SETENA/CLRENA bits in ISER/ICER). The NVIC interrupt priority registers IPR0-IPR7 provide a priority field for each interrupt.

Table 9-3. Interrupt Line Mapping

Peripheral Source	NVIC Line
EIC NMI – External Interrupt Controller	NMI
PM – Power Manager MCLK - Main Clock OSCCTRL - Oscillators Controller OSC32KCTRL - 32kHz Oscillators Controller SUPC - Supply Controller PAC - Protection Access Controller	0
WDT – Watchdog Timer	1
RTC – Real Time Clock	2
EIC – External Interrupt Controller	3
FREQM – Frequency Meter	4
Reserved	5
NVMCTRL – Non-Volatile Memory Controller	6
DMAC - Direct Memory Access Controller	7
EVSYS – Event System	8
SERCOM0 – Serial Communication Controller 0	9
SERCOM1 – Serial Communication Controller 1	10
SERCOM2 – Serial Communication Controller 2	11
SERCOM3 – Serial Communication Controller 3	12

Peripheral Source	NVIC Line
Reserved	13
Reserved	14
Reserved	15
Reserved	16
TCC0 – Timer Counter for Control 0	17
Reserved	18
Reserved	19
TC0 – Timer Counter 0	20
TC1 – Timer Counter 1	21
TC2 – Timer Counter 2	22
	23
	24
ADC0 – Analog-to-Digital Converter 0	25
Reserved	26
AC – Analog Comparator	27
Reserved	28
Reserved	29
PTC – Peripheral Touch Controller	30
Reserved	31

9.3. Micro Trace Buffer

9.3.1. Features

- Program flow tracing for the Cortex-M0+ processor
- MTB SRAM can be used for both trace and general purpose storage by the processor
- The position and size of the trace buffer in SRAM is configurable by software
- CoreSight compliant

9.3.2. Overview

When enabled, the MTB records changes in program flow, reported by the Cortex-M0+ processor over the execution trace interface shared between the Cortex-M0+ processor and the CoreSight MTB-M0+. This information is stored as trace packets in the SRAM by the MTB. An off-chip debugger can extract the trace information using the Debug Access Port to read the trace information from the SRAM. The debugger can then reconstruct the program flow from this information.

The MTB simultaneously stores trace information into the SRAM, and gives the processor access to the SRAM. The MTB ensures that trace write accesses have priority over processor accesses.

The execution trace packet consists of a pair of 32-bit words that the MTB generates when it detects the processor PC value changes non-sequentially. A non-sequential PC change can occur during branch instructions or during exception entry. See the CoreSight MTB-M0+ Technical Reference Manual for more details on the MTB execution trace packet format.

Tracing is enabled when the MASTER.EN bit in the Master Trace Control Register is 1. There are various ways to set the bit to 1 to start tracing, or to 0 to stop tracing. See the CoreSight Cortex-M0+ Technical Reference Manual for more details on the Trace start and stop and for a detailed description of the MTB's MASTER register. The MTB can be programmed to stop tracing automatically when the memory fills to a specified watermark level or to start or stop tracing by writing directly to the MASTER.EN bit. If the watermark mechanism is not being used and the trace buffer overflows, then the buffer wraps around overwriting previous trace packets.

The base address of the MTB registers is 0x41008000; this address is also written in the CoreSight ROM Table. The offset of each register from the base address is fixed and as defined by the CoreSight MTB-M0+ Technical Reference Manual. The MTB has 4 programmable registers to control the behavior of the trace features:

- POSITION: Contains the trace write pointer and the wrap bit,
- MASTER: Contains the main trace enable bit and other trace control fields,
- FLOW: Contains the WATERMARK address and the AUTOSTOP and AUTOHALT control bits,
- BASE: Indicates where the SRAM is located in the processor memory map. This register is provided to enable auto discovery of the MTB SRAM location, by a debug agent.

See the CoreSight MTB-M0+ Technical Reference Manual for a detailed description of these registers.

9.4. High-Speed Bus System

9.4.1. Features

High-Speed Bus Matrix has the following features:

- Symmetric crossbar bus switch implementation
- Allows concurrent accesses from different masters to different slaves
- 32-bit data bus
- Operation at a 1-to-1 clock frequency with the bus masters

10. Packaging Information

10.1. Thermal Considerations

10.1.1. Thermal Resistance Data

The following table summarizes the thermal resistance data depending on the package.

Table 10-1. Thermal Resistance Data

Package Type	θ_{JA}	θ_{JC}
32-pin TQFP	68°C/W	25.8°C/W
48-pin TQFP	78.8°C/W	12.3°C/W
64-pin TQFP	66.7°C/W	11.9°C/W
32-pin QFN	37.2°C/W	3.1°C/W
48-pin QFN	31.6°C/W	10.3°C/W
64-pin QFN	32.2°C/W	10.1°C/W
56-ball WLCSP	37.5°C/W	5.48°C/W

10.1.2. Junction Temperature

The average chip-junction temperature, T_J, in °C can be obtained from the following:

1. $T_J = T_A + (P_D \times \theta_{JA})$
2. $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

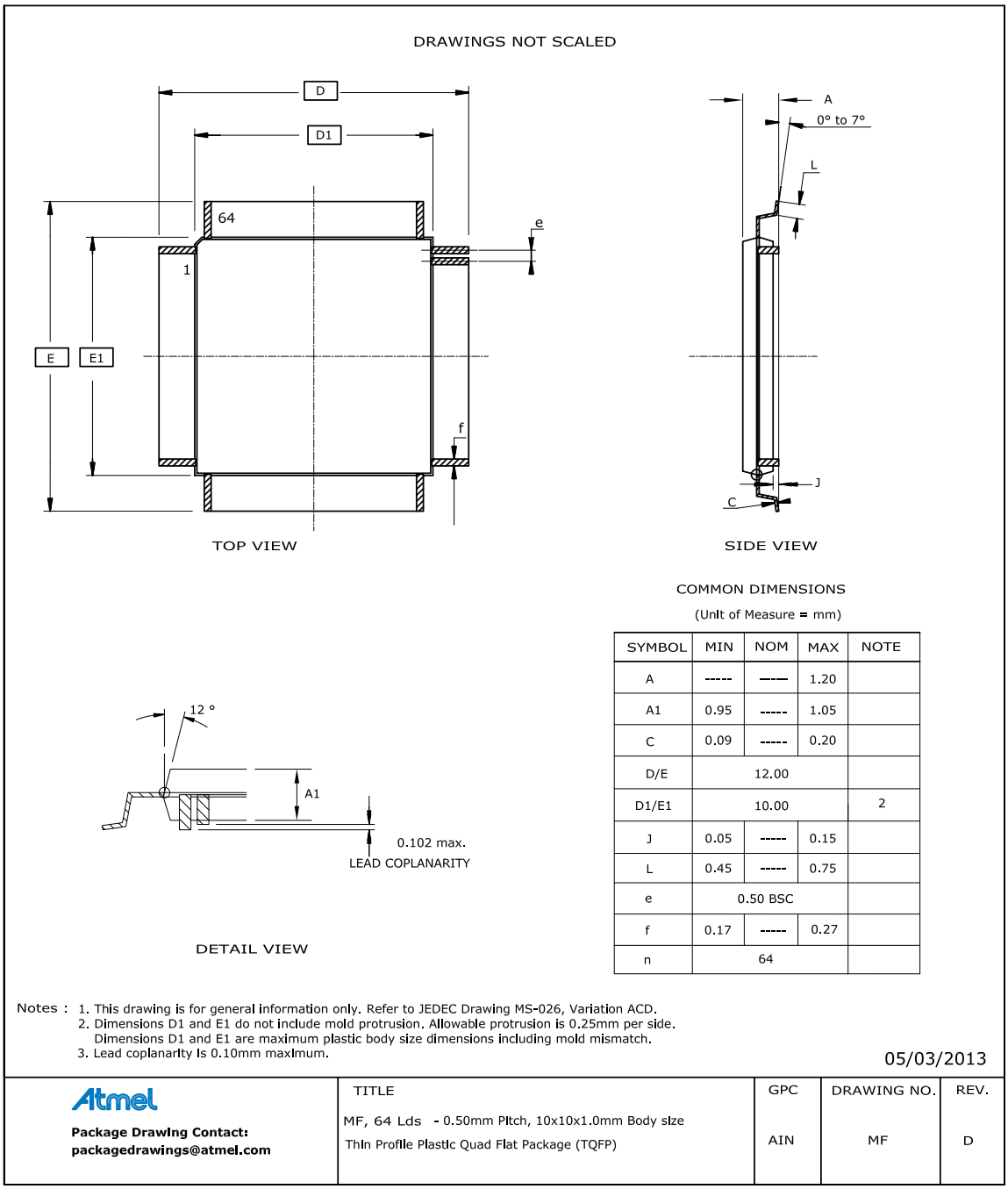
where:

- θ_{JA} = Package thermal resistance, Junction-to-ambient (°C/W), see Thermal Resistance Data
- θ_{JC} = Package thermal resistance, Junction-to-case thermal resistance (°C/W), see Thermal Resistance Data
- $\theta_{HEATSINK}$ = Thermal resistance (°C/W) specification of the external cooling device
- P_D = Device power consumption (W)
- T_A = Ambient temperature (°C)

From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature T_J in °C.

10.2. Package Drawings

10.2.1. 64 pin TQFP



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	1.20	
A1	0.95	-----	1.05	
C	0.09	-----	0.20	
D/E		12.00		
D1/E1		10.00		2
J	0.05	-----	0.15	
L	0.45	-----	0.75	
e		0.50 BSC		
f	0.17	-----	0.27	
n		64		

Notes :
1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ACD.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

05/03/2013

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE MF, 64 Lds - 0.50mm Pitch, 10x10x1.0mm Body size Thin Profile Plastic Quad Flat Package (TQFP)	GPC AIN	DRAWING NO. MF	REV. D

Table 10-2. Device and Package Maximum Weight

300	mg

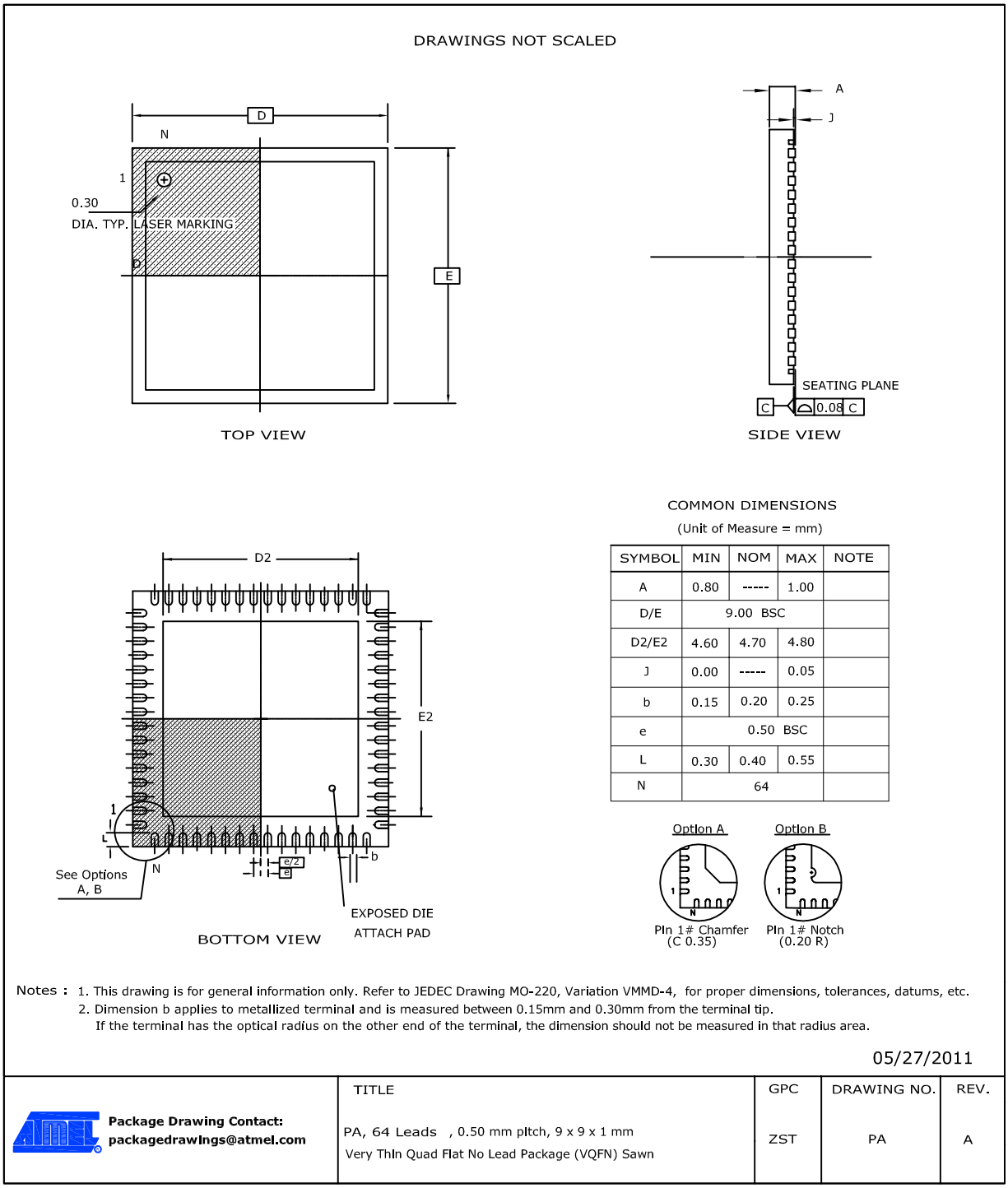
Table 10-3. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 10-4. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

10.2.2. 64 pin QFN



Note: The exposed die attach pad is not connected electrically inside the device.

Table 10-10. Package Reference

JEDEC Drawing Reference	N/A
JESD97 Classification	e1

10.2.4. 48 pin TQFP

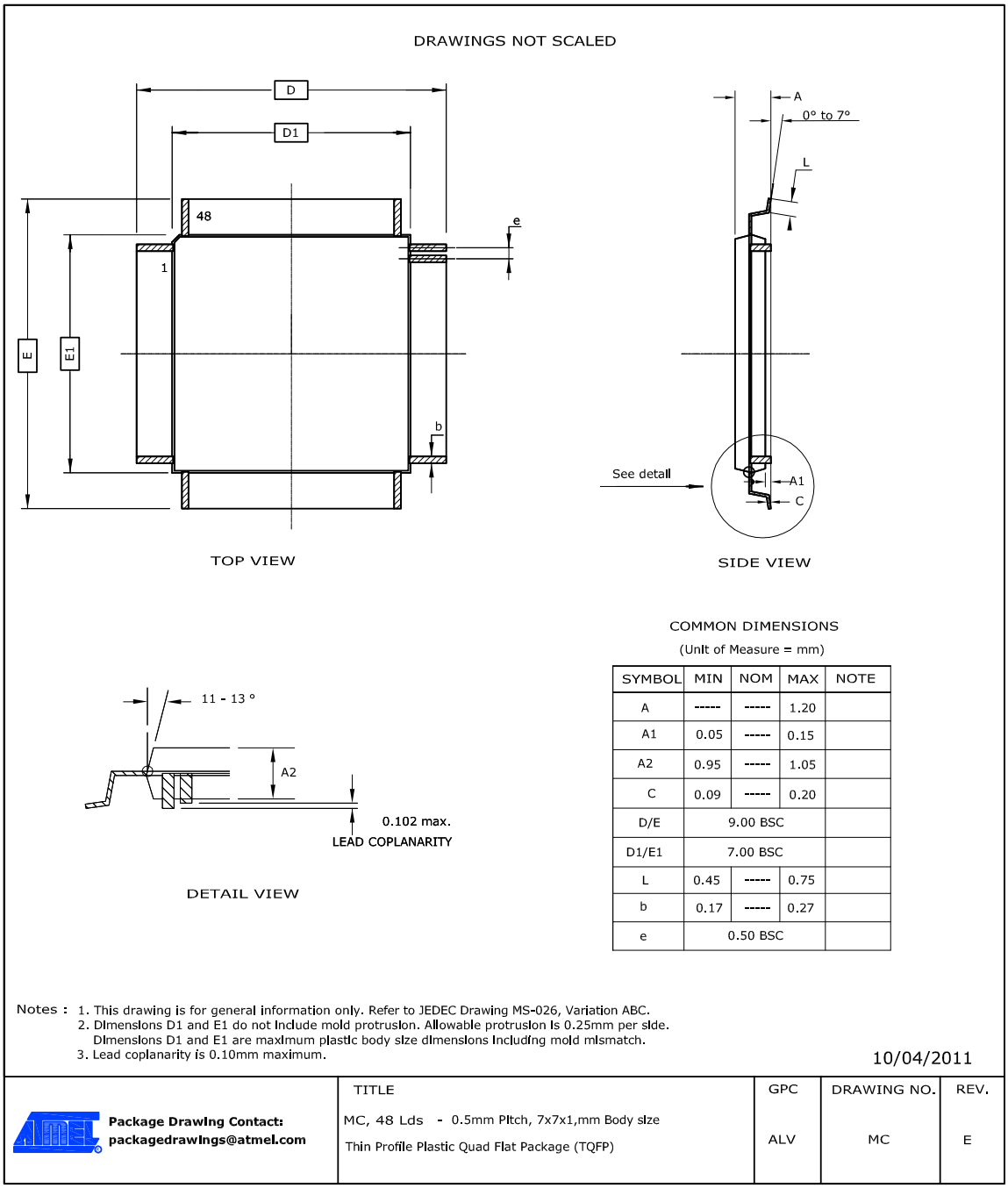


Table 10-11. Device and Package Maximum Weight

140	mg

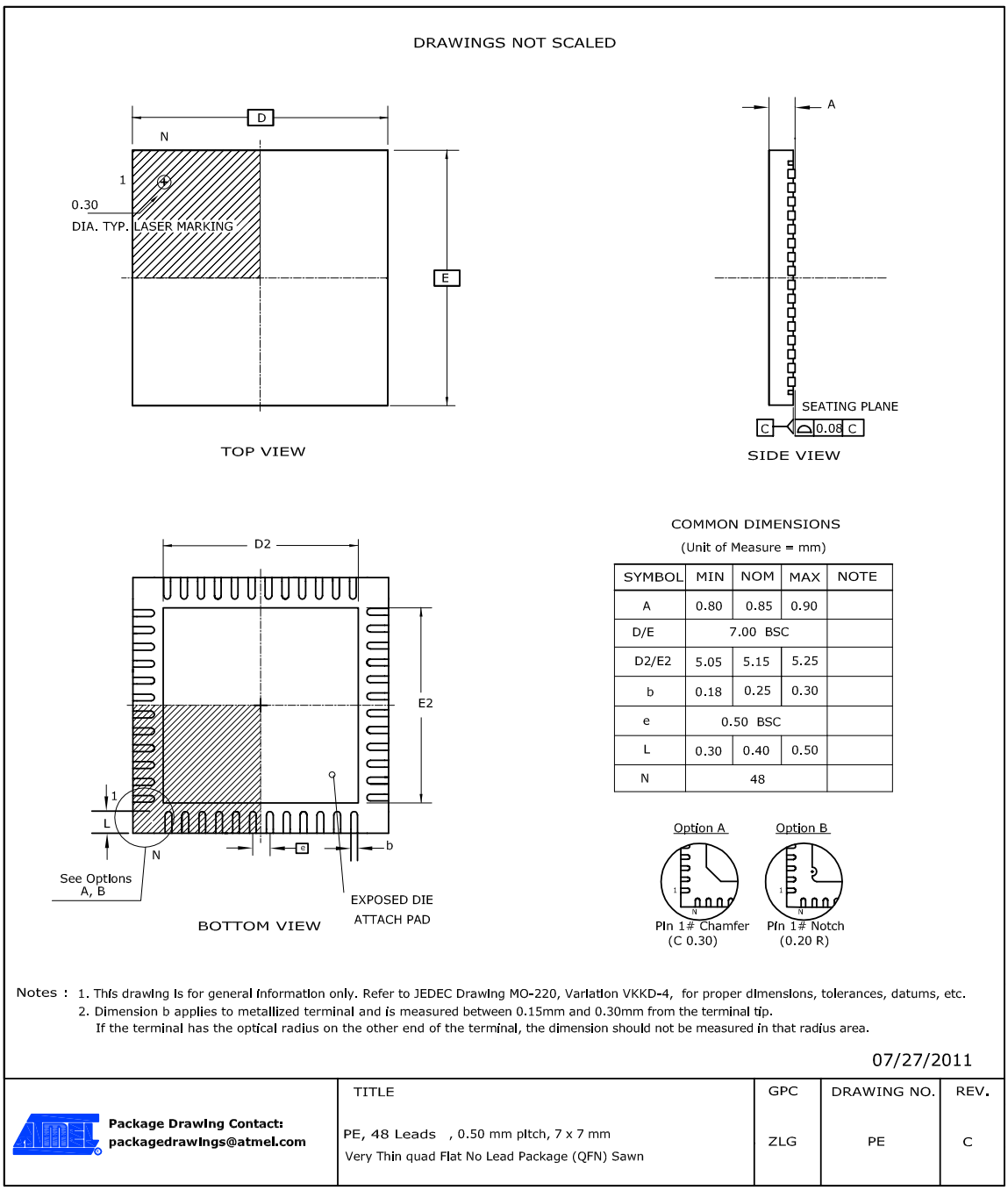
Table 10-12. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 10-13. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

10.2.5. 48 pin QFN

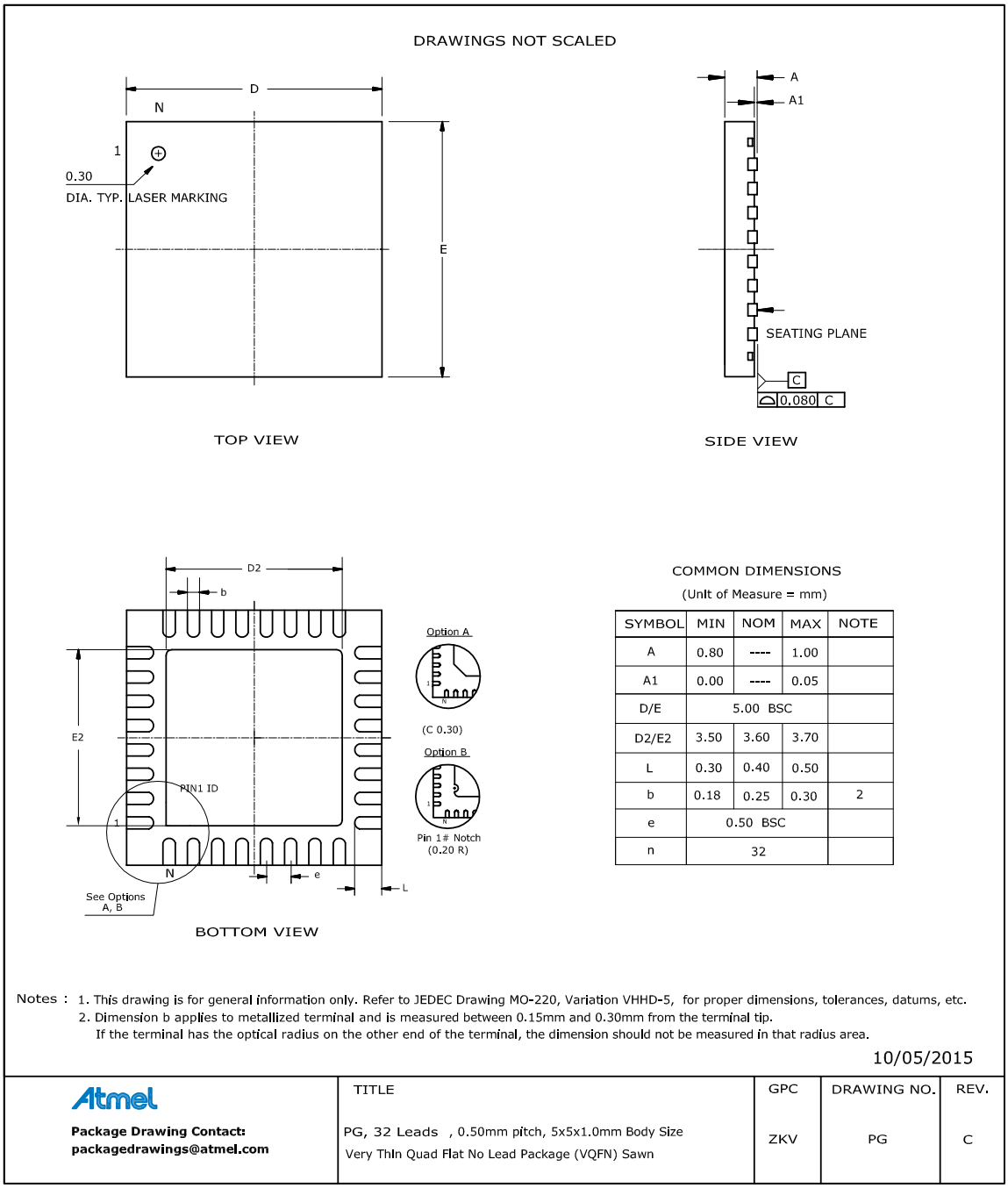


Note: The exposed die attach pad is not connected electrically inside the device.

Table 10-19. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

10.2.7. 32 pin QFN



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	----	1.00	
A1	0.00	----	0.05	
D/E		5.00 BSC		
D2/E2	3.50	3.60	3.70	
L	0.30	0.40	0.50	
b	0.18	0.25	0.30	2
e		0.50 BSC		
n		32		

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VHHD-5, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

10/05/2015

	TITLE	GPC	DRAWING NO.	REV.
Atmel **Package Drawing Contact:** **packagedrawings@atmel.com**	PG, 32 Leads , 0.50mm pitch, 5x5x1.0mm Body Size Very Thin Quad Flat No Lead Package (VQFN) Sawn	ZKV	PG	C

Note: The exposed die attach pad is connected inside the device to GND and GNDANA.

Table 10-20. Device and Package Maximum Weight

90	mg

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