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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | 8051 |
| Core Size | 8-Bit |
| Speed | 25MHz |
| Connectivity | SMBus (2-Wire/I²C), UART/USART |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 8 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 10-VFDFN Exposed Pad |
| Supplier Device Package | 11-QFN (3x3) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/c8051t601-gm |

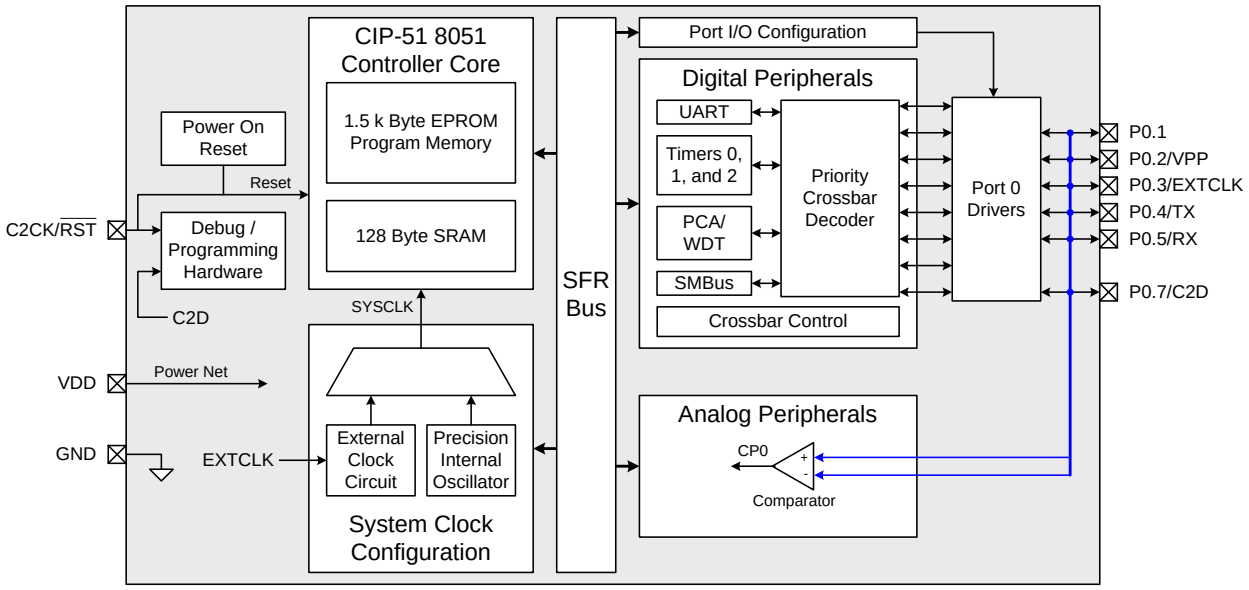


**Figure 1.3. C8051T606 Block Diagram**

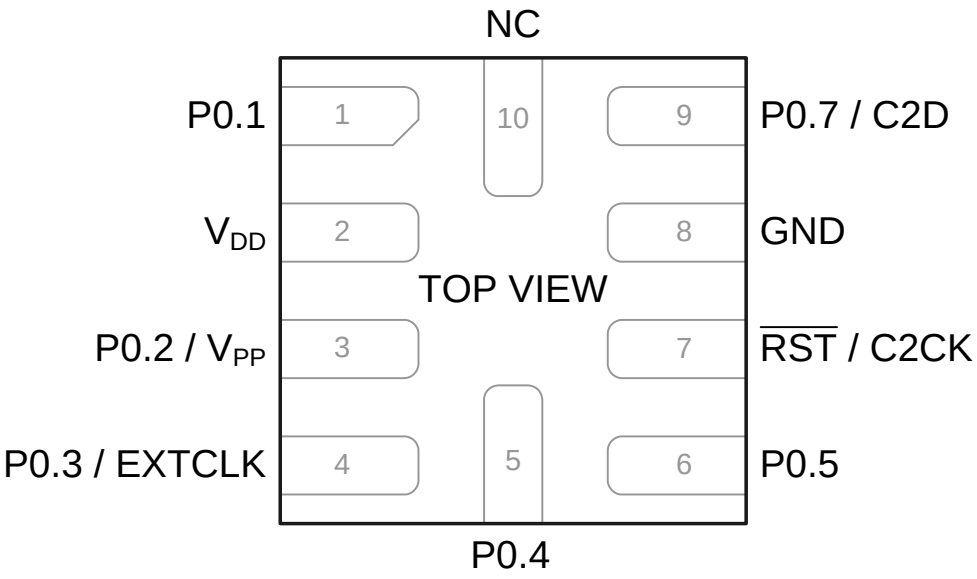


**Figure 3.5. C8051T606-ZM QFN10 Pinout Diagram (Top View)**

## 5. SOIC-14 Package Specifications

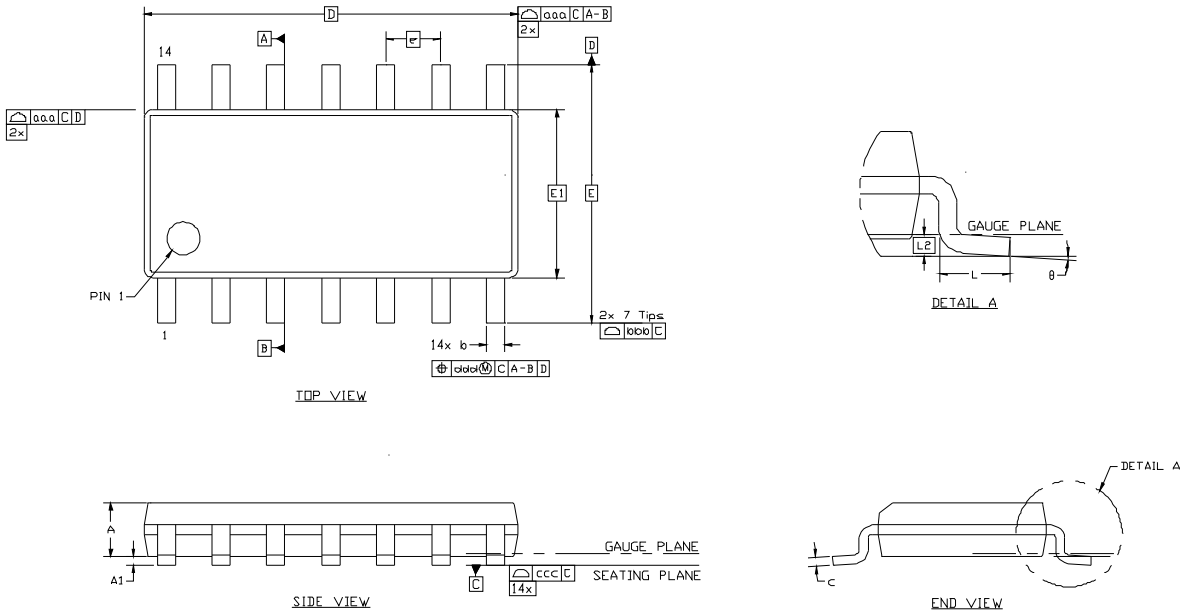


**Figure 5.1. SOIC-14 Package Drawing**

**Table 5.1. SOIC-14 Package Dimensions**

| Dimension | Min | Nom | Max |
|---|---|---|---|
| A | — | — | 1.75 |
| A1 | 0.10 | — | 0.25 |
| b | 0.33 | — | 0.51 |
| c | 0.17 | — | 0.25 |
| D | 8.65 BSC | | |
| E | 6.00 BSC | | |
| E1 | 3.90 BSC | | |
| e | 1.27 BSC | | |

| Dimension | Min | Nom | Max |
|---|---|---|---|
| L | 0.40 | — | 1.27 |
| L2 | 0.25 BSC | | |
| θ | 0° | — | 8° |
| aaa | 0.10 | | |
| bbb | 0.20 | | |
| ccc | 0.10 | | |
| ddd | 0.25 | | |

**Notes:**

1. All dimensions shown are in millimeters (mm).
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MS012, variation AB.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

## 8.2. Electrical Characteristics

### Table 8.2. Global Electrical Characteristics

–40 to +85 °C, 25 MHz system clock unless otherwise specified.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Supply Voltage (Note 1) | Regulator in Normal Mode<br>Regulator in Bypass Mode | 1.8<br>1.7 | 3.0<br>1.8 | 3.6<br>1.9 | V<br>V |
| C8051T600/1/2/3/4/5 Digital Supply Current with CPU Active | $V_{DD}$ = 1.8 V, Clock = 25 MHz<br>$V_{DD}$ = 1.8 V, Clock = 1 MHz<br>$V_{DD}$ = 3.0 V, Clock = 25 MHz<br>$V_{DD}$ = 3.0 V, Clock = 1 MHz | —<br>—<br>—<br>— | 4.3<br>2.0<br>5.0<br>2.4 | 6.0<br>—<br>6.0<br>— | mA<br>mA<br>mA<br>mA |
| C8051T600/1/2/3/4/5 Digital Supply Current with CPU Inactive (not accessing EPROM) | $V_{DD}$ = 1.8 V, Clock = 25 MHz<br>$V_{DD}$ = 1.8 V, Clock = 1 MHz<br>$V_{DD}$ = 3.0 V, Clock = 25 MHz<br>$V_{DD}$ = 3.0 V, Clock = 1 MHz | —<br>—<br>—<br>— | 1.7<br>0.5<br>1.8<br>0.6 | 2.5<br>—<br>2.6<br>— | mA<br>mA<br>mA<br>mA |
| C8051T600/1/2/3/4/5 Digital Supply Current (shutdown) | Oscillator not running (stop mode), Internal Regulator Off | — | 1 | — | µA |
| | Oscillator not running (stop or suspend mode), Internal Regulator On | — | 450 | — | µA |
| C8051T606 Digital Supply Current with CPU Active | $V_{DD}$ = 1.8 V, Clock = 25 MHz<br>$V_{DD}$ = 1.8 V, Clock = 1 MHz<br>$V_{DD}$ = 3.0 V, Clock = 25 MHz<br>$V_{DD}$ = 3.0 V, Clock = 1 MHz | —<br>—<br>—<br>— | 4.6<br>1.9<br>5.0<br>1.9 | 6.0<br>—<br>6.0<br>— | mA<br>mA<br>mA<br>mA |
| C8051T606 Digital Supply Current with CPU Inactive (not accessing EPROM) | $V_{DD}$ = 1.8 V, Clock = 25 MHz<br>$V_{DD}$ = 1.8 V, Clock = 1 MHz<br>$V_{DD}$ = 3.0 V, Clock = 25 MHz<br>$V_{DD}$ = 3.0 V, Clock = 1 MHz | —<br>—<br>—<br>— | 1.7<br>0.35<br>1.8<br>0.36 | 2.5<br>—<br>2.6<br>— | mA<br>mA<br>mA<br>mA |
| C8051T606 Digital Supply Current (shutdown) | Oscillator not running (stop mode), Internal Regulator Off | — | 1 | — | µA |
| | Oscillator not running (stop or suspend mode), Internal Regulator On | — | 300 | — | µA |
| Digital Supply RAM Data Retention Voltage | | — | 1.5 | — | V |
| Specified Operating Temperature Range | | –40 | — | +85 | °C |
| SYSCLK (system clock frequency) | (Note 2) | 0 | — | 25 | MHz |

**Notes:**

1. Analog performance is not guaranteed when $V_{DD}$ is below 1.8 V.
2. SYSCLK must be at least 32 kHz to enable debugging.
3. Supply current parameters specified with Memory Power Controller enabled.

## Table 8.10. ADC0 Electrical Characteristics

$V_{DD}$ = 3.0 V, VREF = 2.40 V (REFSL=0), –40 to +85 °C unless otherwise specified.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **DC Accuracy** | | | | | |
| Resolution | | | 10 | | bits |
| Integral Nonlinearity | | — | ±0.5 | ±1 | LSB |
| Differential Nonlinearity | Guaranteed Monotonic | — | ±0.5 | ±1 | LSB |
| Offset Error | | –2 | 0 | 2 | LSB |
| Full Scale Error | | –2 | 0 | 2 | LSB |
| Offset Temperature Coefficient | | — | 45 | — | ppm/°C |
| **Dynamic performance (10 kHz sine-wave single-ended input, 1 dB below Full Scale, 500 ksps)** | | | | | |
| Signal-to-Noise Plus Distortion | | 56 | 60 | — | dB |
| Total Harmonic Distortion | Up to the 5th harmonic | — | 72 | — | dB |
| Spurious-Free Dynamic Range | | — | –75 | — | dB |
| **Conversion Rate** | | | | | |
| SAR Conversion Clock | | — | — | 8.33 | MHz |
| Conversion Time in SAR Clocks | 10-bit Mode<br>8-bit Mode | 13<br>11 | —<br>— | —<br>— | clocks<br>clocks |
| Track/Hold Acquisition Time | $V_{DD} \geq 2.0$ V<br>$V_{DD} < 2.0$ V | 300<br>2.0 | —<br>— | —<br>— | ns<br>µs |
| Throughput Rate | | — | — | 500 | ksps |
| **Analog Inputs** | | | | | |
| ADC Input Voltage Range | | 0 | — | VREF | V |
| Sampling Capacitance | 1x Gain<br>0.5x Gain | —<br>— | 5<br>3 | —<br>— | pF<br>pF |
| Input Multiplexer Impedance | | — | 5 | — | kΩ |
| **Power Specifications** | | | | | |
| Power Supply Current ($V_{DD}$ supplied to ADC0) | Operating Mode, 500 ksps | — | 600 | 900 | µA |
| Power Supply Rejection | | — | –70 | — | dB |

## SFR Definition 13.2. CPT0MD: Comparator0 Mode Selection

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | | | | | | | CP0MD[1:0] | |
| Type | R | R | R | R | R | R | R/W | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

SFR Address = 0x9D

| Bit | Name | Function |
|---|---|---|
| 7:2 | Unused | Unused. Read = 000000b, Write = Don't Care. |
| 1:0 | CP0MD[1:0] | **Comparator0 Mode Select.**<br>These bits affect the response time and power consumption for Comparator0.<br>00: Mode 0 (Fastest Response Time, Highest Power Consumption)<br>01: Mode 1<br>10: Mode 2<br>11: Mode 3 (Slowest Response Time, Lowest Power Consumption) |

**Table 14.1. CIP-51 Instruction Set Summary**

| Mnemonic | Description | Bytes | Clock Cycles |
|---|---|---|---|
| **Arithmetic Operations** | | | |
| ADD A, Rn | Add register to A | 1 | 1 |
| ADD A, direct | Add direct byte to A | 2 | 2 |
| ADD A, @Ri | Add indirect RAM to A | 1 | 2 |
| ADD A, #data | Add immediate to A | 2 | 2 |
| ADDC A, Rn | Add register to A with carry | 1 | 1 |
| ADDC A, direct | Add direct byte to A with carry | 2 | 2 |
| ADDC A, @Ri | Add indirect RAM to A with carry | 1 | 2 |
| ADDC A, #data | Add immediate to A with carry | 2 | 2 |
| SUBB A, Rn | Subtract register from A with borrow | 1 | 1 |
| SUBB A, direct | Subtract direct byte from A with borrow | 2 | 2 |
| SUBB A, @Ri | Subtract indirect RAM from A with borrow | 1 | 2 |
| SUBB A, #data | Subtract immediate from A with borrow | 2 | 2 |
| INC A | Increment A | 1 | 1 |
| INC Rn | Increment register | 1 | 1 |
| INC direct | Increment direct byte | 2 | 2 |
| INC @Ri | Increment indirect RAM | 1 | 2 |
| DEC A | Decrement A | 1 | 1 |
| DEC Rn | Decrement register | 1 | 1 |
| DEC direct | Decrement direct byte | 2 | 2 |
| DEC @Ri | Decrement indirect RAM | 1 | 2 |
| INC DPTR | Increment Data Pointer | 1 | 1 |
| MUL AB | Multiply A and B | 1 | 4 |
| DIV AB | Divide A by B | 1 | 8 |
| DA A | Decimal adjust A | 1 | 1 |
| **Logical Operations** | | | |
| ANL A, Rn | AND Register to A | 1 | 1 |
| ANL A, direct | AND direct byte to A | 2 | 2 |
| ANL A, @Ri | AND indirect RAM to A | 1 | 2 |
| ANL A, #data | AND immediate to A | 2 | 2 |
| ANL direct, A | AND A to direct byte | 2 | 2 |
| ANL direct, #data | AND immediate to direct byte | 3 | 3 |
| ORL A, Rn | OR Register to A | 1 | 1 |
| ORL A, direct | OR direct byte to A | 2 | 2 |
| ORL A, @Ri | OR indirect RAM to A | 1 | 2 |
| ORL A, #data | OR immediate to A | 2 | 2 |
| ORL direct, A | OR A to direct byte | 2 | 2 |
| ORL direct, #data | OR immediate to direct byte | 3 | 3 |
| XRL A, Rn | Exclusive-OR Register to A | 1 | 1 |
| XRL A, direct | Exclusive-OR direct byte to A | 2 | 2 |
| XRL A, @Ri | Exclusive-OR indirect RAM to A | 1 | 2 |
| XRL A, #data | Exclusive-OR immediate to A | 2 | 2 |
| XRL direct, A | Exclusive-OR A to direct byte | 2 | 2 |

## SFR Definition 14.6. PSW: Program Status Word

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CY | AC | F0 | RS[1:0] | | OV | F1 | PARITY |
| Type | R/W | R/W | R/W | R/W | | R/W | R/W | R |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SFR Address = 0xD0; Bit-Addressable

| Bit | Name | Function |
|---|---|---|
| 7 | CY | **Carry Flag.**<br>This bit is set when the last arithmetic operation resulted in a carry (addition) or a borrow (subtraction). It is cleared to logic 0 by all other arithmetic operations. |
| 6 | AC | **Auxiliary Carry Flag.**<br>This bit is set when the last arithmetic operation resulted in a carry into (addition) or a borrow from (subtraction) the high order nibble. It is cleared to logic 0 by all other arithmetic operations. |
| 5 | F0 | **User Flag 0.**<br>This is a bit-addressable, general purpose flag for use under software control. |
| 4:3 | RS[1:0] | **Register Bank Select.**<br>These bits select which register bank is used during register accesses.<br>00: Bank 0, Addresses 0x00-0x07<br>01: Bank 1, Addresses 0x08-0x0F<br>10: Bank 2, Addresses 0x10-0x17<br>11: Bank 3, Addresses 0x18-0x1F |
| 2 | OV | **Overflow Flag.**<br>This bit is set to 1 under the following circumstances:<br>■ An ADD, ADDC, or SUBB instruction causes a sign-change overflow.<br>■ A MUL instruction results in an overflow (result is greater than 255).<br>■ A DIV instruction causes a divide-by-zero condition.<br>The OV bit is cleared to 0 by the ADD, ADDC, SUBB, MUL, and DIV instructions in all other cases. |
| 1 | F1 | **User Flag 1.**<br>This is a bit-addressable, general purpose flag for use under software control. |
| 0 | PARITY | **Parity Flag.**<br>This bit is set to logic 1 if the sum of the eight bits in the accumulator is odd and cleared if the sum is even. |

## 19. Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- CIP-51 halts program execution
- Special Function Registers (SFRs) are initialized to their defined reset values
- External Port pins are forced to a known state
- Interrupts and timers are disabled

All SFRs are reset to the predefined values noted in the SFR detailed descriptions. The contents of internal data memory are unaffected during a reset; any previously stored data is preserved. However, since the stack pointer SFR is reset, the stack is effectively lost, even though the data on the stack is not altered.

The Port I/O latches are reset to 0xFF (all logic ones) in open-drain mode. Weak pullups are enabled during and after the reset. For $V_{DD}$ Monitor and power-on resets, the $\overline{RST}$ pin is driven low until the device exits the reset state.

On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to the internal oscillator. The Watchdog Timer is enabled with the system clock divided by 12 as its clock source. Program execution begins at location 0x0000.

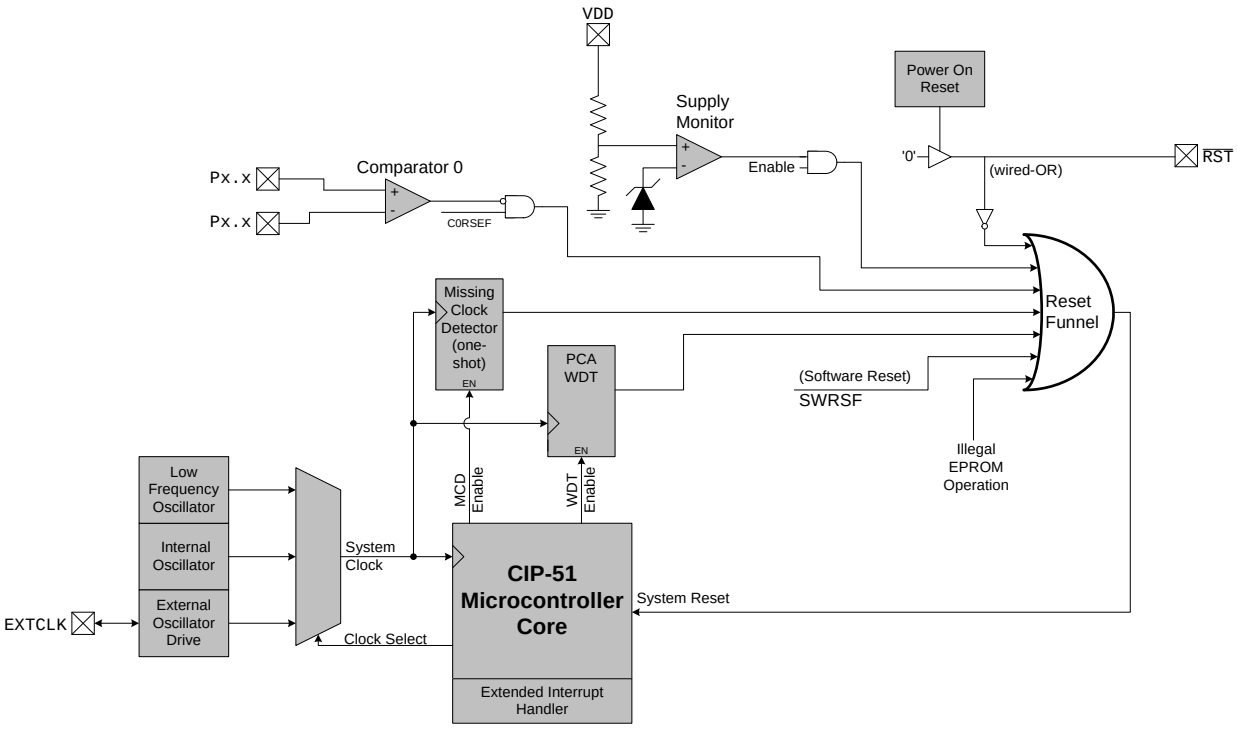


**Figure 19.1. Reset Sources**

## SFR Definition 19.1. RSTSRC: Reset Source

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | | MEMERR | C0RSEF | SWRSF | WDTRSF | MCDRSF | PORSF | PINRSF |
| Type | R | R | R/W | R/W | R | R/W | R/W | R |
| Reset | 0 | Varies | Varies | Varies | Varies | Varies | Varies | Varies |

SFR Address = 0xEF

| Bit | Name | Description | Write | Read |
|---|---|---|---|---|
| 7 | Unused | **Unused.** | Don't care. | 0 |
| 6 | MEMERR | **EPROM Error Reset Flag.** | N/A | Set to 1 if EPROM read/write error caused the last reset. |
| 5 | C0RSEF | **Comparator0 Reset Enable and Flag.** | Writing a 1 enables Comparator0 as a reset source (active-low). | Set to 1 if Comparator0 caused the last reset. |
| 4 | SWRSF | **Software Reset Force and Flag.** | Writing a 1 forces a system reset. | Set to 1 if last reset was caused by a write to SWRSF. |
| 3 | WDTRSF | **Watchdog Timer Reset Flag.** | N/A | Set to 1 if Watchdog Timer overflow caused the last reset. |
| 2 | MCDRSF | **Missing Clock Detector Enable and Flag.** | Writing a 1 enables the Missing Clock Detector. The MCD triggers a reset if a missing clock condition is detected. | Set to 1 if Missing Clock Detector timeout caused the last reset. |
| 1 | PORSF | **Power-On/$V_{DD}$ Monitor Reset Flag, and $V_{DD}$ monitor Reset Enable.** | Writing a 1 enables the $V_{DD}$ monitor and configures it as a reset source. **Writing 1 to this bit while the $V_{DD}$ monitor is disabled may cause a system reset.** | Set to 1 any time a power-on or $V_{DD}$ monitor reset occurs. **When set to 1, all other RSTSRC flags are indeterminate.** |
| 0 | PINRSF | **HW Pin Reset Flag.** | N/A | Set to 1 if $\overline{\text{RST}}$ pin caused the last reset. |

**Note:** Do not use read-modify-write operations on this register

## 20.3. Program Memory CRC

A CRC engine is included on-chip, which provides a means of verifying EPROM contents once the device has been programmed. The CRC engine is available for EPROM verification even if the device is fully read and write locked, allowing for verification of code contents at any time.

The CRC engine is operated through the C2 debug and programming interface, and performs 16-bit CRCs on individual 256-byte blocks of program memory, or a 32-bit CRC the entire memory space. To prevent hacking and extrapolation of security-locked source code, the CRC engine will only allow CRCs to be performed on contiguous 256-byte blocks beginning on 256-byte boundaries (lowest 8-bits of address are 0x00). For example, the CRC engine can perform a CRC for locations 0x0400 through 0x04FF, but it cannot perform a CRC for locations 0x0401 through 0x0500, or on block sizes smaller or larger than 256 bytes.

### 20.3.1. Performing 32-bit CRCs on Full EPROM Content

A 32-bit CRC on the entire EPROM space is initiated by writing to the CRC1 byte over the C2 interface. The CRC calculation begins at address 0x0000 and ends at the end of user EPROM space. The EPBusy bit in register C2ADD will be set during the CRC operation, and cleared once the operation is complete. The 32-bit results will be available in the CRC3-0 registers. CRC3 is the MSB, and CRC0 is the LSB. The polynomial used for the 32-bit CRC calculation is 0x04C11DB7.

**Note**: If a 16-bit CRC has been performed since the last device reset, a device reset should be initiated before performing a 32-bit CRC operation.

### 20.3.2. Performing 16-bit CRCs on 256-Byte EPROM Blocks

A 16-bit CRC of individual 256-byte blocks of EPROM can be initiated by writing to the CRC0 byte over the C2 interface. The value written to CRC0 is the high byte of the beginning address for the CRC. For example, if CRC0 is written to 0x02, the CRC will be performed on the 256 bytes beginning at address 0x0200, and ending at address 0x2FF. The EPBusy bit in register C2ADD will be set during the CRC operation, and cleared once the operation is complete. The 16-bit results will be available in the CRC1-0 registers. CRC1 is the MSB, and CRC0 is the LSB. The polynomial for the 16-bit CRC calculation is 0x1021

# 21. Oscillators and Clock Selection

C8051T600/1/2/3/4/5/6 devices include a programmable internal high-frequency oscillator and an external oscillator drive circuit. The internal high-frequency oscillator can be enabled/disabled and calibrated using the OSCICN and OSCICL registers, as shown in Figure 21.1. The system clock can be sourced by the external oscillator circuit or the internal oscillator (default). The internal oscillator offers a selectable post-scaling feature, which is initially set to divide the clock by 8.

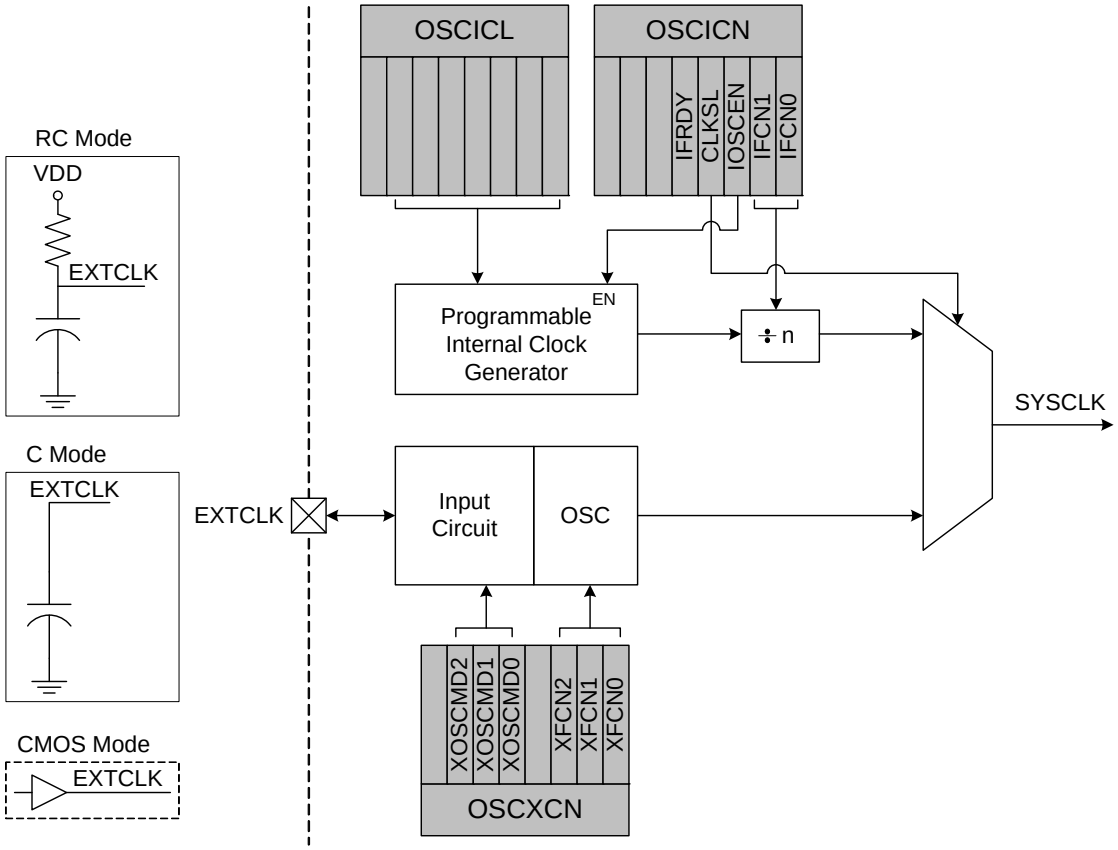


**Figure 21.1. Oscillator Options**

## 21.1. System Clock Selection

The CLKSL bit in register OSCICN selects which oscillator source is used as the system clock. CLKSL must be set to 1 for the system clock to run from the external oscillator; however the external oscillator may still clock certain peripherals (timers, PCA) when the internal oscillator is selected as the system clock. The system clock may be switched on-the-fly between the internal oscillator and external oscillator, as long as the selected clock source is enabled and running.

The internal high-frequency oscillator requires little start-up time and may be selected as the system clock immediately following the register write, which enables the oscillator. The external RC and C modes also typically require no startup time.

## SFR Definition 21.3. OSCXCN: External Oscillator Control

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | | XOSCMD[2:0] | | | | XFCN[2:0] | | |
| Type | R | R/W | | | R | R/W | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SFR Address = 0xB1

| Bit | Name | Function |
|---|---|---|
| 7 | Unused | Read = 0b; Write = Don't Care |
| 6:4 | XOSCMD[2:0] | **External Oscillator Mode Select.**<br>00x: External Oscillator circuit off.<br>010: External CMOS Clock Mode.<br>011: External CMOS Clock Mode with divide by 2 stage.<br>100: RC Oscillator Mode with divide by 2 stage.<br>101: Capacitor Oscillator Mode with divide by 2 stage.<br>11x: Reserved. |
| 3 | Unused | Read = 0b; Write = Don't Care |
| 2:0 | XFCN[2:0] | **External Oscillator Frequency Control Bits.**<br>Set according to the desired frequency range for RC mode.<br>Set according to the desired K Factor for C mode. |

| XFCN | RC Mode | C Mode |
|---|---|---|
| 000 | f ≤ 25 kHz | K Factor = 0.87 |
| 001 | 25 kHz < f ≤ 50 kHz | K Factor = 2.6 |
| 010 | 50 kHz < f ≤ 100 kHz | K Factor = 7.7 |
| 011 | 100 kHz < f ≤ 200 kHz | K Factor = 22 |
| 100 | 200 kHz < f ≤ 400 kHz | K Factor = 65 |
| 101 | 400 kHz < f ≤ 800 kHz | K Factor = 180 |
| 110 | 800 kHz < f ≤ 1.6 MHz | K Factor = 664 |
| 111 | 1.6 MHz < f ≤ 3.2 MHz | K Factor = 1590 |

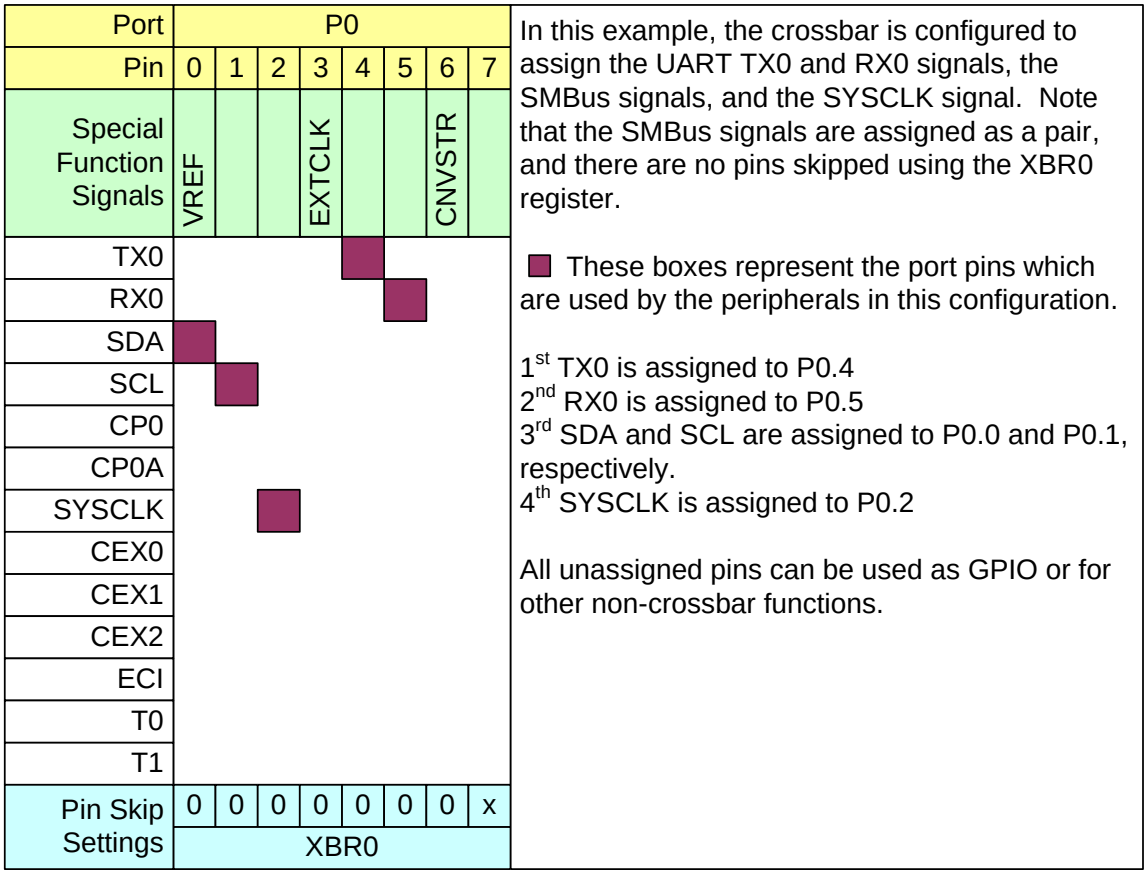


**Figure 22.4. Priority Crossbar Decoder Example 1 - No Skipped Pins**

## SFR Definition 22.5. P0MDIN: Port 0 Input Mode

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | P0MDIN[7:0] | | | | | | | |
| Type | R/W | | | | | | | |
| Reset | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

SFR Address = 0xF1

| Bit | Name | Function |
|---|---|---|
| 7:0 | P0MDIN[7:0] | **Analog Configuration Bits for P0.7–P0.0 (respectively).**<br>Port pins configured for analog mode have their weak pullup, digital driver, and digital receiver disabled.<br>0: Corresponding P0.n pin is configured for analog mode.<br>1: Corresponding P0.n pin is not configured for analog mode.<br><br>**Note:** Bits 6 and 0 on the C8051T606 are read-only. |

## SFR Definition 22.6. P0MDOUT: Port 0 Output Mode

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | P0MDOUT[7:0] | | | | | | | |
| Type | R/W | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SFR Address = 0xA4

| Bit | Name | Function |
|---|---|---|
| 7:0 | P0MDOUT[7:0] | **Output Configuration Bits for P0.7–P0.0 (respectively).**<br>These bits are ignored if the corresponding bit in register P0MDIN is logic 0.<br>0: Corresponding P0.n Output is open-drain.<br>1: Corresponding P0.n Output is push-pull.<br><br>**Note:** Bits 6 and 0 on the C8051T606 are read-only. |

All transactions are initiated by a master, with one or more addressed slave devices as the target. The master generates the START condition and then transmits the slave address and direction bit. If the transaction is a WRITE operation from the master to the slave, the master transmits the data a byte at a time and waits for an ACK from the slave at the end of each byte. For READ operations, the slave transmits the data and waits for an ACK from the master at the end of each byte. At the end of the data transfer, the master generates a STOP condition to terminate the transaction and free the bus. Figure 23.3 illustrates a typical SMBus transaction.

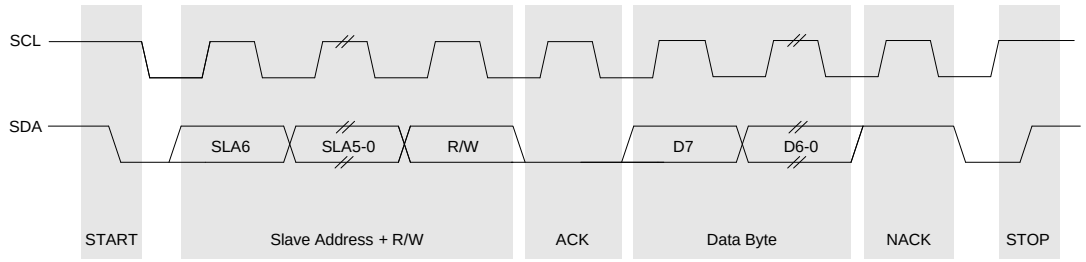


**Figure 23.3. SMBus Transaction**

### 23.3.1. Transmitter Vs. Receiver

On the SMBus communications interface, a device is the “transmitter” when it is sending an address or data byte to another device on the bus. A device is a “receiver” when an address or data byte is being sent to it from another device on the bus. The transmitter controls the SDA line during the address or data byte. After each byte of address or data information is sent by the transmitter, the receiver sends an ACK or NACK bit during the ACK phase of the transfer, during which time the receiver controls the SDA line.

### 23.3.2. Arbitration

A master may start a transfer only if the bus is free. The bus is free after a STOP condition or after the SCL and SDA lines remain high for a specified time (see Section “23.3.5. SCL High (SMBus Free) Timeout” on page 123). In the event that two or more devices attempt to begin a transfer at the same time, an arbitration scheme is employed to force one master to give up the bus. The master devices continue transmitting until one attempts a HIGH while the other transmits a LOW. Since the bus is open-drain, the bus will be pulled LOW. The master attempting the HIGH will detect a LOW SDA and lose the arbitration. The winning master continues its transmission without interruption; the losing master becomes a slave and receives the rest of the transfer if addressed. This arbitration scheme is non-destructive: one device always wins, and no data is lost.

### 23.3.3. Clock Low Extension

SMBus provides a clock synchronization mechanism, similar to $I^2C$, which allows devices with different speed capabilities to coexist on the bus. A clock-low extension is used during a transfer in order to allow slower slave devices to communicate with faster masters. The slave may temporarily hold the SCL line LOW to extend the clock low period, effectively decreasing the serial clock frequency.

### 23.3.4. SCL Low Timeout

If the SCL line is held low by a slave device on the bus, no further communication is possible. Furthermore, the master cannot force the SCL line high to correct the error condition. To solve this problem, the SMBus protocol specifies that devices participating in a transfer must detect any clock cycle held low longer than 25 ms as a “timeout” condition. Devices that have detected the timeout condition must reset the communication no later than 10 ms after detecting the timeout condition.

## SFR Definition 24.2. SBUF0: Serial (UART0) Port Data Buffer

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SBUF0[7:0] | | | | | | | |
| Type | R/W | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SFR Address = 0x99

| Bit | Name | Function |
|---|---|---|
| 7:0 | SBUF0[7:0] | **Serial Data Buffer Bits 7–0 (MSB–LSB).**<br>This SFR accesses two registers; a transmit shift register and a receive latch register. When data is written to SBUF0, it goes to the transmit shift register and is held for serial transmission. Writing a byte to SBUF0 initiates the transmission. A read of SBUF0 returns the contents of the receive latch. |

## SFR Definition 25.2. TCON: Timer Control

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SFR Address = 0x88; Bit-Addressable

| Bit | Name | Function |
|---|---|---|
| 7 | TF1 | **Timer 1 Overflow Flag.**<br>Set to 1 by hardware when Timer 1 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 1 interrupt service routine. |
| 6 | TR1 | **Timer 1 Run Control.**<br>Timer 1 is enabled by setting this bit to 1. |
| 5 | TF0 | **Timer 0 Overflow Flag.**<br>Set to 1 by hardware when Timer 0 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 0 interrupt service routine. |
| 4 | TR0 | **Timer 0 Run Control.**<br>Timer 0 is enabled by setting this bit to 1. |
| 3 | IE1 | **External Interrupt 1.**<br>This flag is set by hardware when an edge/level of type defined by IT1 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 1 service routine in edge-triggered mode. |
| 2 | IT1 | **Interrupt 1 Type Select.**<br>This bit selects whether the configured /INT1 interrupt will be edge or level sensitive. /INT1 is configured active low or high by the IN1PL bit in the IT01CF register (see SFR Definition 17.5).<br>0: /INT1 is level triggered.<br>1: /INT1 is edge triggered. |
| 1 | IE0 | **External Interrupt 0.**<br>This flag is set by hardware when an edge/level of type defined by IT1 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 0 service routine in edge-triggered mode. |
| 0 | IT0 | **Interrupt 0 Type Select.**<br>This bit selects whether the configured $\overline{\text{INT0}}$ interrupt will be edge or level sensitive. $\overline{\text{INT0}}$ is configured active low or high by the IN0PL bit in register IT01CF (see SFR Definition 17.5).<br>0: $\overline{\text{INT0}}$ is level triggered.<br>1: $\overline{\text{INT0}}$ is edge triggered. |

### 26.3.6. 16-Bit Pulse Width Modulator Mode

A PCA module may also be operated in 16-Bit PWM mode. In this mode, the 16-bit Capture/Compare module defines the number of PCA clocks for the low time of the PWM signal. When the PCA counter matches the module contents, the output on CEXn is asserted high; when the 16-bit counter overflows, CEXn is asserted low. To output a varying duty cycle, new value writes should be synchronized with PCA CCFn match interrupts. 16-Bit PWM Mode is enabled by setting the ECOMn, PWMn, and PWM16n bits in the PCA0CPMn register. For a varying duty cycle, match interrupts should be enabled (ECCFn = 1 AND MATn = 1) to help synchronize the Capture/Compare register writes. If the MATn bit is set to 1, the CCFn flag for the module will be set each time a 16-bit comparator match (rising edge) occurs. The CF flag in PCA0CN can be used to detect the overflow (falling edge). The duty cycle for 16-Bit PWM Mode is given by Equation 26.3.

**Important Note about Capture/Compare Registers**: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

$$\text{Duty Cycle} = \frac{(65536 - PCA0CPn)}{65536}$$

**Equation 26.3. 16-Bit PWM Duty Cycle**

Using Equation 26.3, the largest duty cycle is 100% (PCA0CPn = 0), and the smallest duty cycle is 0.0015% (PCA0CPn = 0xFFFF). A 0% duty cycle may be generated by clearing the ECOMn bit to 0.

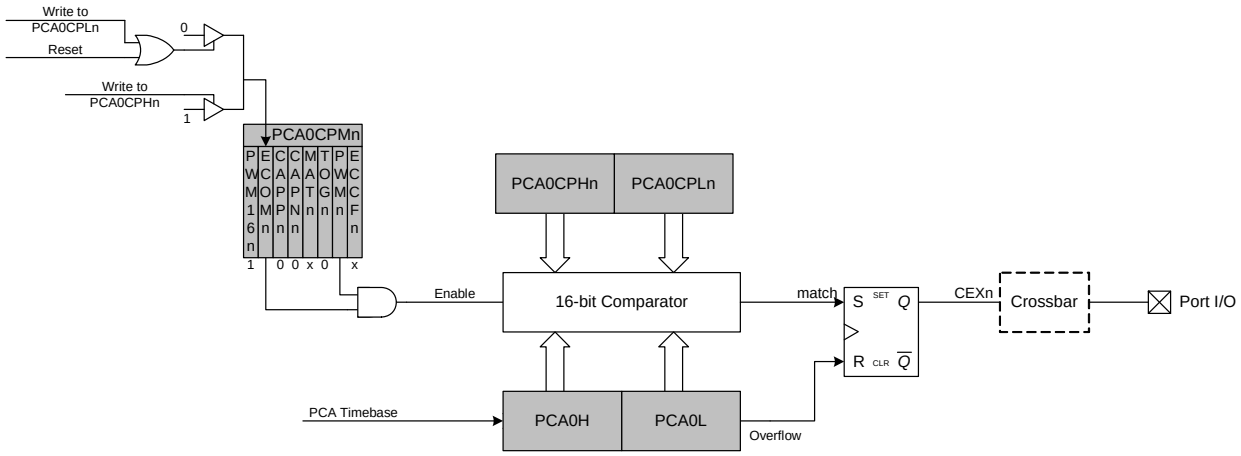


**Figure 26.9. PCA 16-Bit PWM Mode**

## 26.5. Register Descriptions for PCA0

Following are detailed descriptions of the special function registers related to the operation of the PCA.

### SFR Definition 26.1. PCA0CN: PCA Control

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | CF | CR | | | | CCF2 | CCF1 | CCF0 |
| Type | R/W | R/W | R | R | R | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SFR Address = 0xD8; Bit-Addressable

| Bit | Name | Function |
|---|---|---|
| 7 | CF | **PCA Counter/Timer Overflow Flag.**<br>Set by hardware when the PCA Counter/Timer overflows from 0xFFFF to 0x0000. When the Counter/Timer Overflow (CF) interrupt is enabled, setting this bit causes the CPU to vector to the PCA interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software. |
| 6 | CR | **PCA Counter/Timer Run Control.**<br>This bit enables/disables the PCA Counter/Timer.<br>0: PCA Counter/Timer disabled<br>1: PCA Counter/Timer enabled. |
| 5:3 | Unused | Unused. Read = 000b, Write = Don't care. |
| 2 | CCF2 | **PCA Module 2 Capture/Compare Flag.**<br>This bit is set by hardware when a match or capture occurs. When the CCF2 interrupt is enabled, setting this bit causes the CPU to vector to the PCA interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software. |
| 1 | CCF1 | **PCA Module 1 Capture/Compare Flag.**<br>This bit is set by hardware when a match or capture occurs. When the CCF1 interrupt is enabled, setting this bit causes the CPU to vector to the PCA interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software. |
| 0 | CCF0 | **PCA Module 0 Capture/Compare Flag.**<br>This bit is set by hardware when a match or capture occurs. When the CCF0 interrupt is enabled, setting this bit causes the CPU to vector to the PCA interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software. |