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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I²C), UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	8
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-SOIC (0.154", 3.90mm Width)
Supplier Device Package	14-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051t601-gsr

3. Pin Definitions

Table 3.1. Pin Definitions for the C8051T600/1/2/3/4/5

Name	QFN11 Pin	SOIC14 Pin	Type	Description
V_{DD}	3	7		Power Supply Voltage.
GND	11	3		Ground.
$\overline{RST}$ /	8	14	D I/O	Device Reset. Open-drain output of internal POR or V_{DD} monitor.
C2CK			D I/O	Clock signal for the C2 Debug Interface.
P0.7 /	10	2	D I/O or A In	Port 0.7.
C2D			D I/O	Bi-directional data signal for the C2 Debug Interface.
P0.0 /	1	5	D I/O or A In	Port 0.0.
VREF			A In	External VREF input.
P0.1	2	6	D I/O or A In	Port 0.1.
P0.2 /	4	8	D I/O or A In	Port 0.2.
V_{PP}			A In	V_{PP} Programming Supply Voltage.
P0.3 /	5	10	D I/O or A In	Port 0.3.
EXTCLK			A I/O or D In	External Clock Pin. This pin can be used as the external clock input for CMOS, capacitor, or RC oscillator configurations.
P0.4	6	12	D I/O or A In	Port 0.4.
P0.5	7	13	D I/O or A In	Port 0.5.
P0.6 /	9	1	D I/O or A In	Port 0.6.
CNVSTR			D In	ADC0 External Convert Start Input.
NC	—	4,9,11		No Connection.

Table 3.2. Pin Definitions for the C8051T606

Name	QFN11 Pin	MSOP10 Pin	QFN10 Pin	Type	Description
V_{DD}	3	3	2		Power Supply Voltage.
GND	9	9	8		Ground (Required).
GND*	11	—	—		Ground (Optional).
$\overline{RST}$ /	8	8	7	D I/O	Device Reset. Open-drain output of internal POR or V_{DD} monitor.
C2CK				D I/O	Clock signal for the C2 Debug Interface.
P0.7 /	10	10	9	D I/O or A In	Port 0.7.
C2D				D I/O	Bi-directional data signal for the C2 Debug Interface.
P0.1	2	2	1	D I/O or A In	Port 0.1.
P0.2 /	4	4	3	D I/O or A In	Port 0.2.
V_{PP}				A In	V_{PP} Programming Supply Voltage.
P0.3 /	5	5	4	D I/O or A In	Port 0.3.
EXTCLK				A I/O or D In	External Clock Pin. This pin can be used as the external clock input for CMOS, capacitor, or RC oscillator configurations.
P0.4	6	6	5	D I/O or A In	Port 0.4.
P0.5	7	7	6	D I/O or A In	Port 0.5.
NC	1	1	10		No Connection.

4. QFN-11 Package Specifications

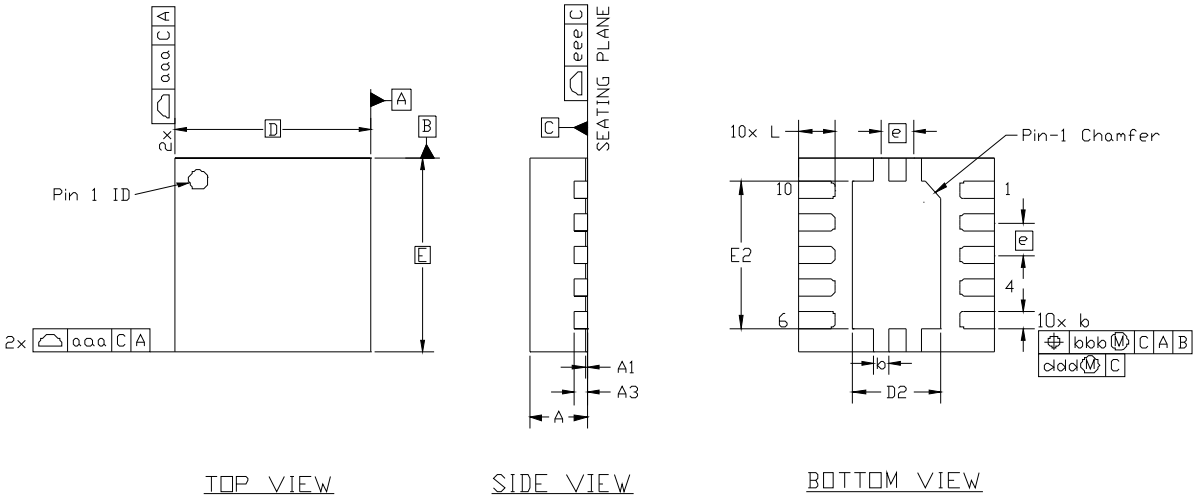

Figure 4.1. QFN-11 Package Drawing

Table 4.1. QFN-11 Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.90	1.00
A1	0.03	0.07	0.11
A3		0.25 REF	
b	0.18	0.25	0.30
D		3.00 BSC	
D2	1.30	1.35	1.40
e		0.50 BSC	

Dimension	Min	Nom	Max
E		3.00 BSC	
E2	2.20	2.25	2.30
L	0.45	0.55	0.65
aaa	—	—	0.15
bbb	—	—	0.15
ddd	—	—	0.05
eee	—	—	0.08

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-243, variation VEED except for custom features D2, E2, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

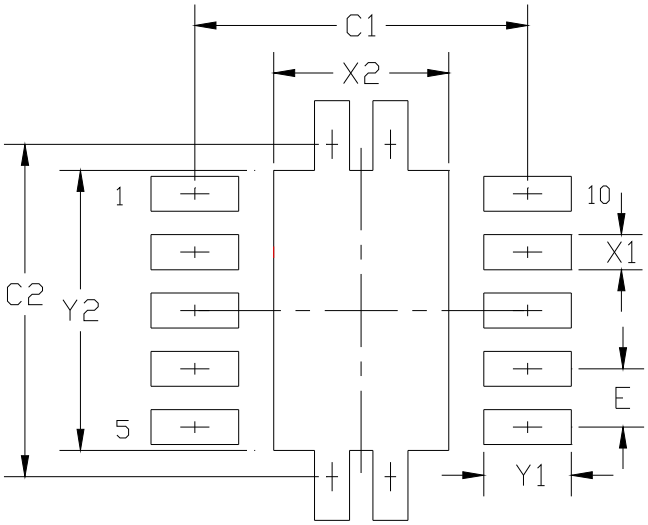

Figure 4.2. QFN-11 PCB Land Pattern

Table 4.2. QFN-11 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	2.75	2.85
C2	2.75	2.85
E	0.50 BSC	
X1	0.20	0.30

Dimension	Min	Max
X2	1.40	1.50
Y1	0.65	0.75
Y2	2.30	2.40

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.
7. A 3 x 1 array of 1.30 x 0.60 mm openings on 0.80 mm pitch should be used for the center pad.

Card Assembly

8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

5. SOIC-14 Package Specifications

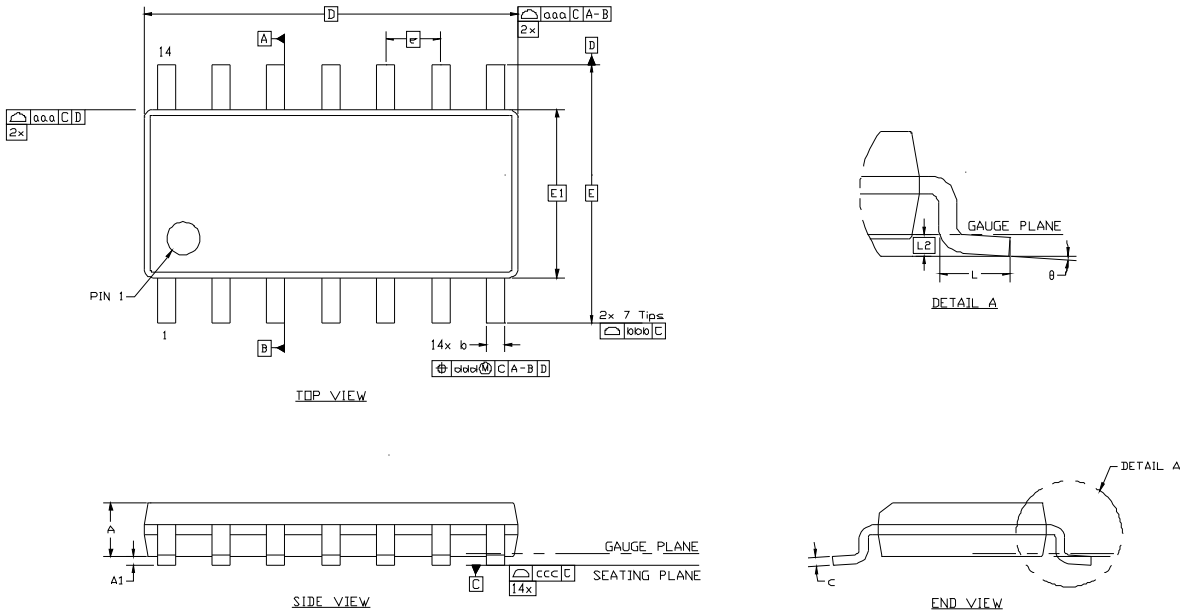

Figure 5.1. SOIC-14 Package Drawing

Table 5.1. SOIC-14 Package Dimensions

Dimension	Min	Nom	Max
A	—	—	1.75
A1	0.10	—	0.25
b	0.33	—	0.51
c	0.17	—	0.25
D	8.65 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		

Dimension	Min	Nom	Max
L	0.40	—	1.27
L2	0.25 BSC		
θ	0°	—	8°
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		

Notes:

1. All dimensions shown are in millimeters (mm).
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MS012, variation AB.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

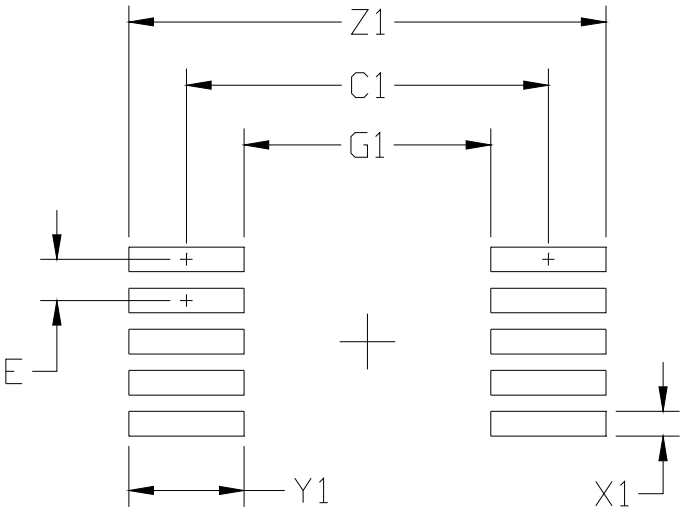

Figure 6.2. MSOP-10 PCB Land Pattern

Table 6.2. MSOP-10 PCB Land Pattern Dimensions

Dimension	Min	Max	Dimension	Min	Max
C1	4.40 REF		X1	—	0.30
E	0.50 BSC		Y1	1.40 REF	
G1	3.00	—	Z1	—	5.80

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ASME Y14.5M-1994.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.

Card Assembly

9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. Electrical Characteristics

8.1. Absolute Maximum Specifications

Table 8.1. Absolute Maximum Ratings

Parameter	Conditions	Min	Typ	Max	Units
Ambient temperature under bias		–55	—	125	°C
Storage temperature		–65	—	150	°C
Voltage on $\overline{RST}$ or any Port I/O pin (except V_{PP} during programming) with respect to GND	$V_{DD} \geq 2.2$ V $V_{DD} < 2.2$ V	–0.3 –0.3	— —	5.8 V_{DD} + 3.6	V V
Voltage on V_{PP} with respect to GND during a programming operation	$V_{DD} > 2.4$ V	–0.3	—	7.0	V
Duration of High-voltage on V_{PP} pin (cumulative)	$V_{PP} > (V_{DD} + 3.6$ V)	—	—	10	s
Voltage on V_{DD} with respect to GND	Regulator in Normal Mode Regulator in Bypass Mode	–0.3 –0.3	— —	4.2 1.98	V V
Maximum total current through V_{DD} or GND		—	—	500	mA
Maximum output current sunk or sourced by $\overline{RST}$ or any Port pin		—	—	100	mA

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8.4. Reset Electrical Characteristics

–40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
$\overline{\text{RST}}$ Output Low Voltage	I_{OL} = 8.5 mA, V_{DD} = 1.8 V to 3.6 V	—	—	0.6	V
$\overline{\text{RST}}$ Input High Voltage		0.75 x V_{DD}	—	—	V
$\overline{\text{RST}}$ Input Low Voltage		—	—	0.6	V_{DD}
$\overline{\text{RST}}$ Input Pullup Current	$\overline{\text{RST}}$ = 0.0 V	—	25	50	µA
V_{DD} POR Ramp Time		—	—	1	ms
V_{DD} Monitor Threshold (V_{RST})		1.7	1.75	1.8	V
Missing Clock Detector Timeout	Time from last system clock rising edge to reset initiation	400	625	900	µs
Reset Time Delay	Delay between release of any reset source and code execution at location 0x0000	—	—	60	µs
Minimum $\overline{\text{RST}}$ Low Time to Generate a System Reset		15	—	—	µs
V_{DD} Monitor Turn-on Time	V_{DD} = V_{RST} - 0.1 V	—	50	—	µs
V_{DD} Monitor Supply Current		—	20	30	µA

Table 8.5. Internal Voltage Regulator Electrical Characteristics

–40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Input Voltage Range		1.8	—	3.6	V
Bias Current	Normal Mode	—	30	50	µA

Table 8.6. EPROM Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Units
EPROM Size	C8051T600/1	8192*	—	—	bytes
	C8051T602/3	4096	—	—	bytes
	C8051T604/5	2048	—	—	bytes
	C8051T606	1536	—	—	bytes
Write Cycle Time (per Byte)		105	155	205	µs
Programming Voltage (V_{PP})	C8051T600/1/2/3/4/5	6.25	6.5	6.75	V
Programming Voltage (V_{PP})	C8051T606	5.75	6.0	6.25	V
Note: 512 bytes at location 0x1E00 to 0x1FFF are not available for program storage					

externally driven from –0.25 V to (V_{DD}) + 0.25 V without damage or upset. The complete Comparator electrical specifications are given in Section “8. Electrical Characteristics” on page 30.

The Comparator response time may be configured in software via the CPT0MD register (see SFR Definition 13.2). Selecting a longer response time reduces the Comparator supply current.

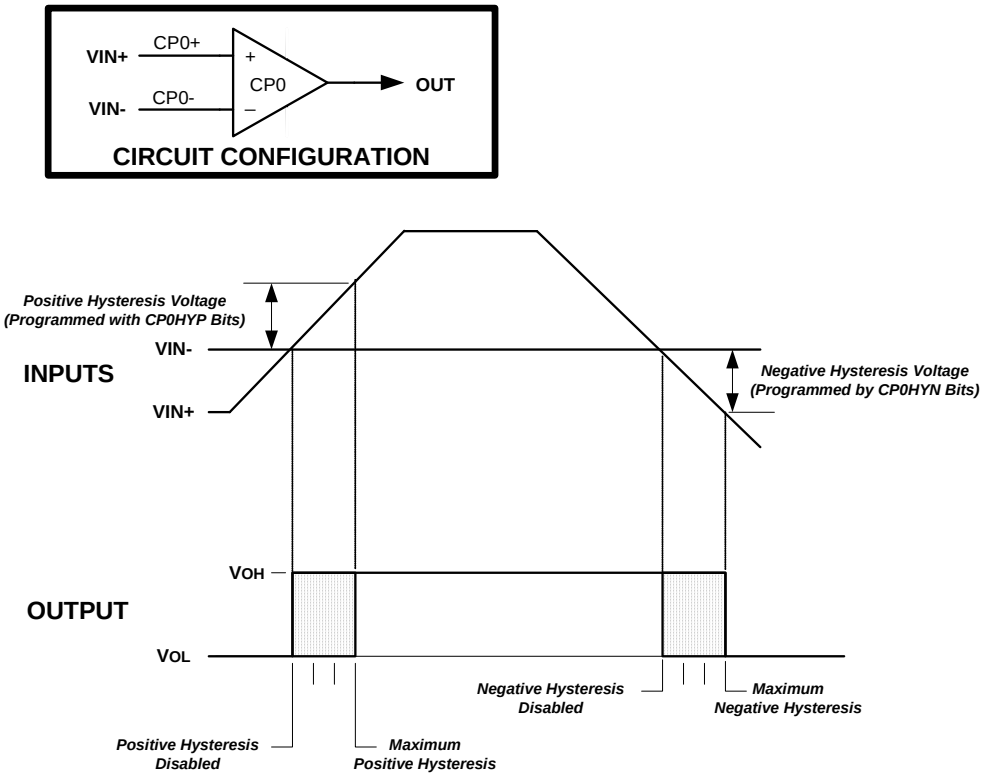

Figure 13.2. Comparator Hysteresis Plot

The Comparator hysteresis is software-programmable via its Comparator Control register CPT0CN. The user can program both the amount of hysteresis voltage (referred to as the input voltage) and the positive and negative-going symmetry of this hysteresis around the threshold voltage.

The Comparator hysteresis is programmed using Bits3–0 in the Comparator Control Register CPT0CN (shown in SFR Definition 13.1). The amount of negative hysteresis voltage is determined by the settings of the CP0HYN bits. As shown in Figure 13.2, settings of 20, 10 or 5 mV of negative hysteresis can be programmed, or negative hysteresis can be disabled. In a similar way, the amount of positive hysteresis is determined by the setting the CP0HYP bits.

Comparator interrupts can be generated on both rising-edge and falling-edge output transitions. (For Interrupt enable and priority control, see Section “17.1. MCU Interrupt Sources and Vectors” on page 81). The CP0FIF flag is set to logic 1 upon a Comparator falling-edge occurrence, and the CP0RIF flag is set to logic 1 upon the Comparator rising-edge occurrence. Once set, these bits remain set until cleared by software.

The output state of the Comparator can be obtained at any time by reading the CP0OUT bit. The Comparator is enabled by setting the CP0EN bit to logic 1, and is disabled by clearing this bit to logic 0.

Table 16.2. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	Description	Page
ADC0GTL	0xC3	ADC0 Greater-Than Compare Low	47
ADC0H	0xBE	ADC0 High	45
ADC0L	0xBD	ADC0 Low	45
ADC0LTH	0xC6	ADC0 Less-Than Compare Word High	48
ADC0LTL	0xC5	ADC0 Less-Than Compare Word Low	48
AMX0SL	0xBB	AMUX0 Multiplexer Channel Select	51
B	0xF0	B Register	72
CKCON	0x8E	Clock Control	146
CPT0CN	0xF8	Comparator0 Control	61
CPT0MD	0x9D	Comparator0 Mode Selection	62
CPT0MX	0x9F	Comparator0 MUX Selection	64
DPH	0x83	Data Pointer High	71
DPL	0x82	Data Pointer Low	71
EIE1	0xE6	Extended Interrupt Enable 1	85
EIP1	0xF6	Extended Interrupt Priority 1	86
IE	0xA8	Interrupt Enable	83
IP	0xB8	Interrupt Priority	84
IT01CF	0xE4	INT0/INT1 Configuration	88
OSCICL	0xB3	Internal Oscillator Calibration	101
OSCICN	0xB2	Internal Oscillator Control	102
OSCXCN	0xB1	External Oscillator Control	104
P0	0x80	Port 0 Latch	118
P0MDIN	0xF1	Port 0 Input Mode Configuration	119
P0MDOUT	0xA4	Port 0 Output Mode Configuration	119
PCA0CN	0xD8	PCA Control	173
PCA0CPH0	0xFC	PCA Capture 0 High	177
PCA0CPH1	0xEA	PCA Capture 1 High	177
PCA0CPH2	0xEC	PCA Capture 2 High	177
PCA0CPL0	0xFB	PCA Capture 0 Low	177
PCA0CPL1	0xE9	PCA Capture 1 Low	177
PCA0CPL2	0xEB	PCA Capture 2 Low	177
PCA0CPM0	0xDA	PCA Module 0 Mode Register	175
PCA0CPM1	0xDB	PCA Module 1 Mode Register	175
PCA0CPM2	0xDC	PCA Module 2 Mode Register	175

SFR Definition 18.1. PCON: Power Control

Bit	7	6	5	4	3	2	1	0
Name	GF[5:0]						STOP	IDLE
Type	R/W						R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x87

Bit	Name	Function
7:2	GF[5:0]	**General Purpose Flags 5–0.** These are general purpose flags for use under software control.
1	STOP	**Stop Mode Select.** Setting this bit will place the CIP-51 in Stop mode. This bit will always be read as 0. 1: CPU goes into Stop mode (internal oscillator stopped).
0	IDLE	**Idle Mode Select.** Setting this bit will place the CIP-51 in Idle mode. This bit will always be read as 0. 1: CPU goes into Idle mode. (Shuts off clock to CPU, but clock to Timers, Interrupts, Serial Ports, and Analog Peripherals are still active.)

19. Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- CIP-51 halts program execution
- Special Function Registers (SFRs) are initialized to their defined reset values
- External Port pins are forced to a known state
- Interrupts and timers are disabled

All SFRs are reset to the predefined values noted in the SFR detailed descriptions. The contents of internal data memory are unaffected during a reset; any previously stored data is preserved. However, since the stack pointer SFR is reset, the stack is effectively lost, even though the data on the stack is not altered.

The Port I/O latches are reset to 0xFF (all logic ones) in open-drain mode. Weak pullups are enabled during and after the reset. For V_{DD} Monitor and power-on resets, the $\overline{RST}$ pin is driven low until the device exits the reset state.

On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to the internal oscillator. The Watchdog Timer is enabled with the system clock divided by 12 as its clock source. Program execution begins at location 0x0000.

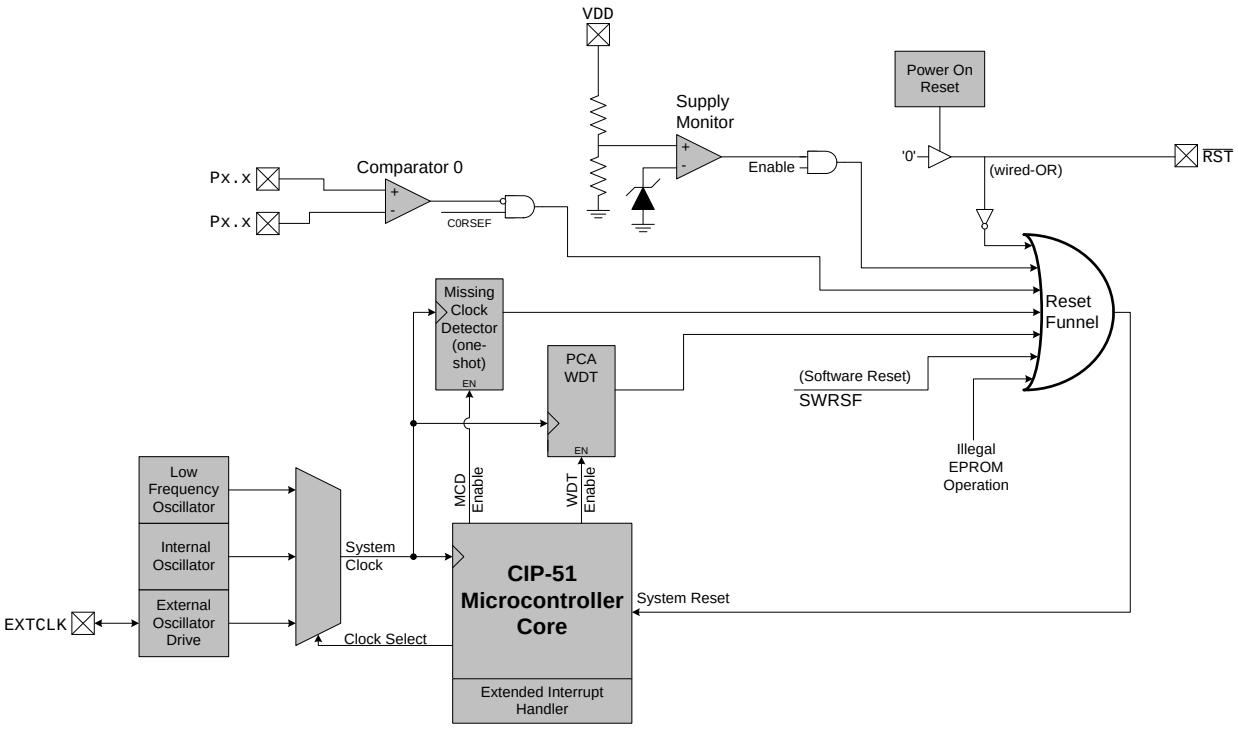

Figure 19.1. Reset Sources

20. EPROM Memory

Electrically programmable read-only memory (EPROM) is included on-chip for program code storage. The EPROM memory can be programmed via the C2 debug and programming interface when a special programming voltage is applied to the V_{PP} pin. Each location in EPROM memory is programmable only once (i.e., non-erasable). Table 8.6 on page 34 shows the EPROM specifications.

20.1. Programming and Reading the EPROM Memory

Reading and writing the EPROM memory is accomplished through the C2 programming and debug interface. When creating hardware to program the EPROM, it is necessary to follow the programming steps listed below. Refer to the “C2 Interface Specification” available at http://www.silabs.com for details on communicating via the C2 interface. Section “27. C2 Interface” on page 178 has information about C2 register addresses for the C8051T600/1/2/3/4/5/6.

20.1.1. EPROM Write Procedure

1. Reset the device using the $\overline{\text{RST}}$ pin.
2. Wait at least 20 µs before sending the first C2 command.
3. Place the device in core reset: Write 0x04 to the DEVCTL register.
4. Set the device to program mode (1st step): Write 0x40 to the EPCTL register.
5. Set the device to program mode (2nd step): Write 0x58 to the EPCTL register.
6. Apply the VPP programming Voltage.
7. Write the first EPROM address for programming to EPADDRH and EPADDRL.
8. Write a data byte to EPDAT. EPADDRH:L will increment by 1 after this write.
9. Use a C2 Address Read command to poll for write completion.
10. (Optional) Check the ERROR bit in register EPSTAT and abort the programming operation if necessary.
11. If programming is not finished, return to Step 8 to write the next address in sequence, or return to Step 7 to program a new address.
12. Remove the VPP programming Voltage.
13. Remove program mode (1st step): Write 0x40 to the EPCTL register.
14. Remove program mode (2nd step): Write 0x00 to the EPCTL register.
15. Reset the device: Write 0x02 and then 0x00 to the DEVCTL register.

Important Note: There is a finite amount of time which V_{PP} can be applied without damaging the device, which is cumulative over the life of the device. Refer to Table 8.1 on page 30 for the V_{PP} timing specification.

21. Oscillators and Clock Selection

C8051T600/1/2/3/4/5/6 devices include a programmable internal high-frequency oscillator and an external oscillator drive circuit. The internal high-frequency oscillator can be enabled/disabled and calibrated using the OSCICN and OSCICL registers, as shown in Figure 21.1. The system clock can be sourced by the external oscillator circuit or the internal oscillator (default). The internal oscillator offers a selectable post-scaling feature, which is initially set to divide the clock by 8.

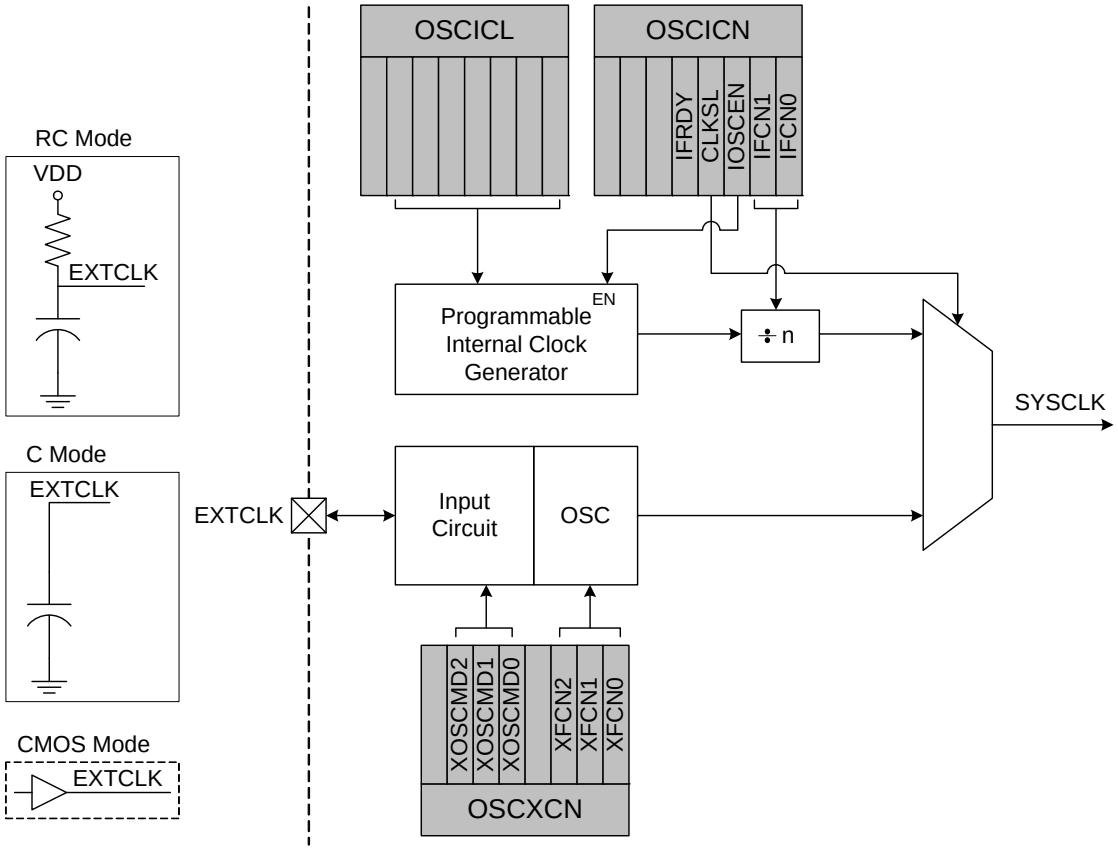

Figure 21.1. Oscillator Options

21.1. System Clock Selection

The CLKSL bit in register OSCICN selects which oscillator source is used as the system clock. CLKSL must be set to 1 for the system clock to run from the external oscillator; however the external oscillator may still clock certain peripherals (timers, PCA) when the internal oscillator is selected as the system clock. The system clock may be switched on-the-fly between the internal oscillator and external oscillator, as long as the selected clock source is enabled and running.

The internal high-frequency oscillator requires little start-up time and may be selected as the system clock immediately following the register write, which enables the oscillator. The external RC and C modes also typically require no startup time.

22.2. Assigning Port I/O Pins to Analog and Digital Functions

Port I/O pins can be assigned to various analog, digital, and external interrupt functions. The Port pins assigned to analog functions should be configured for analog I/O, and Port pins assigned to digital or external interrupt functions should be configured for digital I/O.

22.2.1. Assigning Port I/O Pins to Analog Functions

Table 22.1 shows all available analog functions that require Port I/O assignments. **Port pins selected for these analog functions should have their corresponding bit in XBR0 set to 1.** This reserves the pin for use by the analog function and does not allow it to be claimed by the crossbar. Table 22.1 shows the potential mapping of Port I/O to each analog function.

Table 22.1. Port I/O Assignment for Analog Functions

Analog Function	Potentially Assignable Port Pins	SFR(s) used for Assignment
ADC Input	P0.0–P0.7	AMX0SL, XBR0
Comparator0 Input	P0.0–P0.7	CPT0MX, XBR0
Voltage Reference Input for ADC (VREF)	P0.0	REF0CN, XBR0
External Oscillator in RC or C Mode (EXTCLK)	P0.3	OSCXCN, XBR0

22.2.2. Assigning Port I/O Pins to Digital Functions

Any Port pins not assigned to analog functions may be assigned to digital functions or used as GPIO. Most digital functions rely on the crossbar for pin assignment; however, some digital functions bypass the crossbar in a manner similar to the analog functions listed above. **Port pins used by these digital functions and any Port pins selected for use as GPIO should have their corresponding bit in XBR0 set to 1.** Table 22.2 shows all available digital functions and the potential mapping of Port I/O to each digital function.

Table 22.2. Port I/O Assignment for Digital Functions

Digital Function	Potentially Assignable Port Pins	SFR(s) used for Assignment
UART0, SMBus, CP0, CP0A, SYSCLK, PCA0 (CEX0-2 and ECI), T0 or T1.	Any Port pin available for assignment by the crossbar. This includes P0.0 - P0.7 pins which have their XBR0 bit set to 0. **Note:** The crossbar will always assign UART0 pins to P0.4 and P0.5.	XBR1, XBR2
Any pin used for GPIO	P0.0–P0.7	XBR0

SFR Definition 22.2. XBR1: Port I/O Crossbar Register 1

Bit	7	6	5	4	3	2	1	0
Name	PCA0ME[1:0]		CP0AE	CP0E	SYSCKE	SMB0E	URX0E	UTX0E
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xE2

Bit	Name	Function
7:6	PCA0ME[1:0]	**PCA Module I/O Enable Bits.** 00: All PCA I/O unavailable at Port pins. 01: CEX0 routed to Port pin. 10: CEX0, CEX1 routed to Port pins. 11: CEX0, CEX1, CEX2 routed to Port pins.
5	CP0AE	**Comparator0 Asynchronous Output Enable.** 0: Asynchronous CP0 unavailable at Port pin. 1: Asynchronous CP0 routed to Port pin.
4	CP0E	**Comparator0 Output Enable.** 0: CP0 unavailable at Port pin. 1: CP0 routed to Port pin.
3	SYSCKE	**/SYSCLK Output Enable.** 0: /SYSCLK unavailable at Port pin. 1: /SYSCLK output routed to Port pin.
2	SMB0E	**SMBus I/O Enable.** 0: SMBus I/O unavailable at Port pins. 1: SMBus I/O (SDA, SCL) routed to Port pins.
1	URX0E	**UART RX Input Enable.** 0: UART RX unavailable at Port pin. 1: UART RX0 routed to Port pin P0.5.
0	UTX0E	**UART TX Output Enable.** 0: UART TX0 unavailable at Port pin. 1: UART TX0 routed to Port pin P0.4.

23.5. SMBus Transfer Modes

The SMBus interface may be configured to operate as master and/or slave. At any particular time, it will be operating in one of the following four modes: Master Transmitter, Master Receiver, Slave Transmitter, or Slave Receiver. The SMBus interface enters Master Mode any time a START is generated, and remains in Master Mode until it loses an arbitration or generates a STOP. An SMBus interrupt is generated at the end of all SMBus byte frames. As a receiver, the interrupt for an ACK occurs **before** the ACK. As a transmitter, interrupts occur **after** the ACK.

23.5.1. Write Sequence (Master)

During a write sequence, an SMBus master writes data to a slave device. The master in this transfer will be a transmitter during the address byte, and a transmitter during all data bytes. The SMBus interface generates the START condition and transmits the first byte containing the address of the target slave and the data direction bit. In this case the data direction bit (R/W) will be logic 0 (WRITE). The master then transmits one or more bytes of serial data. After each byte is transmitted, an acknowledge bit is generated by the slave. The transfer is ended when the STO bit is set and a STOP is generated. Note that the interface will switch to Master Receiver Mode if SMB0DAT is not written following a Master Transmitter interrupt. Figure 23.5 shows a typical master write sequence. Two transmit data bytes are shown, though any number of bytes may be transmitted. Notice that all of the “data byte transferred” interrupts occur **after** the ACK cycle in this mode.

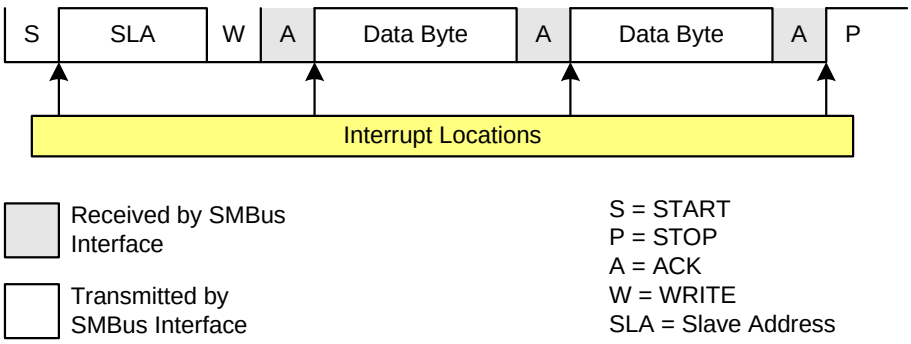

Figure 23.5. Typical Master Write Sequence

SFR Definition 25.3. TMOD: Timer Mode

Bit	7	6	5	4	3	2	1	0
Name	GATE1	C/T1	T1M[1:0]		GATE0	C/T0	T0M[1:0]	
Type	R/W	R/W	R/W		R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x89

Bit	Name	Function
7	GATE1	**Timer 1 Gate Control.** 0: Timer 1 enabled when TR1 = 1 irrespective of $\overline{INT1}$ logic level. 1: Timer 1 enabled only when TR1 = 1 AND $\overline{INT1}$ is active as defined by bit IN1PL in register IT01CF (see SFR Definition 17.5).
6	C/T1	**Counter/Timer 1 Select.** 0: Timer: Timer 1 incremented by clock defined by T1M bit in register CKCON. 1: Counter: Timer 1 incremented by high-to-low transitions on external pin (T1).
5:4	T1M[1:0]	**Timer 1 Mode Select.** These bits select the Timer 1 operation mode. 00: Mode 0, 13-bit Counter/Timer 01: Mode 1, 16-bit Counter/Timer 10: Mode 2, 8-bit Counter/Timer with Auto-Reload 11: Mode 3, Timer 1 Inactive
3	GATE0	**Timer 0 Gate Control.** 0: Timer 0 enabled when TR0 = 1 irrespective of $\overline{INT0}$ logic level. 1: Timer 0 enabled only when TR0 = 1 AND $\overline{INT0}$ is active as defined by bit IN0PL in register IT01CF (see SFR Definition 17.5).
2	C/T0	**Counter/Timer 0 Select.** 0: Timer: Timer 0 incremented by clock defined by T0M bit in register CKCON. 1: Counter: Timer 0 incremented by high-to-low transitions on external pin (T0).
1:0	T0M[1:0]	**Timer 0 Mode Select.** These bits select the Timer 0 operation mode. 00: Mode 0, 13-bit Counter/Timer 01: Mode 1, 16-bit Counter/Timer 10: Mode 2, 8-bit Counter/Timer with Auto-Reload 11: Mode 3, Two 8-bit Counters/Timers

26.3.4. Frequency Output Mode

Frequency Output Mode produces a programmable-frequency square wave on the module's associated CEXn pin. The Capture/Compare module high byte holds the number of PCA clocks to count before the output is toggled. The frequency of the square wave is then defined by Equation 26.1.

$$F_{CEXn} = \frac{F_{PCA}}{2 \times PCA0CPHn}$$

Note: A value of 0x00 in the PCA0CPHn register is equal to 256 for this equation.

Equation 26.1. Square Wave Frequency Output

Where F_{PCA} is the frequency of the clock selected by the CPS2–0 bits in the PCA mode register, PCA0MD. The lower byte of the capture/compare module is compared to the PCA counter low byte; on a match, CEXn is toggled and the offset held in the high byte is added to the matched value in PCA0CPLn. Frequency Output Mode is enabled by setting the ECOMn, TOGn, and PWMn bits in the PCA0CPMn register. Note that the MATn bit should normally be set to 0 in this mode. If the MATn bit is set to 1, the CCFn flag for the channel will be set when the 16-bit PCA0 counter and the 16-bit capture/compare register for the channel are equal.

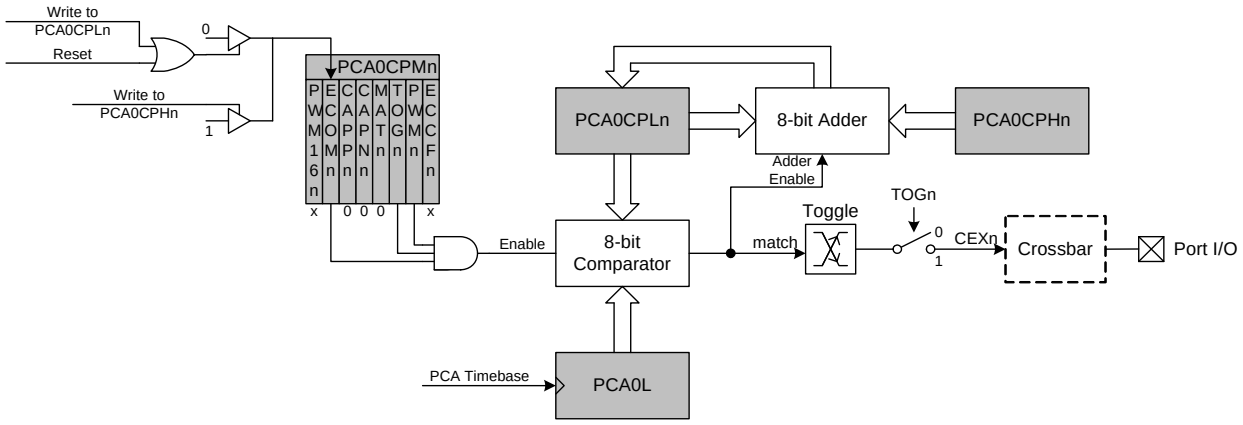

Figure 26.7. PCA Frequency Output Mode

C2 Register Definition 27.10. CRC0: CRC Byte 0

Bit	7	6	5	4	3	2	1	0
Name	CRC[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

C2 Address: 0xA9

Bit	Name	Function
7:0	CRC[7:0]	**CRC Byte 0.** A write to this register initiates a 16-bit CRC of one 256-byte block of EPROM memory. The byte written to CRC0 is the upper byte of the 16-bit address where the CRC will begin. The lower byte of the beginning address is always 0x00. When complete, the 16-bit result will be available in CRC1 (MSB) and CRC0 (LSB). See Section “20.3. Program Memory CRC” on page 99.

C2 Register Definition 27.11. CRC1: CRC Byte 1

Bit	7	6	5	4	3	2	1	0
Name	CRC[15:8]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

C2 Address: 0xAA

Bit	Name	Function
7:0	CRC[15:8]	**CRC Byte 1.** A write to this register initiates a 32-bit CRC on the entire program memory space. The CRC begins at address 0x0000. When complete, the 32-bit result is stored in CRC3 (MSB), CRC2, CRC1, and CRC0 (LSB). See Section “20.3. Program Memory CRC” on page 99.