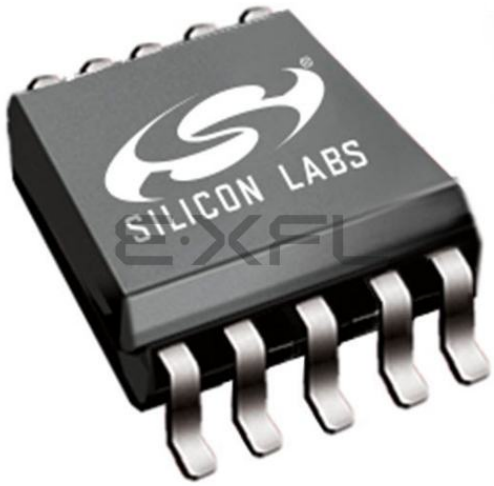

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I²C), UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	6
Program Memory Size	1.5KB (1.5K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	10-TFSOP, 10-MSOP (0.118", 3.00mm Width)
Supplier Device Package	10-MSOP
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051t606-gt

List of Figures

1. System Overview

C8051T600/1/2/3/4/5/6 devices are fully integrated, mixed-signal, system-on-a-chip MCUs. Highlighted features are listed below. Refer to Table 2.1 for specific product feature selection and part ordering numbers.

- High-speed pipelined 8051-compatible microcontroller core (up to 25 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- C8051F300 ISP Flash device is available for quick in-system code development
- 10-bit 500 ksps Single-ended ADC with analog multiplexer and integrated temperature sensor
- Precision calibrated 24.5 MHz internal oscillator
- 8 k, 4 k, 2 k or 1.5 kB of on-chip Byte-Programmable EPROM—(512 bytes are reserved on 8k version)
- 256 or 128 bytes of on-chip RAM
- SMBus/I^2C, and ART serial interfaces implemented in hardware
- Three general-purpose 16-bit timers
- Programmable Counter/Timer Array (PCA) with three capture/compare modules and Watchdog Timer function
- On-chip Power-On Reset and Supply Monitor
- On-chip Voltage Comparator
- 8 or 6 Port I/O

With on-chip power-on reset, V_{DD} monitor, watchdog timer, and clock oscillator, the C8051T600/1/2/3/4/5/6 devices are truly stand-alone, system-on-a-chip solutions. User software has complete control of all peripherals and may individually shut down any or all peripherals for power savings.

Code written for the C8051T600/1/2/3/4/5/6 family of processors will run on the C8051F300 Mixed-Signal ISP Flash microcontroller, providing a quick, cost-effective way to develop code without requiring special emulator circuitry. The C8051T600/1/2/3/4/5/6 processors include Silicon Laboratories' 2-Wire C2 Debug and Programming interface, which allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection of memory, viewing and modification of special function registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

Each device is specified for 1.8–3.6 V operation over the industrial temperature range (–45 to +85 °C). An internal LDO is used to supply the processor core voltage at 1.8 V. The Port I/O and $\overline{RST}$ pins are tolerant of input signals up to 5 V. See Table 2.1 for ordering information. Block diagrams of the devices in the C8051T600/1/2/3/4/5/6 family are shown in Figure 1.1, Figure 1.2, and Figure 1.3.

4. QFN-11 Package Specifications

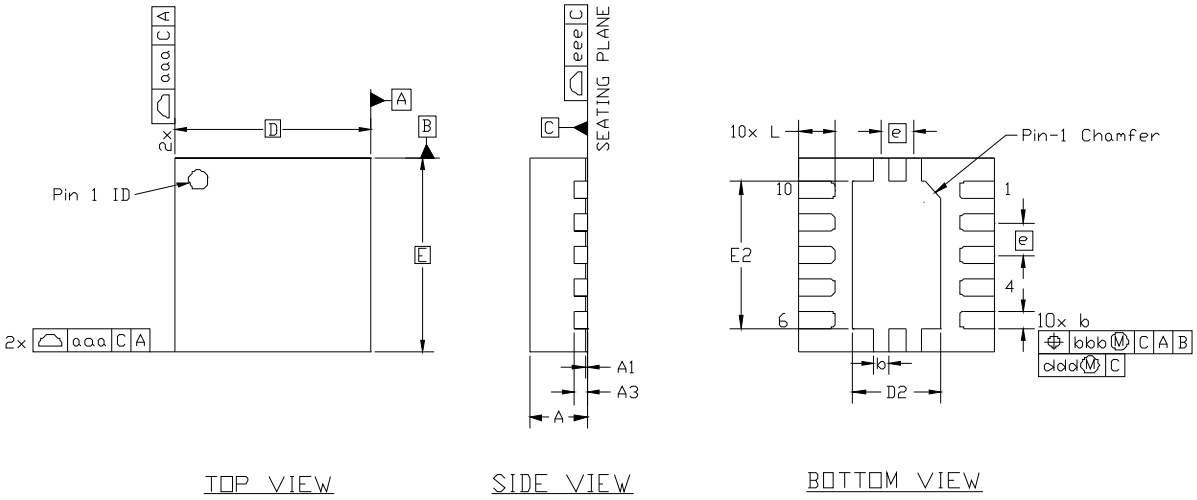

Figure 4.1. QFN-11 Package Drawing

Table 4.1. QFN-11 Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.90	1.00
A1	0.03	0.07	0.11
A3		0.25 REF	
b	0.18	0.25	0.30
D		3.00 BSC	
D2	1.30	1.35	1.40
e		0.50 BSC	

Dimension	Min	Nom	Max
E		3.00 BSC	
E2	2.20	2.25	2.30
L	0.45	0.55	0.65
aaa	—	—	0.15
bbb	—	—	0.15
ddd	—	—	0.05
eee	—	—	0.08

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-243, variation VEED except for custom features D2, E2, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Table 8.10. ADC0 Electrical Characteristics

V_{DD} = 3.0 V, VREF = 2.40 V (REFSL=0), –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
DC Accuracy					
Resolution			10		bits
Integral Nonlinearity		—	±0.5	±1	LSB
Differential Nonlinearity	Guaranteed Monotonic	—	±0.5	±1	LSB
Offset Error		–2	0	2	LSB
Full Scale Error		–2	0	2	LSB
Offset Temperature Coefficient		—	45	—	ppm/°C
Dynamic performance (10 kHz sine-wave single-ended input, 1 dB below Full Scale, 500 ksps)					
Signal-to-Noise Plus Distortion		56	60	—	dB
Total Harmonic Distortion	Up to the 5th harmonic	—	72	—	dB
Spurious-Free Dynamic Range		—	–75	—	dB
Conversion Rate					
SAR Conversion Clock		—	—	8.33	MHz
Conversion Time in SAR Clocks	10-bit Mode 8-bit Mode	13 11	— —	— —	clocks clocks
Track/Hold Acquisition Time	$V_{DD} \geq 2.0$ V $V_{DD} < 2.0$ V	300 2.0	— —	— —	ns µs
Throughput Rate		—	—	500	ksps
Analog Inputs					
ADC Input Voltage Range		0	—	VREF	V
Sampling Capacitance	1x Gain 0.5x Gain	— —	5 3	— —	pF pF
Input Multiplexer Impedance		—	5	—	kΩ
Power Specifications					
Power Supply Current (V_{DD} supplied to ADC0)	Operating Mode, 500 ksps	—	600	900	µA
Power Supply Rejection		—	–70	—	dB

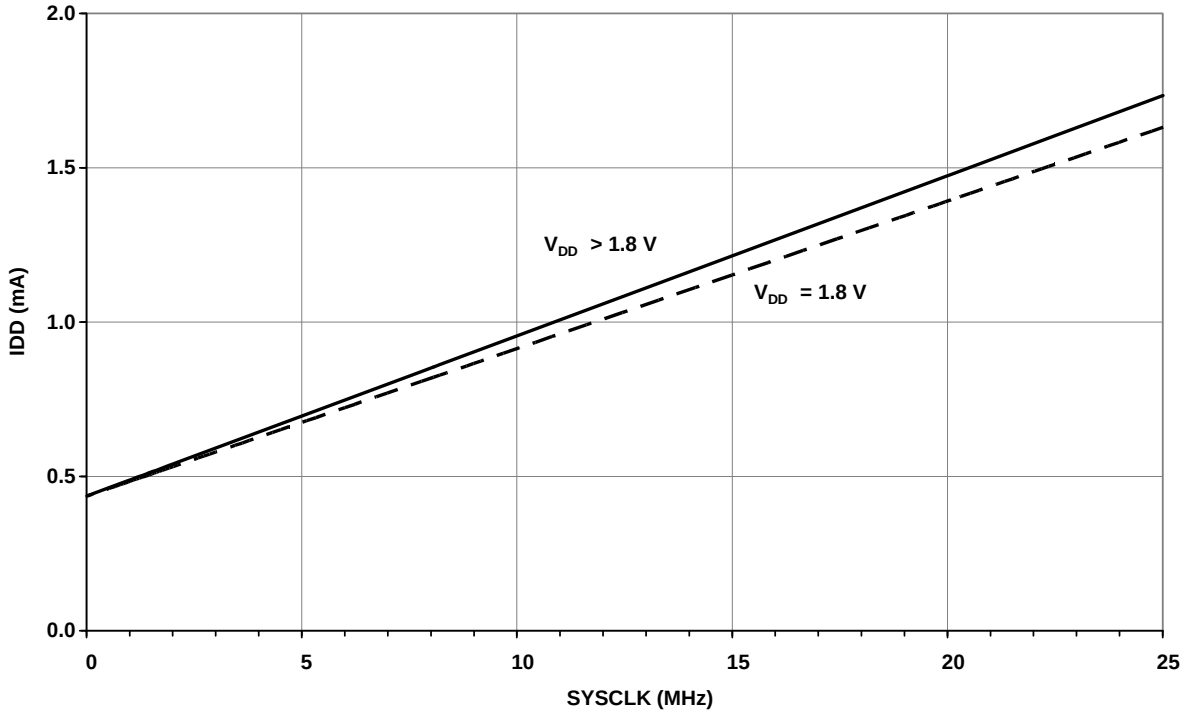

Figure 8.3. C8051T600/1/2/3/4/5 Idle Mode Supply Current vs. Frequency (MPCE = 1)

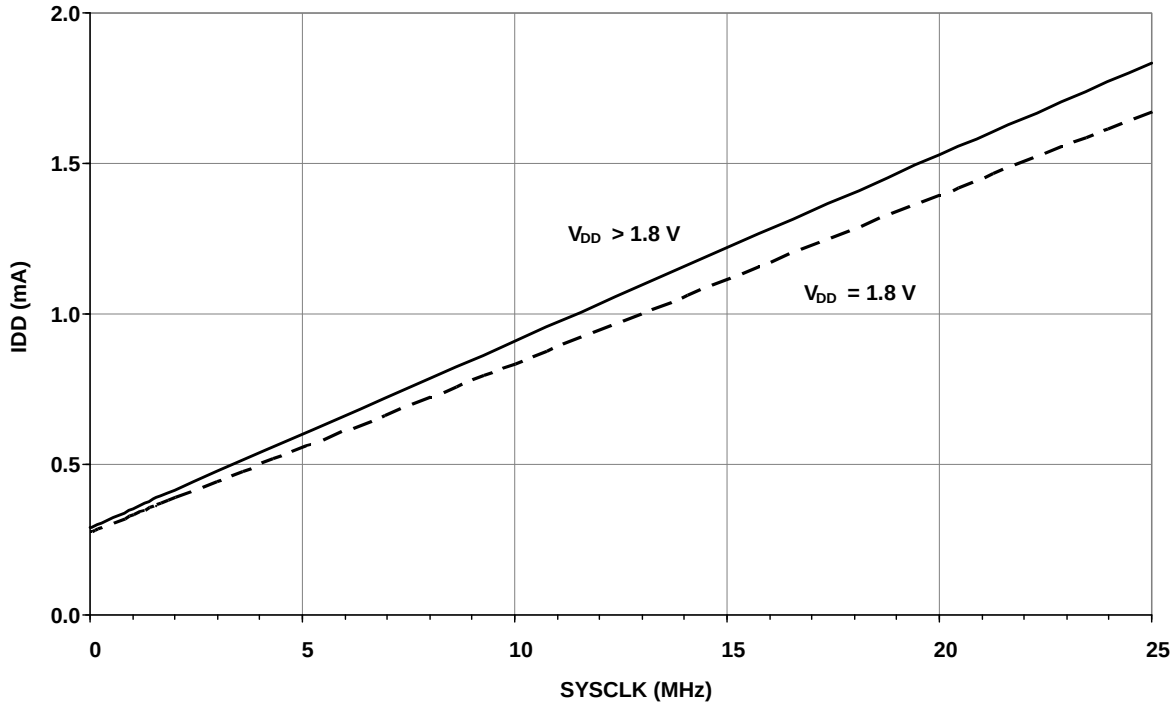

Figure 8.4. C8051T606 Idle Mode Digital Current vs. Frequency (MPCE = 1)

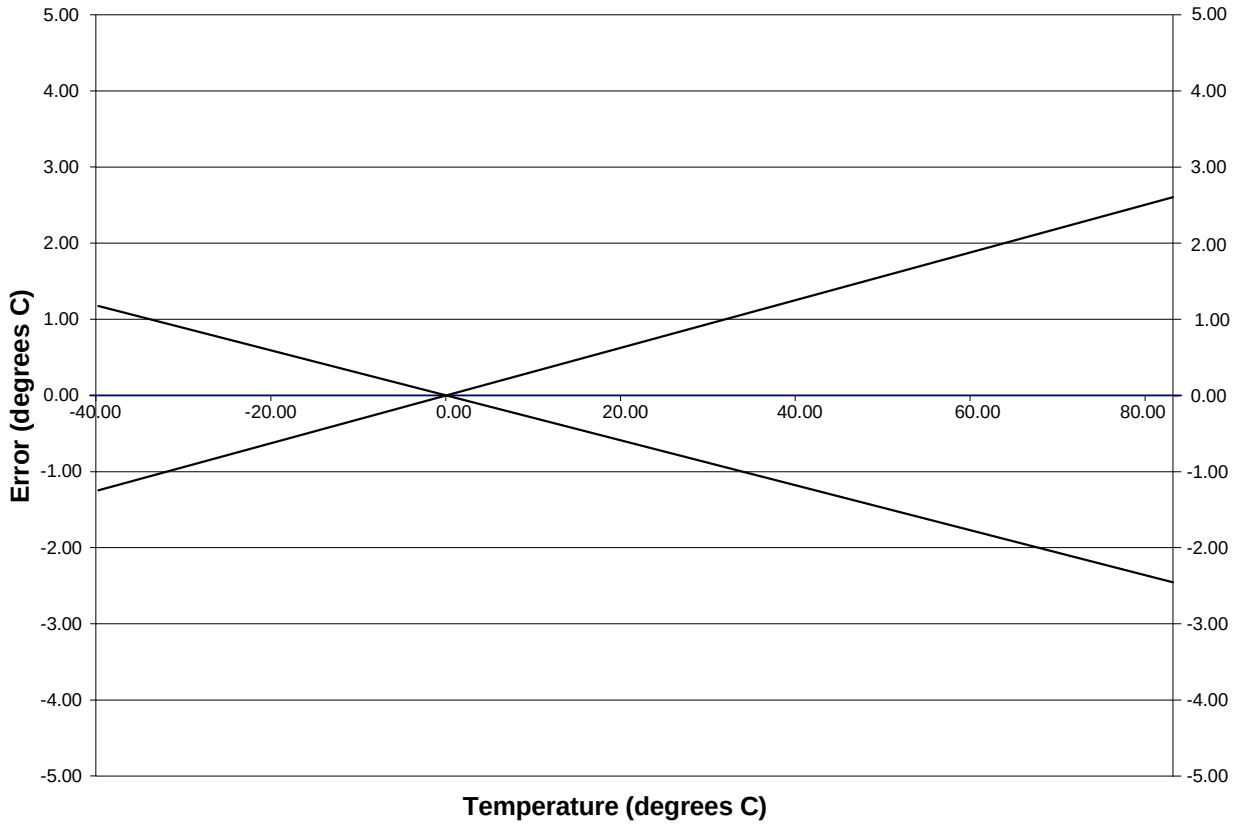

Figure 10.2. Temperature Sensor Error with 1-Point Calibration at 0 °C

SFR Definition 12.1. REG0CN: Voltage Regulator Control

Bit	7	6	5	4	3	2	1	0
Name	STOPCF	BYPASS						MPCE
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xC7

Bit	Name	Function
7	STOPCF	**Stop Mode Configuration.** This bit configures the regulator's behavior when the device enters STOP mode. 0: Regulator is still active in STOP mode. Any enabled reset source will reset the device. 1: Regulator is shut down in STOP mode. Only the $\overline{RST}$ pin or power cycle can reset the device.
6	BYPASS	**Bypass Internal Regulator.** This bit places the regulator in bypass mode, turning off the regulator, and allowing the core to run directly from the V_{DD} supply pin. 0: Normal Mode—Regulator is on. 1: Bypass Mode—Regulator is off, and the microcontroller core operates directly from the V_{DD} supply voltage. **IMPORTANT: Bypass mode is for use with an external regulator as the supply voltage only. Never place the regulator in bypass mode when the V_{DD} supply voltage is greater than the specifications given in Table 8.1 on page 30. Doing so may cause permanent damage to the device.**
5:1	Reserved	Reserved. Must Write 00000b.
0	MPCE	**Memory Power Controller Enable.** This bit can help the system save power at slower system clock frequencies (about 2.0 MHz or less) by automatically shutting down the EPROM memory between clocks when information is not being fetched from the EPROM memory. 0: Normal Mode—Memory power controller disabled (EPROM memory is always on). 1: Low Power Mode—Memory power controller enabled (EPROM memory turns on/off as needed). **Note:** If an external clock source is used with the Memory Power Controller enabled, and the clock frequency changes from slow (<2.0 MHz) to fast (> 2.0 MHz), the EPROM power will turn on, and up to 20 clocks may be "skipped" to ensure that the EPROM power is stable before reading memory.

13. Comparator0

C8051T600/1/2/3/4/5/6 devices include an on-chip programmable voltage comparator, Comparator0, shown in Figure 13.1.

The Comparator offers programmable response time and hysteresis, an analog input multiplexer, and two outputs that are optionally available at the Port pins: a synchronous “latched” output (CP0), or an asynchronous “raw” output (CP0A). The asynchronous CP0A signal is available even when the system clock is not active. This allows the Comparator to operate and generate an output with the device in STOP mode. When assigned to a Port pin, the Comparator output may be configured as open drain or push-pull (see Section “22.4. Port I/O Initialization” on page 114). Comparator0 may also be used as a reset source (see Section “19.5. Comparator0 Reset” on page 94).

The Comparator0 inputs are selected by the comparator input multiplexer, as detailed in Section “13.1. Comparator Multiplexer” on page 63.

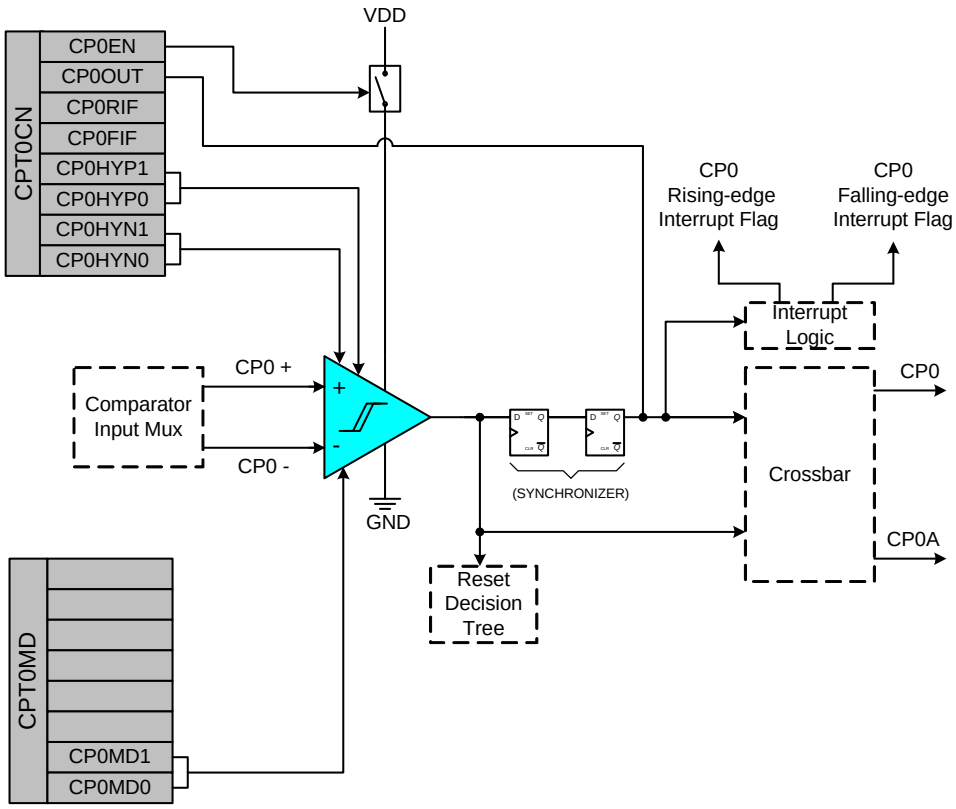

Figure 13.1. Comparator0 Functional Block Diagram

The Comparator output can be polled in software, used as an interrupt source, and/or routed to a Port pin. When routed to a Port pin, the Comparator output is available asynchronous or synchronous to the system clock; the asynchronous output is available even in STOP mode (with no system clock active). When disabled, the Comparator output (if assigned to a Port I/O pin via the Crossbar) defaults to the logic low state, and the power supply to the comparator is turned off. See Section “22.3. Priority Crossbar Decoder” on page 111 for details on configuring Comparator outputs via the digital Crossbar. Comparator inputs can be

15.2. Data Memory

The C8051T600/1/2/3/4/5 devices include 256 bytes of RAM, and the C8051T606 devices include 128 bytes of RAM. This memory is mapped into the internal data memory space of the 8051 controller core. The RAM memory organization of the C8051T600/1/2/3/4/5/6 device family is shown in Figure 15.2

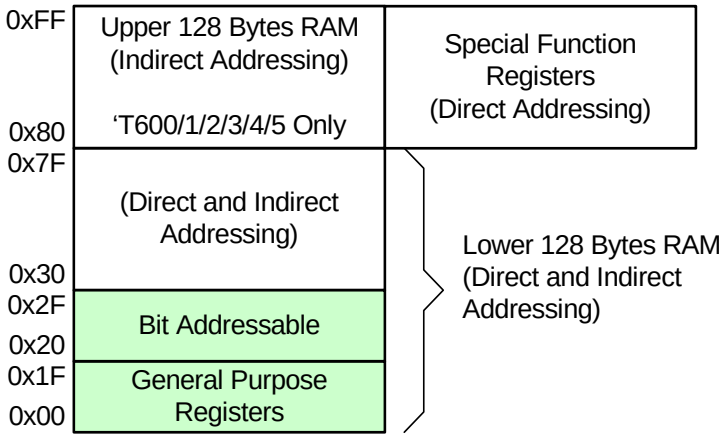

Figure 15.2. RAM Memory Map

15.2.1. Internal RAM

The 256 bytes of internal RAM on the C8051T600/1/2/3/4/5 are mapped into the data memory space from 0x00 through 0xFF. The 128 bytes of internal RAM on the C8051T606 are mapped into the data memory space from 0x00 through 0x7F. The 128 bytes of data memory from 0x00 to 0x7F on all devices are used for general purpose registers and scratch pad memory. Either direct or indirect addressing may be used to access these 128 bytes of data memory. Locations 0x00 through 0x1F are addressable as four banks of general purpose registers, each bank consisting of eight byte-wide registers. The next 16 bytes, locations 0x20 through 0x2F, may either be addressed as bytes or as 128 bit locations accessible with the direct addressing mode.

The upper 128 bytes of data memory available on the C8051T600/1/2/3/4/5 are accessible only by indirect addressing. This region occupies the same address space as the Special Function Registers (SFR) but is physically separate from the SFR space. The addressing mode used by an instruction when accessing locations above 0x7F determines whether the CPU accesses the upper 128 bytes of data memory space or the SFRs. Instructions that use direct addressing will access the SFR space. Instructions using indirect addressing above 0x7F access the upper 128 bytes of data memory. Figure 15.2 illustrates the data memory organization of the C8051T600/1/2/3/4/5/6.

Table 16.2. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	Description	Page
ADC0GTL	0xC3	ADC0 Greater-Than Compare Low	47
ADC0H	0xBE	ADC0 High	45
ADC0L	0xBD	ADC0 Low	45
ADC0LTH	0xC6	ADC0 Less-Than Compare Word High	48
ADC0LTL	0xC5	ADC0 Less-Than Compare Word Low	48
AMX0SL	0xBB	AMUX0 Multiplexer Channel Select	51
B	0xF0	B Register	72
CKCON	0x8E	Clock Control	146
CPT0CN	0xF8	Comparator0 Control	61
CPT0MD	0x9D	Comparator0 Mode Selection	62
CPT0MX	0x9F	Comparator0 MUX Selection	64
DPH	0x83	Data Pointer High	71
DPL	0x82	Data Pointer Low	71
EIE1	0xE6	Extended Interrupt Enable 1	85
EIP1	0xF6	Extended Interrupt Priority 1	86
IE	0xA8	Interrupt Enable	83
IP	0xB8	Interrupt Priority	84
IT01CF	0xE4	INT0/INT1 Configuration	88
OSCICL	0xB3	Internal Oscillator Calibration	101
OSCICN	0xB2	Internal Oscillator Control	102
OSCXCN	0xB1	External Oscillator Control	104
P0	0x80	Port 0 Latch	118
P0MDIN	0xF1	Port 0 Input Mode Configuration	119
P0MDOUT	0xA4	Port 0 Output Mode Configuration	119
PCA0CN	0xD8	PCA Control	173
PCA0CPH0	0xFC	PCA Capture 0 High	177
PCA0CPH1	0xEA	PCA Capture 1 High	177
PCA0CPH2	0xEC	PCA Capture 2 High	177
PCA0CPL0	0xFB	PCA Capture 0 Low	177
PCA0CPL1	0xE9	PCA Capture 1 Low	177
PCA0CPL2	0xEB	PCA Capture 2 Low	177
PCA0CPM0	0xDA	PCA Module 0 Mode Register	175
PCA0CPM1	0xDB	PCA Module 1 Mode Register	175
PCA0CPM2	0xDC	PCA Module 2 Mode Register	175

17.3. INT0 and INT1 External Interrupt Sources

The INT0 and INT1 external interrupt sources are configurable as active high or low, edge or level sensitive. The IN0PL (INT0 Polarity) and IN1PL (INT1 Polarity) bits in the IT01CF register select active high or active low; the IT0 and IT1 bits in TCON (Section “25.1. Timer 0 and Timer 1” on page 147) select level or edge sensitive. The table below lists the possible configurations.

IT0	IN0PL	/INT0 Interrupt
1	0	Active low, edge sensitive
1	1	Active high, edge sensitive
0	0	Active low, level sensitive
0	1	Active high, level sensitive

IT1	IN1PL	/INT1 Interrupt
1	0	Active low, edge sensitive
1	1	Active high, edge sensitive
0	0	Active low, level sensitive
0	1	Active high, level sensitive

INT0 and INT1 are assigned to Port pins as defined in the IT01CF register (see SFR Definition 17.5). Note that INT0 and INT0 Port pin assignments are independent of any Crossbar assignments. INT0 and INT1 will monitor their assigned Port pins without disturbing the peripheral that was assigned the Port pin via the Crossbar. To assign a Port pin only to INT0 and/or INT1, configure the Crossbar to skip the selected pin(s). This is accomplished by setting the associated bit in register XBR0 (see Section “22.3. Priority Crossbar Decoder” on page 111 for complete details on configuring the Crossbar).

IE0 (TCON.1) and IE1 (TCON.3) serve as the interrupt-pending flags for the INT0 and INT1 external interrupts, respectively. If an INT0 or INT1 external interrupt is configured as edge-sensitive, the corresponding interrupt-pending flag is automatically cleared by the hardware when the CPU vectors to the ISR. When configured as level sensitive, the interrupt-pending flag remains logic 1 while the input is active as defined by the corresponding polarity bit (IN0PL or IN1PL); the flag remains logic 0 while the input is inactive. The external interrupt source must hold the input active until the interrupt request is recognized. It must then deactivate the interrupt request before execution of the ISR completes or another interrupt request will be generated.

22.2. Assigning Port I/O Pins to Analog and Digital Functions

Port I/O pins can be assigned to various analog, digital, and external interrupt functions. The Port pins assigned to analog functions should be configured for analog I/O, and Port pins assigned to digital or external interrupt functions should be configured for digital I/O.

22.2.1. Assigning Port I/O Pins to Analog Functions

Table 22.1 shows all available analog functions that require Port I/O assignments. **Port pins selected for these analog functions should have their corresponding bit in XBR0 set to 1.** This reserves the pin for use by the analog function and does not allow it to be claimed by the crossbar. Table 22.1 shows the potential mapping of Port I/O to each analog function.

Table 22.1. Port I/O Assignment for Analog Functions

Analog Function	Potentially Assignable Port Pins	SFR(s) used for Assignment
ADC Input	P0.0–P0.7	AMX0SL, XBR0
Comparator0 Input	P0.0–P0.7	CPT0MX, XBR0
Voltage Reference Input for ADC (VREF)	P0.0	REF0CN, XBR0
External Oscillator in RC or C Mode (EXTCLK)	P0.3	OSCXCN, XBR0

22.2.2. Assigning Port I/O Pins to Digital Functions

Any Port pins not assigned to analog functions may be assigned to digital functions or used as GPIO. Most digital functions rely on the crossbar for pin assignment; however, some digital functions bypass the crossbar in a manner similar to the analog functions listed above. **Port pins used by these digital functions and any Port pins selected for use as GPIO should have their corresponding bit in XBR0 set to 1.** Table 22.2 shows all available digital functions and the potential mapping of Port I/O to each digital function.

Table 22.2. Port I/O Assignment for Digital Functions

Digital Function	Potentially Assignable Port Pins	SFR(s) used for Assignment
UART0, SMBus, CP0, CP0A, SYSCLK, PCA0 (CEX0-2 and ECI), T0 or T1.	Any Port pin available for assignment by the crossbar. This includes P0.0 - P0.7 pins which have their XBR0 bit set to 0. **Note:** The crossbar will always assign UART0 pins to P0.4 and P0.5.	XBR1, XBR2
Any pin used for GPIO	P0.0–P0.7	XBR0

22.3. Priority Crossbar Decoder

The Priority Crossbar Decoder (Figure 22.3) assigns a priority to each I/O function, starting at the top with UART0. When a digital resource is selected, the least-significant unassigned Port pin is assigned to that resource (excluding UART0, which is always at pins P0.4 and P0.5). If a Port pin is assigned, the crossbar skips that pin when assigning the next selected resource. Additionally, the crossbar will skip Port pins whose associated bits in the XBR0 register are set. The XBR0 register allows software to skip Port pins that are to be used for analog input, dedicated functions, or GPIO.

Important note on crossbar configuration: If a Port pin is claimed by a peripheral without use of the crossbar, its corresponding XBR0 bit should be set. This applies to P0.0 if VREF is used, P0.3 if the external oscillator circuit is enabled, P0.6 if the ADC is configured to use the external conversion start signal (CNVSTR), and any selected ADC or comparator inputs. The crossbar skips selected pins as if they were already assigned, and moves to the next unassigned pin. Figure 22.3 shows the potential pin assigments available to the crossbar peripherals. Figure 22.4 and Figure 22.5 show two example crossbar configurations, with and without skipping pins.

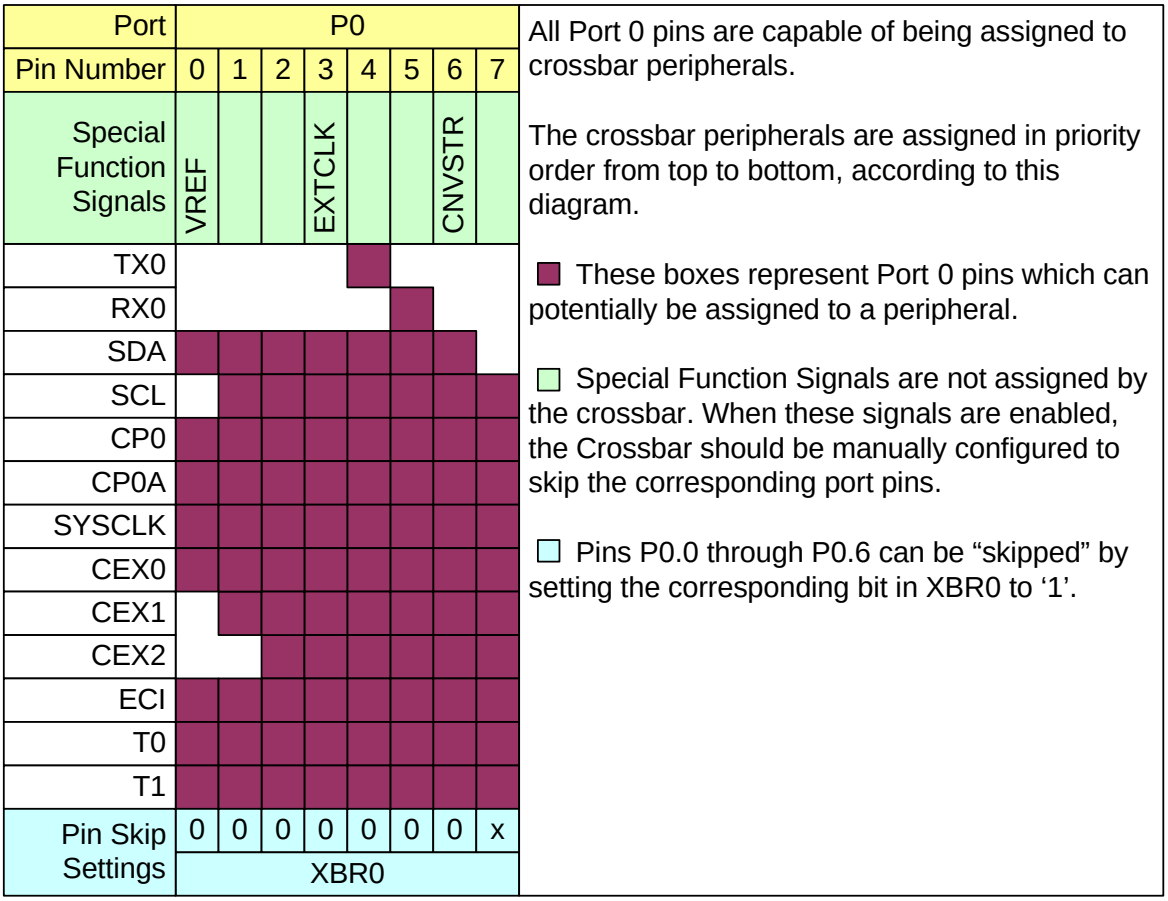

Figure 22.3. Priority Crossbar Decoder Potential Pin Assignments

22.4. Port I/O Initialization

Port I/O initialization consists of the following steps:

1. Select the input mode (analog or digital) for all Port pins, using the Port Input Mode register (P0MDIN).
2. Select the output mode (open-drain or push-pull) for all Port pins, using the Port Output Mode register (P0MDOUT).
3. Select any pins to be skipped by the I/O crossbar using the XBR0 register.
4. Assign Port pins to desired peripherals.
5. Enable the crossbar (XBARE = 1).

All Port pins must be configured as either analog or digital inputs. Any pins to be used as Comparator or ADC inputs should be configured as analog inputs. When a pin is configured as an analog input, its weak pullup, digital driver, and digital receiver are disabled. This process saves power and reduces noise on the analog input. Pins configured as digital inputs may still be used by analog peripherals; however this practice is not recommended.

Additionally, all analog input pins should be configured to be skipped by the crossbar (accomplished by setting the associated bits in XBR0). Port input mode is set in the P0MDIN register, where a 1 indicates a digital input, and a 0 indicates an analog input. All pins default to digital inputs on reset. See SFR Definition 22.5 for the P0MDIN register details.

The output driver characteristics of the I/O pins are defined using the Port Output Mode register (P0MDOUT). Each Port Output driver can be configured as either open drain or push-pull. This selection is required even for the digital resources selected in the XBRn registers, and is not automatic. The only exception to this is the SMBus (SDA, SCL) pins, which are configured as open-drain regardless of the P0MDOUT settings. When the WEAKPUD bit in XBR2 is 0, a weak pullup is enabled for all Port I/O configured as open-drain. WEAKPUD does not affect the push-pull Port I/O. Furthermore, the weak pullup is turned off on an output that is driving a 0 to avoid unnecessary power dissipation.

Registers XBR1 and XBR2 must be loaded with the appropriate values to select the digital I/O functions required by the design. Setting the XBARE bit in XBR2 to 1 enables the crossbar. Until the crossbar is enabled, the external pins remain as standard Port I/O (in input mode), regardless of the XBRn Register settings. For given XBRn Register settings, one can determine the I/O pin-out using the Priority Decode Table. An alternative is to use the Configuration Wizard utility available on the Silicon Laboratories web site to determine the Port I/O pin-assignments based on the XBRn Register settings.

The crossbar must be enabled to use Port pins as standard Port I/O in output mode. Port output drivers are disabled while the crossbar is disabled.

after SCL transitions from high-to-low. EXTHOLD should be set so that the minimum setup and hold times meet the SMBus Specification requirements of 250 ns and 300 ns, respectively. Table 23.2 shows the minimum setup and hold times for the two EXTHOLD settings. Setup and hold time extensions are typically necessary when SYSCLK is above 10 MHz.

Table 23.2. Minimum SDA Setup and Hold Times

EXTHOLD	Minimum SDA Setup Time	Minimum SDA Hold Time
0	T_{low} – 4 system clocks or 1 system clock + s/w delay*	3 system clocks
1	11 system clocks	12 system clocks
Note: Setup Time for ACK bit transmissions and the MSB of all data transfers. When using software acknowledgement, the s/w delay occurs between the time SMB0DAT or ACK is written and when SI is cleared. Note that if SI is cleared in the same write that defines the outgoing ACK value, s/w delay is zero.		

With the SMBTOE bit set, Timer 3 should be configured to overflow after 25 ms in order to detect SCL low timeouts (see Section “23.3.4. SCL Low Timeout” on page 122). The SMBus interface will force Timer 3 to reload while SCL is high, and allow Timer 3 to count when SCL is low. The Timer 3 interrupt service routine should be used to reset SMBus communication by disabling and re-enabling the SMBus.

SMBus Free Timeout detection can be enabled by setting the SMBFTE bit. When this bit is set, the bus will be considered free if SDA and SCL remain high for more than 10 SMBus clock source periods (see Figure 23.4).

23.4.2. SMB0CN Control Register

SMB0CN is used to control the interface and to provide status information (see SFR Definition 23.2). The higher four bits of SMB0CN (MASTER, TXMODE, STA, and STO) form a status vector that can be used to jump to service routines. MASTER indicates whether a device is the master or slave during the current transfer. TXMODE indicates whether the device is transmitting or receiving data for the current byte.

STA and STO indicate that a START and/or STOP has been detected or generated since the last SMBus interrupt. STA and STO are also used to generate START and STOP conditions when operating as a master. Writing a 1 to STA will cause the SMBus interface to enter Master Mode and generate a START when the bus becomes free (STA is not cleared by hardware after the START is generated). Writing a 1 to STO while in Master Mode will cause the interface to generate a STOP and end the current transfer after the next ACK cycle. If STO and STA are both set (while in Master Mode), a STOP followed by a START will be generated.

As a receiver, writing the ACK bit defines the outgoing ACK value; as a transmitter, reading the ACK bit indicates the value received on the last ACK cycle. ACKRQ is set each time a byte is received, indicating that an outgoing ACK value is needed. When ACKRQ is set, software should write the desired outgoing value to the ACK bit before clearing SI. A NACK will be generated if software does not write the ACK bit before clearing SI. SDA will reflect the defined ACK value immediately following a write to the ACK bit; however SCL will remain low until SI is cleared. If a received slave address is not acknowledged, further slave events will be ignored until the next START is detected.

The ARBLOST bit indicates that the interface has lost an arbitration. This may occur anytime the interface is transmitting (master or slave). A lost arbitration while operating as a slave indicates a bus error condition. ARBLOST is cleared by hardware each time SI is cleared.

The SI bit (SMBus Interrupt Flag) is set at the beginning and end of each transfer, after each byte frame, or when an arbitration is lost; see Table 23.3 for more details.

Important Note About the SI Bit: The SMBus interface is stalled while SI is set; thus SCL is held low, and the bus is stalled until software clears SI.

Table 23.3 lists all sources for hardware changes to the SMB0CN bits. Refer to Table 23.4 for SMBus status decoding using the SMB0CN register.

SFR Definition 23.2. SMB0CN: SMBus Control

Bit	7	6	5	4	3	2	1	0
Name	MASTER	TXMODE	STA	STO	ACKRQ	ARBLOST	ACK	SI
Type	R	R	R/W	R/W	R	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xC0; Bit-Addressable

Bit	Name	Description	Read	Write
7	MASTER	**SMBus Master/Slave Indicator.** This read-only bit indicates when the SMBus is operating as a master.	0: SMBus operating in slave mode. 1: SMBus operating in master mode.	N/A
6	TXMODE	**SMBus Transmit Mode Indicator.** This read-only bit indicates when the SMBus is operating as a transmitter.	0: SMBus in Receiver Mode. 1: SMBus in Transmitter Mode.	N/A
5	STA	**SMBus Start Flag.**	0: No Start or repeated Start detected. 1: Start or repeated Start detected.	0: No Start generated. 1: When Configured as a Master, initiates a START or repeated START.
4	STO	**SMBus Stop Flag.**	0: No Stop condition detected. 1: Stop condition detected (if in Slave Mode) or pending (if in Master Mode).	0: No STOP condition is transmitted. 1: When configured as a Master, causes a STOP condition to be transmitted after the next ACK cycle. Cleared by Hardware.
3	ACKRQ	**SMBus Acknowledge Request.**	0: No Ack requested 1: ACK requested	N/A
2	ARBLOST	**SMBus Arbitration Lost Indicator.**	0: No arbitration error. 1: Arbitration Lost	N/A
1	ACK	**SMBus Acknowledge.**	0: NACK received. 1: ACK received.	0: Send NACK 1: Send ACK
0	SI	**SMBus Interrupt Flag.** This bit is set by hardware under the conditions listed in Table 15.3. SI must be cleared by software. While SI is set, SCL is held low and the SMBus is stalled.	0: No interrupt pending 1: Interrupt Pending	0: Clear interrupt, and initiate next state machine event. 1: Force interrupt.

23.5.2. Read Sequence (Master)

During a read sequence, an SMBus master reads data from a slave device. The master in this transfer will be a transmitter during the address byte, and a receiver during all data bytes. The SMBus interface generates the START condition and transmits the first byte containing the address of the target slave and the data direction bit. In this case the data direction bit (R/W) will be logic 1 (READ). Serial data is then received from the slave on SDA while the SMBus outputs the serial clock. The slave transmits one or more bytes of serial data.

The ACKRQ bit is set to 1 and an interrupt is generated after each received byte. Software must write the ACK bit at that time to ACK or NACK the received byte.

Writing a 1 to the ACK bit generates an ACK; writing a 0 generates a NACK. Software should write a 0 to the ACK bit for the last data transfer to transmit a NACK. The interface exits Master Receiver Mode after the STO bit is set and a STOP is generated. The interface will switch to Master Transmitter Mode if SMB0DAT is written while an active Master Receiver. Figure 23.6 shows a typical master read sequence. Two received data bytes are shown, though any number of bytes may be received. Notice that the ‘data byte transferred’ interrupts occur **before** the ACK.

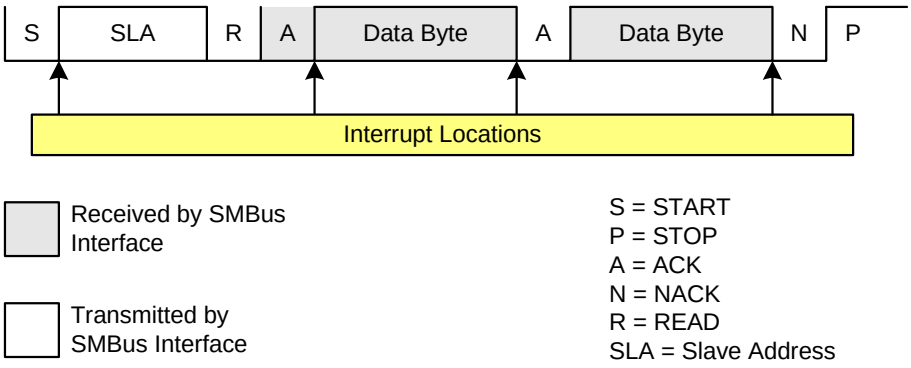

Figure 23.6. Typical Master Read Sequence

SFR Definition 25.4. TL0: Timer 0 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TL0[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x8A

Bit	Name	Function
7:0	TL0[7:0]	**Timer 0 Low Byte.** The TL0 register is the low byte of the 16-bit Timer 0.

SFR Definition 25.5. TL1: Timer 1 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TL1[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x8B

Bit	Name	Function
7:0	TL1[7:0]	**Timer 1 Low Byte.** The TL1 register is the low byte of the 16-bit Timer 1.

27.2. C2 Pin Sharing

The C2 protocol allows the C2 pins to be shared with user functions so that in-system debugging and EPROM programming functions may be performed. This is possible because C2 communication is typically performed when the device is in the halt state, where all on-chip peripherals and user software are stalled. In this halted state, the C2 interface can safely ‘borrow’ the C2CK (normally $\overline{\text{RST}}$) and C2D pins. In most applications, external resistors are required to isolate C2 interface traffic from the user application when performing debug functions. These external resistors are not necessary for production boards. A typical isolation configuration is shown in Figure 27.1.

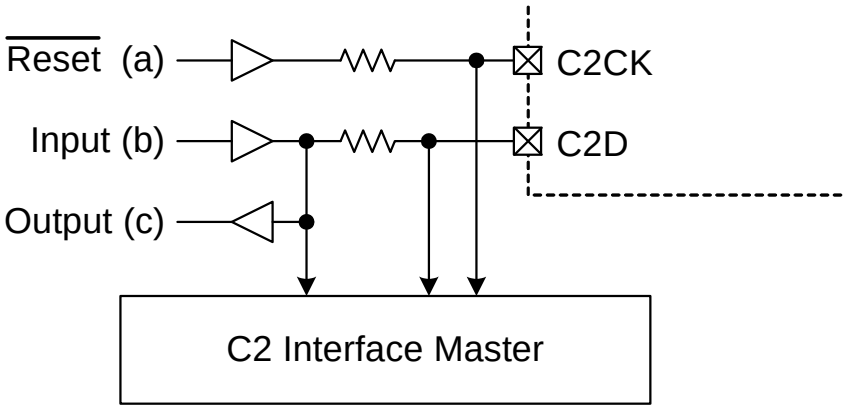

Figure 27.1. Typical C2 Pin Sharing

The configuration in Figure 27.1 assumes the following:

1. The user input (b) cannot change state while the target device is halted.
2. The $\overline{\text{RST}}$ pin on the target device is used as an input only.

Additional resistors may be necessary depending on the specific application.